HARDWARE-ACCELERATED LOCALIZATION FOR AUTOMATED LICENSE PLATE RECOGNITION SYSTEM

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For my beloved family.

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ABSTRACT

Automatic License Plate Recognition (ALPR) is a continuous process of extracting license plate information from a series of input images. Localization is an imperative stage in ALPR system because it extracts the sub image which contains the potential license plate for subsequent processing. Many ALPR systems are designed to operate on general purpose processor, in which the low degree of instruction and data level parallelism is not maximized, resulting in lower efficiency. Also, current ALPR system in the market is not modular and generalized to cater license plates from different nations with different languages and standards. This project proposes a multi-feature extraction algorithm for license plate localization catering various plate and environment variation factors, as well as hardware architecture to implement the algorithm with full modularity baseline. The proposed hardware architecture has been successfully modelled and implemented using System Verilog. It achieves an average speed up of $222 \times$ across different test images compared to software-based algorithm and 100% matching the localization accuracy in software.

ABSTRAK

Pengenalan Plat Lesen Automatik (PPLA) adalah satu proses berterusan yang mengekstrak maklumat plat lesen daripada beberapa siri imej input. Lokalisasi adalah peringkat yang penting dalam sistem PPLA kerana ia memproses sub-imej yang mengandungi plat lesen untuk pemprosesan selanjutnya. Kebanyakan sistem PPLA direka bentuk untuk beroperasi menggunakan mikroprosesor serbaguna, di mana aturan sistem dan data yang rendah tidak dioptimumkan, mengakibatkan kecekapan sistem yang rendah. Sistem PPLA semasa di pasaran tidak dapat membezakan plat lesen dari negara-negara yang berbeza dari segi bahasa dan spesifikasi. Projek ini mencadangkan satu algoritma lokalisasi dalam menganalisa pelbagai jenis ciri imej input untuk faktor plat lesen dan persekitaran. Struktur senibina perkakasan juga dicadangkan untuk melaksanakan algoritma ini dengan suai garis dasar penuh. Sistem yang dicadangkan telah berjaya dimodelkan menggunakan Sistem Verilog. Ia mencapai kelajuan purata 222× daripada seluruh imej cubaan apabila berbanding dengan algoritma berasaskan perisian, dan 100% terbukti sama dengan ketepatan perisian.

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LIST OF ABBREVIATIONS

ALPR	-	Automatic License Plate Recognition
ASIC	-	Application Specific Integrated Circuit
ASM	-	Algorithmic State Machine
CCA	-	Connected Component Analysis
CCL	-	Connected Component Labelling
CCTV	-	Closed-Circuit Television
DFT	-	Discrete Fourier Transform
DSP	-	Digital Signal Processing
DUT	-	Device Under Test
EAV	-	End of Active Video
EDH	-	Error Detection and Handling
FDA	-	Fully Dedicated Architecture
FPGA	-	Field Programmable Gate Array
FSM	-	Finite State Machine
HLS	-	Hue-Luminance-Saturation
IC	-	Integrated Circuit
IP	-	Intellectual Property
ITU	-	International Telecommunication Union
RGB	-	Red-Green-Blue
SAV	-	Start of Active Video
SCW	-	Sliding Concentric Windows
SOM	-	Self-Organizing Map
SVN	-	Support Vector Machine
VEDA	-	Vertical Edge Detection Algorithm
VQ	-	Vector Quantization
WT	-	Wavelet Transform

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CHAPTER 1

INTRODUCTION

1.1 Introduction

The number of motor vehicles on the road increases over the years and it has driven an urgent need to manage these vehicles systematically and efficiently. This results in the emergence of transportation related applications such as traffic monitoring and surveillance, congestion avoidance and control, and automatic electronic payment for toll and parking fee.

Most of these intelligent transportation systems utilize image processing algorithms to process still images or video frames captured remotely. Advanced computer vision technologies in recent years have enabled the development of various efficient software-based algorithms in this field. Researches published in [1] and [2] have provided complete study of computer vision techniques in transportation domain. Many current works utilize neural networks to process and analyze the torrents of traffic images [3,4], but there are very few real time devices being developed.

One of the critical stages in intelligent transportation systems is Automatic License Plate Recognition (ALPR). ALPR is a continuous process of extracting information of license plate from the raw input images captured remotely. They can be color or black and white. There are many different ways of implementing an ALPR system, which is one of the focused research area in past decade [5–8]. At present, many successful commercial software-based ALPR systems are available in the market, but most of them require dedicated camera systems which provide video input acquired under controlled environment [4]. In other words, quality of the acquired images is indeed critical for an ALPR system.

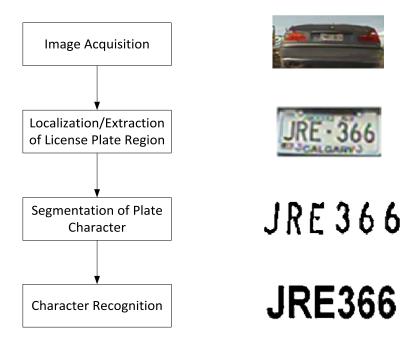


Figure 1.1: Overview of ALPR systems [5].

Another imperative requirement for an efficient ALPR is the processing time. Real time processing is required so that the system will not miss out a single frame in the continuous video stream. The definition of real time is very much dependent on the target traffic flow. For example, the throughput of an ALPR system for highway monitoring ought to be higher than an ALPR system deployed in the residential area with lighter traffic. On a road in residential area, the video stream of 20 frames per second is sufficient for real-time analysis, but this is insufficient for highway with speed limit of 110 km/hour [9]. ALPR systems are generally composed of four processing stages [5] as depicted in Figure 1.1. Table 1.1 provides short descriptions of each ALPR's stage.

1.2 Motivation and Problem Statement

Even this area has been actively researched, many areas of improvement are still possible on existing ALPR systems [5]. Currently, most of the ALPR algorithms are developed based on specific constrained conditions. The implicit assumption for these ALPR systems is that the input video is obtained in a controlled capture environment, via a dedicated camera with high speed and high resolution [4]. A modular and generalized solution which is able to cater license plates from different nations with different languages and standards does not exist at present.

ALPR Stage	Descriptions
Image Acquisition	 Involves capturing of input images using a camera. Heavily dependent on camera parameters: resolution, shutter speed, exposure, light, and orientation. Depends on hardware performance, not many researches have been carried out in this stage. ALPR's main objective is to eliminate hardware dependency in this stage.
Localization of License Plate Region	 To identify the potential license plate region with some image features. The input is raw image acquired by the camera. The output is sub-image of extracted license plate or the coordinates bounding the sub-image. Critical in overall ALPR's recognition accuracy.
Segmentation of Plate Character	 Involves extracting characters from localized plate region. Resolve the undesired problems on the localized sub image which are inherited from previous stage such as tilt and non-uniform brightness.
Character Recognition	 Involves pattern matching algorithm between the segmented characters and a predefined database. Accuracy issue due to non-uniform sizes of the extracted character. Hence, the characters are typically resized before recognition is performed.

 Table 1.1: Summary of ALPR Stages.

Many advanced software-based ALPR systems have been designed to operate on a general purpose processor. The general purpose processor is not efficient at low degree of instruction and data level parallelism to perform real time computation resulting in lower efficiency compared to dedicated hardware with pipelining design [10]. Besides, the general purpose processors require higher power consumption and cost. Hence, there is an intensified need of ALPR system with higher computing power, but lower energy consumption to handle the exponential growth of vehicles [11]. Therefore, hardware implementation of ALPR algorithms has gained much attention during past decade along with the advancement of on-chip processing technology such as Field Programmable Gate Array (FPGA) and Application Specific Integrated Circuit (ASIC).

Analyzing the three compute intensive stages of an ALPR system, it was proven in [12, 13], that the recognition rate can be increased by applying prior knowledge on the potential characters in segmentation stage. Also, certain amount of pre-stored information is required to achieve high accuracy in character recognition stage, which in turns translates to memory requirements [5]. Due to the memory requirement of these two stages, it is more efficient to have them remain in the backend process running on general purpose processors. Hence, there is strong motivation to explore the feasibility of hardware based localization to realize a real-time ALPR system. It is very critical to locate the potential local area containing only license plates and limit the backend compute intensive algorithms operating only on the pixels within this local area [14].

1.3 Aim and Objectives

The aim of this project is to design and develop hardware accelerated localization architecture for ALPR system. To achieve the aim, the objectives of this project are:

- 1. To propose a multi-feature extraction algorithm for license plate localization catering various plate and environment variation factors. This algorithm needs to be simplified for hardware implementation without compromising localization accuracy.
- 2. To design hardware based fully dedicated architecture (FDA) to implement the proposed algorithm with full modularity baseline. This follows by performance analysis and benchmark of the proposed FDA with related works.

1.4 Project Scope

Out of the four ALPR stages described in Section 1.1, this project focuses only on the localization stage. The segmentation and recognition stages are more complicated which require training based on a priori database and hence they are more efficient to be implemented on backend server with higher memory requirements. Hence, the feasibility of accelerating localization stage with dedicated hardware architecture is explored in this project.

It involves analysis of various localization algorithms in term of efficiency, accuracy, and feasibility for hardware implementation, follows by a selection of critical features to be integrated into a multi-feature extraction algorithm for license plate localization. This newly proposed algorithm is developed to address various plate and environment variations which severely impair ALPR's performance. The data format of the input image used in this project is in accordance to Recommendation ITU-R BT.656-4 which describes the means of interconnecting digital television equipment operating on the 525-line or 625-line standards, complying with the 4:2:2 encoding parameters as defined in Recommendation ITU-R BT.601.

A FDA is proposed to implement the multi-feature extraction algorithm for license plate localization. This FDA only extracts a subset of information from the real time video frames acquired by ALPR's front end camera nodes. In this case, information required to be sent to the backend recognition system only consists of potential localized license plate region of smaller resolution. This system decreases the bandwidth requirement between the smart camera and the backend server. Subsequently, performance analysis and algorithm profiling of both hardware and software are performed in term of execution time, localization accuracy and hardware resource utilization.

1.5 Report Organization

This report is divided into six chapters to present the entire project in an organized manner.

In Chapter 2, the theoretical background and related works involved in this project are described. It includes an overview on ALPR system, before focuses on detail discussion of related works in license plate localization and hardware implementation of various localization algorithms. It also includes detail description of Recommendation ITU-R BT.656-4 – the video standard used in this project.

In Chapter 3, methodologies involved in this project are described. It illustrates in detail the five main stages of methodology involved in this project: algorithm development on software-based platform, algorithm validation and verification, algorithm profiling, hardware architecture design, and hardware simulation and verification. In order to give the reader a further insight on this project, the softwares used throughout the course of this project are described in this chapter as well. In Chapter 4, the details of the proposed localization algorithm with multifeature extraction is presented, followed by a series of analysis in term of accuracy based on data set used in this project. Also, overall performance of the proposed localization algorithm developed in MATLAB® is profiled and discussed.

In Chapter 5, the reader will be briefed on the design consideration involved in this project, followed by detailed architectural descriptions of every major hardware module designed. Also, a series of timing diagrams obtained from the simulation process are presented. These simulation results will be analyzed and discussed in this chapter in order to verify the functionality and evaluate the performance of the proposed FDA. A comparison and benchmark summary of the proposed FDA with previous works is also included.

In Chapter 6, the conclusion of this project is made. Also included in this chapter are the limitations of this project and recommendations for future works.

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