SOFTWARE AND HARDWARE CO-SIMULATION PLATFORM FOR IMAGE PROCESSING

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"I hereby declare that I have read this project report and in my
opinion this project report is sufficient in terms of scope
and quality for the award of the degree of
Master of Engineering (Electrical - Computer and Microelectronics System)"

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requirements for the award of the degree of
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My genuine dedications to,

My beloved daddy, mummy and sister;

My enduring supervisor;

My compassionate friends;

And the love ones;

Who are always there for me,

Every step of the way,

Thanks!

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ABSTRACT

Nowadays, modern SoCs have larger scale and complexity. Modelling hardware design archicteture of SoCs normally required RTL design. Since, the system design is getting larger, it is usually partitioned into two parts: software and hardware. For the sack of achieving real time performance, it is essential to map some of the algorithms into hardware. Previously, the hardware and software design of a system are done by different people. Therefore, the design lifecycle is longer. Now, market pressures on short design cycle, maintainability and reusability of system design. To reduce design cycle, a new method must be applied. SystemVerilog is the extension of Verilog HDL that improved with a lot of new features added. Direct programming interface (DPI) is one of the new features whereas it allow SV call C function and vice versa. This work proposed to use Altera-Modelsim simulator to run co-simulation on several test cases: 16-bit unsigned adder, greater common divisor (GCD), 9-tap FIR filter and binary median filter. All the hardware design modelling are using SystemVerilog due to DPI technique can only work with SV. 16-bit unsigned adder and GCD test cases are the startup work before a more complex and real world case studies are applied. 9-tap FIR filter is designed and the input data are passed from random number generator from C function. The output of FIR fitler are verified with C function. Due to window size of median filter is small, line buffer technique is applied in this work. It is a straight forward method and suit for design processing window in digital hardware. The proposed work has overcome the problems faced when running co-simulation based on Modelsim simulator using DPI technique.

ABSTRAK

SoCs kini mempunyai skala yang lebih besar dan rumit. Kebanyakan reka bentuk untuk perkakasan adalah menggunakan teknik RTL. Sistem reka bentuk telah dipechkan kepada dua jenis, iaitu perisian dan perkakasan. Untuk mencapai prestasi masa nyata, sesetengah algoritma perlu dibentukkan dalam perkakasan. Sebelum ini, reka bentuk perkaksan dan perisian adalah dibuat oleh orang yang berlainan. Oleh itu, kitaran hayat reka bentuk akan menjadi lebih panjang. Buat masa ini, pasaran teknologi mempunyai satu trend, iaitu kitaran hayat reka bentuk yang singkat, penyelenggaran dan pengunaan semlua reka bentuk. Demi mengurangkan kitran hayat reka bentuk, kaedah baru haruslah diaplikasi. SystemVerilog merupakan lanjuatan daripada Verilog HDL telah diubahsuaikan dan penambahan fungsi yang banayak. Antaramuka pemprograman terus ialah salah satu fungis baru yang boleh memanggil fungsi dalam bentuk C ke dalam SV atau sebaliknya. Dalam tesis ini, perisian Altera-Modelsim digunakan untuk menjalankan co-simulation terhadap kes-kes ujian yang dipilih. Antara kes ujian yang dipilih ialah 16-bit unsigned adder, pembahagi sepunya yang lebih besar (GCD), penapis FIR dan penapis median binari. Semua reka bentuk perkakasan dimodelkan dengan menggunakan SV. 16-bit unsigned adder dan GCD merupakan kes-kes ujian asas sebelum kes-kes ujian yang lebih rumit dan sebenar diaplikasikan. Data input penapis FIR dipindahkan dari penjana nombor rawak daripada fungsi C. Output penapis FIR akan disahkan dengan fungsi C. Disebabkkan saiz tetingkap penapis median adalah kecil, teknik line buffer digunakan dalam kes ujian ini. Segala masalah yang akan dihadapi semasa simulasi berdasarkan perisian Modelsim mengguanakan teknik DPI telah diatasi dengan mengaplikasikan kes-kes ujian yang dipilih.

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LIST OF ABBREVIATIONS AND SYMBOLS

ALU	-	Arithmetic logic unit
API	-	Application programming interface
ASM	-	Algorithmic sate machine
CWM	-	Center weighted median
DFG	-	Data flow graph
DPI	-	Direct programming interface
FIR	-	Finite impulse response
FPGA	-	Field programmable gate array
GUI	-	Graphic User Interface
HDL	-	Hardware description language
HDVL	-	Hardware decription and verification language
MATLAB	-	Matrix laboratory
MRI	-	Magnetic resonance imaging
PLI	-	Programming language interface
RAM	-	Random access memory
RGB	-	Red Green Blue
RTL	-	Register transfer level
SDFG	-	Signal data flow graph
SFG	-	Signal flow graph
SM	-	Standard median
SoC	-	System-on-chip
SV	-	SystemVerilog
UCDB	-	Unified Coverage Database

VLI	-	Verilog Procedural Interface
2D	-	2-dimensional

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CHAPTER 1

INTRODUCTION

This thesis proposes a co-design simulation model that utilizing the state-of-art SystemVerilog HDVL via direct programming interface (DPI) technique on subsystems of digital signal processing and image processing. This chapter gives an overview of the proposed title and, problem statement, objectives, scope of work, expected contribution and thesis outline.

1.1 Background of Study

Nowadays, modern system-on-chip (SoCs) design is getting more complex and sophisticated. Hardware modeling or design at register transfer level (RTL) will consume a lot of time and effort. It is impossible to integrate every algorithms or problems into a single piece of hardware. Even it is done so, the end product of hardware will be costly and not suitable for the market right now. The market now pressures on short design cycle, hight fault coverage, high speed and low cost. Since the register transfer level design now is getting more complicated, it is advisable that some of the algorithm remain in the

software. Hardware design is done only when performance is taken into concern. This is due to hardware design will speed up the whole system or an application.

There is a report show that functional verification has become the biggest bottleneck as it consumes roughly 70% of chip development time and efforts. RTL testbenches have become more complex and difficult to manage [1]. New method has to be introduced to reduce the verification cycle. Therefore, SystemVerilog (SV) can be used to overcome drawbacks as aforesaid. SV is the extension of Verilog 2001 HDL, contains both hardware description language and hardware verification language [2]. It enhances the design specification method, testbenches language including coverage and assertions application programming interface (API) and direction programming interface (DPI).

Direct programming interface is an interfacing between SystemVerilog and foreign programming language. Usually, the foreign programming language is referred as C or C++ programming language. Designers can call C or C++ code into SystemVerilog or vice versa by using correct protocol and linking model. Hence by using SV and DPI, designers are able to develop a fast co-simulation model to their desired applications. Other than that, designers can use the C/C++ code output result as a golden reference to verify the hardware model designed in HDVL.

Image processing can be defined as 2D function, $f(x,y)$ where x and y are spatial coordinates. Amplitude f is called intensity or gray level of the image [4]. Digital image is a 2D rectangular array of quantized sample values of an image. These quantized values are known as picture elements, image elements and pixels. Basically, digital image processing is a processing of an input image to obtain desired output image. Image analysis is understanding of an image as input to extract some useful information of image output such as features, texture or shape. Computer vision is known as emulating human vision such as face recognition, fingerprint recognition, tracking moving object and etc. Image processing can be applied in many area especially, medical (MRI, X-ray, Ultrasound), military, untouchable territorial explorations (deep space and deep sea), security and surveillance (biometric, border control) and entertainment.

1.2 Problem Statement

With the massive development of electronic information system in today's society, SoCs have bigger and more complicated design. Previously, the hardware and software design are done separately by different designers. The only way to verify the system design is using field programmable gate array (FPGA). However, verification through FPGA will take longer time and more effort due to technical details for FPGA board must be well-equipped. As aforesaid when the design on any applications is getting bigger and complex, the design has to be done by the same person. If the conventional method is used, it will cause more debugging problems and interfacing between hardware and software design. Therefore, it is necessary to ultilize the SystemVerilog HDVL which provides interfacing between SV and C. It enables the same designers to do both software and hardware system design on a co-simulation platform. Hence, the design lifecycle of a system can be greatly reduced.

To achieve real time performance in image processing's application, it is advisable to map some systems design into hardware. It is not a good method to keep every modules of design in software design because a high power computer is needed in order to achieve real time performance. Thus, it is better to design an embedded system for a particular applications. Most of the algorithms of image processing compute intensively such as multiplication and addition. To impove the performance, it is necessary to partition the design into hardware and software instead of keeping every algorithms in software.

1.3 Objectives

The project aims to develop a co-simulation model based on open source software tool, Modelsim simulator by using SystemVerilog HDVL via direct programming interface technique. The main objective are supported by the sub-objectives as follow:

(i) To overcome the problems and discover the limitation of Modelsim simulator when interfacing between SystemVerilog and C functions.

(ii) To propose an efficient design of background noise removal to achieve the real time performance.

1.4 Scope of the Research

The scopes of the work for this thesis are:

(i) SystemVerilog HDVL is used throughout the all the hardware modeling and C programming language is applied for the foreign programming language (Currently DPI only support C but it is designed to be extensible interface that can support other languages [25]).

(ii) Open source software tools such as Quartus II 13.0 and Altera-Modelsim 10.1d are used to ensure this work can be repeated and extended in future.

(iii) Test cases that are applied in this work are limited to these problems: a 16-bit unsigned adder, greater common divisor, 9-tap FIR filter and binary median filter.

1.5 Expected Contribution

The expected contribution of this work is creation a co-simulation environment based on a free software tool, Modelsim simulator with limited features. Most of the technical details as well as limitations about the Modelsim are overcome and discovered by applying several test cases. Moreover, this work will apply the state-of-art hardware description and verification language (HDVL), SystemVerilog. SV is the extension of Verilog HDL with more advanced features such as direct programming interface (DPI). Due to the new release of SV, not many research or papers are published on hardware design using SystemVerilog. In SV, it allows the interfacing between hardware design with software design. In another words, a co-simulation model for software and hardware designs can be developed by ultilizing this state-of-art HDVL. The software designs here are meant to C.

1.6 Thesis Outline

This thesis is organised into six chapters. The first chapter presents the introduction of this work, problem statement, objectives, scope of work and expected contribution of this thesis.

Chapter 2 is the background and literature review chapter. It gives some information of subsystem of image processing, hardware design implementation of median filter. Previous related work on state-of-the-art co-simulation using SystemVerilog DPI is presented as well.

Chapter 3 decribes the methodology of this work. The commands and workflow on how to use DPI in Modelsim simulator are illustrated. A startup example using DPI that *printf("Hello World")* is presented. This is a key point before a more complex test

case is applied. The *import* and *export* are the main keyword to be used to call C function or SV are explained.

Chapter 4 mainly exaplains on the algorithm of the applied in the proposed test cases especially FIR filter and binary median filter. The method being used such as circular buffers and line buffers for data aligning are discussed. The chapter continues with more explanation on the hardware design from algorithms (9-tap FIR filter and binary median filter).

Chapter 5 is the design verification and testing chapter. Results and discussion are given in this chapter. Chapter 6 concludes the limitation of Modelsim simulator and future work to further enhance the co-simulation using SystemVerilog DPI.

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