SILICON NANOWIRE FIELD-EFFECT TRANSISTOR (SINWFET) AND ITS CIRCUIT LEVEL PERFORMANCE

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Dedicated to my beloved parents, my siblings,

and all my friends

for their love and sacrifice.

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ABSTRACT

Since the number of transistors on Integrated Circuit (IC) double every 18 months, the scaling of a device in nanometer is highly required. Due to the downscaling process, conventional Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFET) lead to the short-channel effects, gate-leakage current and interconnect problem. Hence, the introduction of new structure of Silicon Nanowire (SiNW) is necessary and crucial. The SiNW had been proven with an ability to effectively suppress the off-leakage current with its Gate-All-Around (GAA) configuration when compared to the planar MOSFET. In addition, the SiNWFET will be considered to be a promising structure for ultra-CMOS devices to the extend device approaching their downsized limits. This research is accomplished by developing a model of Silicon Nanowire (SiNW) with GAA configuration in MATLAB. In order to evaluate the performance in digital level, HSPICE is used to create its own library based on developed model. The on-current as high as 5µA can be achieved by the *n*-type SiNWFET while *p*-type SiNWFET can reach until same 5µA saturation current. Both models show symmetrical results indicating a fast switching inverter. These models are utilized to build some logic gates in order to further examining their performance in circuit application. The SiNWFET performance is also compared with the nano-MOSFET for benchmarking. The finding of this research is that the SiNWFET model is proven to have better performance than nano-MOSFET in terms of Power Delay Product and Energy Delay Product. Furthermore, when T_{ox} is reduced and R_{si}, N_d and L are increased, a significant device improvement of SiNWFET GAA is attained. This is achieved by having reduced Drain Induced Barrier Lowering, Subthreshold Slope and providing higher I_{on}/I_{off} current ratio by improving the parameter in the device modelling of SiNWFET.

ABSTRAK

Sejak bilangan transistor pada Litar Bersepadu (IC) berganda dalam tempoh 18 bulan, penskalaan peranti dalam nanometer amat diperlukan dan menjadi sangat penting. Disebabkan proses penskalaan, Logam Konvensional Transistor Kesan Magnet Semikonduktor Oksida (MOSFET) boleh membawa kepada kesan saluran pendek, get-arus bocor dan masalah penyambungan. Oleh itu, pengenalan bahan baru seperti Silikon Nanowire (SiNW) adalah perlu dan menjadi sangat penting. SiNW telah dibuktikan berupaya secara efektif menyekat berlakunya kebocoran luar dengan Get-Sekitar-Semua (GAA) apabila dibandingkan dengan MOSFET satah. Di samping itu, SiNWFET dipertimbangkan menjanjikan pencapaian yang lebih baik bagi ultra-CMOS peranti apabila penskalaan dilakukan. Penyelidikan ini membentangkan model Silikon Nanowire (SiNW) dengan konfigurasi GAA menggunakan MATLAB. Bagi tujuan menilai prestasi di peringkat digital, HSPICE digunakan bagi membuat kod tersendiri berdasarkan model yang dibina. Arus litar boleh mencapai sehingga 5μA bagi jenis-*n* manakala jenis-*p* boleh mencapai 5μA bagi kedua-dua keadaan arus tepu. Kedua-dua model menunjukkan kepantasan SiNWFET sebagai litar logik inverter. SiNWFET kemudian dibandingkan dengan logik get untuk menilai prestasi dalam aplikasi litar. Untuk tujuan perbandingan, model ini digunakan untuk membina beberapa get logik dalam membuat perbandingan dengan nano-MOSFET. Hasil yang ditunjukkan daripada kajian ini adalah model SiNWFET dibuktikan mempunyai prestasi yang lebih baik berbanding nano-MOSFET dalam Hasil Darab Kuasa and Hasil Darab Tenaga. Selain daripada itu, apabila T_{ox} and R_{si} dikurangkan, N_d dan L ditingkatkan, prestasi SiNWFET GAA meningkat. Ini kerana, pengurangan Parit Galakan Penyekat Penurunan dan Kecerunan Ambang yang lebih baik serta nisbah I_{on}/I_{off} arus yang tinggi meningkatkan prestasi dengan variasi parameter dalam model SiNWFET.

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LIST OF ABBREVIATIONS

L	-	Channel Length
e	-	Electron charge
G	-	Conductance
I	-	Current
T	-	Temperature
k	-	Wave number
E_g	-	Band gap energy
k_B	-	Boltzmann's constant
m^*	-	Carrier effective mass
E_F	-	Fermi Energy
V_g	-	Gate Voltage
G_0	-	Maximum conductance
q	-	Elementary charge
f_F	-	Fermi-Dirac Distribution
M(E)	-	Number of mode at an energy, E
E	-	Energy
T(E)	-	Transmission probability

$\mathfrak{I}_{-1/2}$	-	Fermi Dirac Integral order of -1/2
SiNW	-	Silicon Nanowire
MOSFET	-	Metal-Oxide Semiconductor Field-Effect Transistor
GAA	-	Gate-All-Around
SPICE	-	Simulation Program with Integrated Circuit Emphasis
MATLAB	-	Matrix Laboratory
I-V	-	Current-Voltage characteristic
CMOS	-	Complementary Metal–Oxide–Semiconductor

LIST OF SYMBOLS

ε_o	-	dielectric constant of vacuum
ε_{ox}	-	dielectric constant of oxide
ε_{Si}	-	dielectric constant of silicon
ε_{SiGe}	-	dielectric constant of silicon germanium
ϕ_F	-	Fermi potential (V)
ϕ_s	-	surface potential (V)
ϕ_{smin}	-	minimum surface potential (V)
$\hbar$	-	Plank constant
l_0	-	mean free path
Γ	-	gamma function
μ_{eff}	-	effective mobility
μ_0	-	low field mobility
χ	-	electron affinity in silicon
χ^{SiGe}	-	electron affinity in silicon germanium
η_F	-	reduced Fermi energy
$\Im_i$	-	Fermi-Dirac integral of order *i*
λ	-	natural length
C_{ox}	-	oxide capacitance
C_G^{QM}	-	quantum gate oxide capacitance
E_g	-	silicon bandgap
$E_{g,SiGe}$	-	silicon germanium bandgap
E_y	-	electric field
E_L	-	longitudinal electric field

ε_c	-	critical electric field
$f(E)$	-	Fermi-Dirac distribution
Ge	-	germanium
I_D	-	drain current (A)
I_{Dsat}	-	saturation drain current (A)
I_{on}	-	off current (A)
I_{off}	-	on current (A)
k_B	-	Boltzmann constant
L	-	channel length (nm)
m_0	-	electron mass
m^*	-	effective mass
n_i	-	intrinsic carrier density of silicon
N_A	-	channel doping density (cm^{-3})
N_D	-	source/drain doping density (cm^{-3})
N_{cd}	-	effective density of state in conduction band
q	-	charge (C)
r_j	-	junction depth (nm)
S	-	subthreshold slope (mV/dec)
Si	-	silicon
$SiGe$	-	Silicon Germanium
SiO_2	-	silicon dioxide
T	-	temperature (K)
T_{ox}	-	oxide thickness (nm)
T_{Si}	-	silicon thickness (nm)
V_{bi}	-	silicon build-in voltage (V)
$V_{bi,SiGe}$	-	silicon germanium build-in voltage (V)
V_c	-	critical voltage (V)
V_D	-	drain voltage (V)
V_{DS}	-	drain-to-source voltage
V_{Dsat}	-	saturation voltage
V_{fb}	-	flatband voltage (V)

η_d	-	carrier concentration
V_G	-	gate voltage (V)
V_{GS}	-	gate-to-source voltage (V)
V_{th}	-	threshold voltage (V)
V_{th}^{QM}	-	quantum threshold voltage (V)
V_{sub}	-	substrate voltage (V)
v_d	-	drift velocity
v_i	-	intrinsic velocity
v_{sat}	-	saturation velocity
v_{th}	-	thermal velocity
W	-	channel width (µm)

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CHAPTER 1

INTRODUCTION

1.1 Background

In the computing world, packing more transistors onto a chip leads to higher speeds. It may also give rise to more functions integrated within a system. According to the famous Moore's Law, the number of transistors it is possible to fit on an Integrated Circuit (IC) will double every 18 months, as the feature size of each transistor shrinks to half of its original size (Moore, 1975). Figure 1.1 shows that the numbers of transistors in Intel processor increased exponentially throughout the years from 1960 to 2010 (Gunther, 2007).

A wide variety of studies have been undertaken to develop techniques involving increasing the population of transistors on a single integrated circuit. This aim is realised through shrinking the transistors as well as increasing the number of transistors. Complementary Metal-Oxide-Semiconductor (CMOS) device scaling and miniaturization are some of the approaches used to design such devices and achieve Moore's Law. Furthermore, the microelectronic industry is scaling down in nanotechnology, in which the size of transistor decreases from the micrometre scale into nanometre scale.

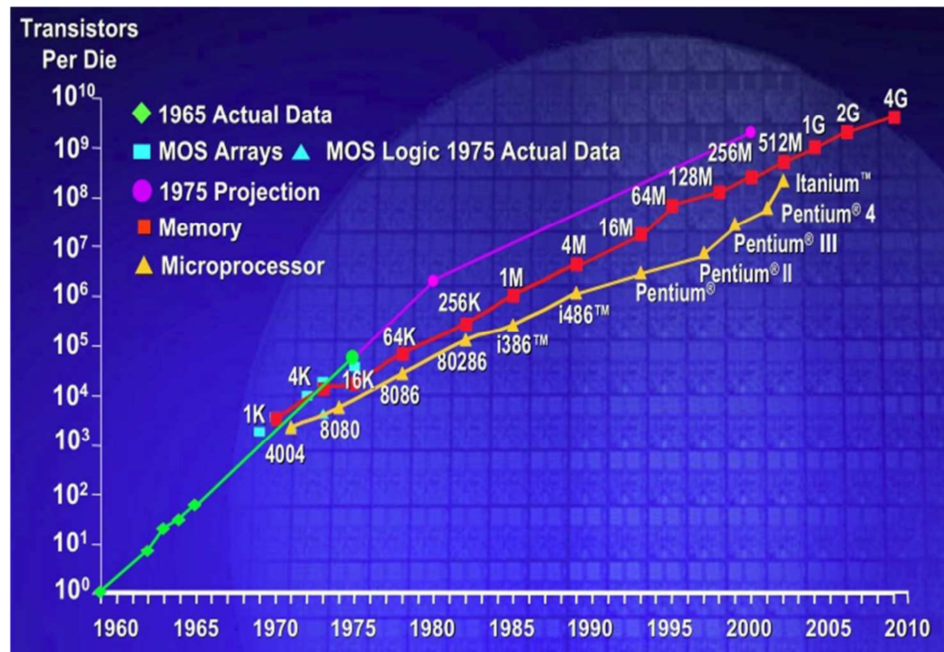

Figure 1.1: Exponential increase of the transistors in Intel processor per year according to Moore's Law (Gunther, 2007).

The challenge that engineers and scientists face is that the performance of silicon-made transistors will be affected when the transistor size enters the nanometre region, due to disturbances known as 'short channel effects'. Coupling these consequences with an increase in the cost of production will provide difficulties. In an effort to change the perspective of scaling down transistor size, scientists introduced new materials and new structures as alternatives for silicon-made gate channel CMOS, or introduced new CMOS architectures to replace common CMOS.

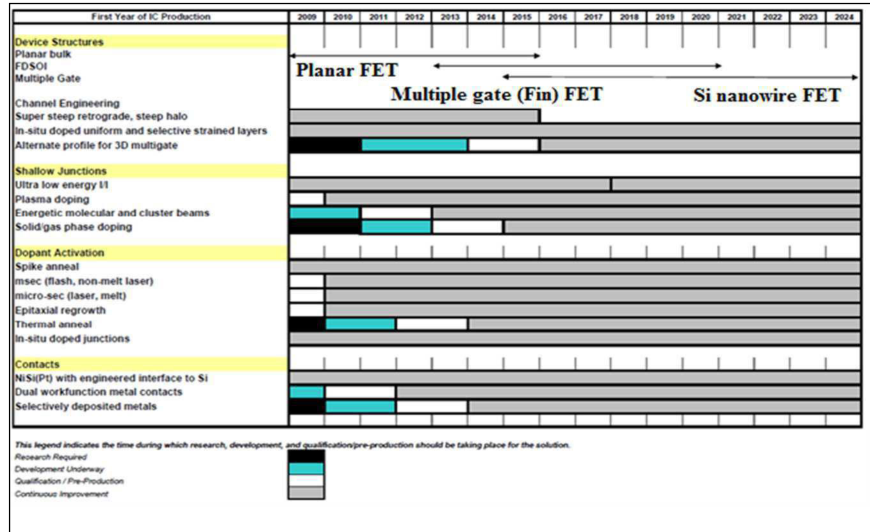

Figure 1.2: MOSFET structure trend (ITRS, 2011).

In this research, the use of new structure known as Silicon Nanowire Field-Effect Transistor (SiNWFET) is being explored. According to the International Technology Roadmap Semiconductor (ITRS) 2011, depicted in Figure 1.2, planar MOSFET are predicted to be obsolete and will be replaced by advanced MOSFET structures. The implementation of nanowire FET will be considered to replace existing FinFETs MOSFET structures that have the ability to reduce the short-channel effect (SCE) and have greater gate control (Iwai et al., 2011).

The introduction of new structures for nanotransistors is of utmost importance to overcoming downscaling problems. Nanowire transistors could keep Moore's Law alive by perfecting ways to produce Gate-All-Around Nanowire devices. Current research on the use of Gate-All-Around Nanowire Transistors in a new design is being explored, where the transistor channel is made up of an array of vertical nanowires. The gate surrounds all the nanowires, which improves its ability to control the flow of current as shown in Figure 1.3. In this research, the used of platinum-based source and drain contacts sits at the top and bottom of the nanowires (Hellemans, 2013).

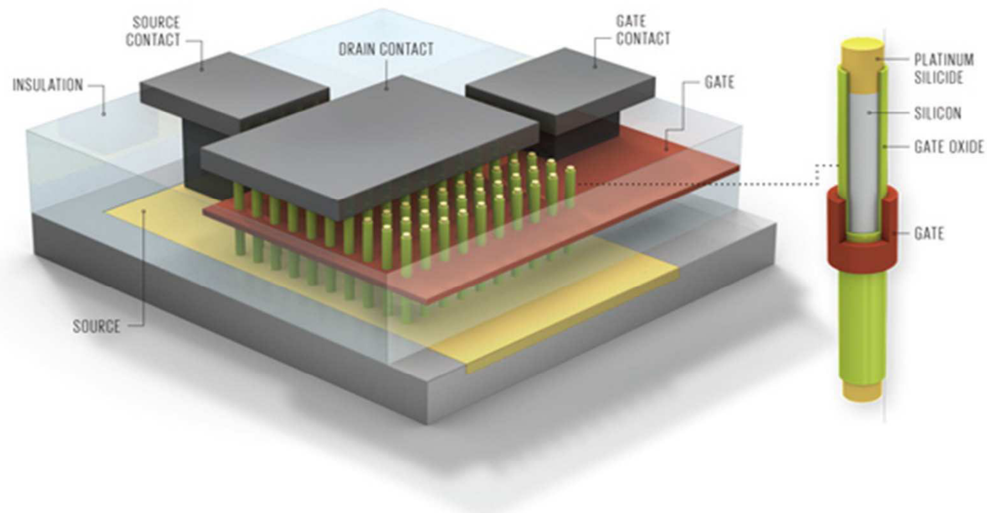

Figure 1.3: Gate-All-Around Nanowire Transistor Arrays (Hellemans, 2013).

Furthermore, the development of a compact model of the device is essential to examine the performance of the device on a circuit level, namely in a digital system. Device modeling plays a vital role in the characterization and application of SiNWFET. The ultimate goal of this thesis is to establish a comprehensive SiNWFET device model.

Following that, the performance of SiNWFET devices is predicted through simulation, and subsequently, the potential of SiNWFET in a digital system can be explored in terms of speed, power consumption, and feature size. In addition, device performance can be improved by using certain methods, which are shown in Table 1.1 (Wong, 2002). The challenges faced over channel scaling are physical limitations on gate oxide thickness, doping concentration, depletion and junction depth, as well as the increased complexity of fabrication for shorter dimension, as well as the presence of short channel effects (SCE). SCEs have caused the scaling of conventional MOSFET to become more difficult.

The short channel effect includes threshold voltage (V_T) reduction, increasing dissipation power (P_{disp}), higher leakage current (I_{OFF}) roll-off and larger drain induced barrier lowering (*DIBL*) (M. A. Riyadi *et al.*, 2009; M. A. Riyadi, Suseno, Napiah, Hamid, & Saad, 2010). Threshold reduction can reduce the operating voltage and power, however very low V_T is undesirable due to the exponentially higher leakage current and lower noise margin in logic applications (M. A. Riyadi et al., 2009; Saad, Riyadi, N, Hamid, & Ismail, 2010).

As the channel potential of the MOSFET is controlled by all terminals, scaling down the channel length (*L*) increases the drain bias influence on the channel's potential and electric field configuration that determines the device operation. The rise of drain controllability on the channel reduces the gate control on the channel current. These in turn intensify the SCEs, which may cause large off-currents through the DIBL effect. When the SCEs are dramatic, the drain can turn on the channel even when the gate is based in the off region.

Table 1.1: Device performances improvement opportunities (Wong, 2002).

Source of improvement	**Parameters affected**	**Methods**
Charge density	1. *S* (inverse subthreshold voltage) 2. Q_{inv} at a fixed off-current	1. Double-gate FET 2. Lower the operating temperature
Carrier transport	1. Mobility μ_{eff} 2. Carrier velocity 3. Ballistic transport	1. Strained silicon 2. High mobility and saturation velocity materials (Ge, lnGaAs, lnP) 3. Reduce mobility degradation factors (e.g. reduce transverse electric field, reduce Coulomb due to dopants, reduce phonon scattering) 4. A shorter channel length 5. Lower the operating temperature
Ensure device scalability to a shorter channel length	1. Generalized scale length (λ) 2. Channel length (L_g)	1. Maintain good electrostatic control of channel potential (e.g. double-gate FET, ground-plane FET, and ultra-thin body SOI) by controlling the device physical geometry and providing means to terminate drain electric fields 2. Sharp doping profiles, halo/pocket implants 3. High gate capacitance (thin gate dielectrics, metal gate electrode) to provide strong gate control of channel potential
Parasitic resistance	1. R_{ext}	1. Extended/Raised source/drain 2. Low-barrier Schottky contact
Parasitic capacitance	1. C_{jn} 2. C_{GD}, C_{GS}, C_{GB}	1. SOI - floating gate problem 2. Double-gate FET

1.2 Problem Statement

The downsizing of channel length in a planar MOSFET leads to several disadvantages, including short channel effects. Therefore, conventional device modeling is no longer accurate when the channel lengths reach the nanometer regime, due to the numerous unknown parameters. Figure 1.4 shows the transistor innovation starting from 130nm to 22nm technology nodes. In 130nm technology node, the gate oxide leakage is measurable at 4 nm, and grows 10x for every ~0.4 nm gate oxide reduction. This can lead to gate oxide leakage increase by gate oxide reduction. Following that, in 90nm technology node strains have been introduced, where strain is more beneficial to PMOS as it is able to improve mobility. Strain is benificial, but it doesn't solve the problem with gate oxide leakage. Next in 45nm node, where High-k/Metal were introduced to solve gate oxide leakage issues by reducing the effective oxide thickness and gate leakage at the same time by using high-k materials. However, Vt roll up is not stable, and lower performance (causing mobility degradation) and the threshold voltage roll-up is similar to the 65nm node.

In 22nm node technology, gate scaling crises are overcome by a new architecture called multiple gate, where the scaled devices are determined by body thickness (t_{si}) instead of depletion thickness, Xd. The challenge in MOSFET scaling can be overcome by introduction of new materials and new structures. In this research, the focus on is evaluating Silicon Nanowire (SiNW) in Gate-All-Around (GAA) configuration at the circuit level performance. In these architectures, scaling length includes T_{si} which can be varied independently from gate oxide thickness.

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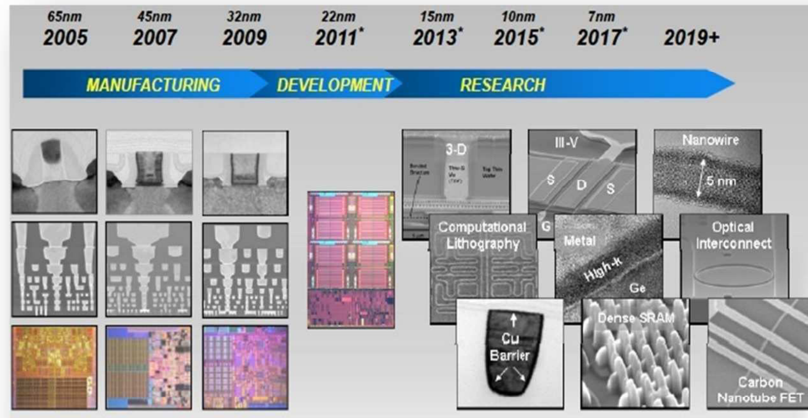

Figure 1.4 : The transistor research timeline in Intel starting from 2005 (Jakub Kedzierski, 2012)

Hence, in order to determine the efficiency of device performance at the circuit and logic gate level, it will be benchmarked with the nano-MOSFET, using conventional simulators such as SPICE. In addition, analytical expressions are required to obtain the Current-Voltage (I-V) of the device.

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1.3 Research Objectives

The research focuses on the analytical analysis of Gate-All-Around SiNWFET and its performance evaluation. The modeling approach will be used as the reference for the device optimization. Matrix Laboratory (MATLAB) is used as the main platform to optimize and analyze the SiNWFET while HSPICE software is utilized to evaluate the performance of the model to be benchmarked with nano-MOSFET. On the whole, the objectives of the research are:

a) To study and formulate an analytical and semi-empirical model of quasi-one-dimensional (Q1D) Silicon Nanowire FET (SiNWFET) structure.

b) To implement the unified-drain current SiNWFET I-V circuit model in a SPICE environment.

c) To evaluate the performance evaluation of SiNWFET logic gates and benchmark with nano-MOSFET in terms of Power Delay Product (PDP), Energy Delay Product (EDP) and propagation delay, t_p.

d) To investigate the performance of SiNWFET in terms of T_{ox}, R_{si}, N_d and L.

1.4 Research Scopes

The research begins with the development of a unified-drain current model of Silicon Nanowire Field-Effect Transistor (SiNWFET). In this stage, the I-V characteristics of SiNWFET are formulated by modeling approaches found in the literature. Next, the circuit configuration and logic gates of the inverter are implemented and other simple logic gate circuits and analytical analysis for device optimization. Software such as MATLAB, Statistical Package for the Social Sciences (SPSS) and HSPICE are used as platforms to establish the research. A literature review is carried out in order to understand the Quantum-1-Dimensional SiNWFET device physics, their limitations, as well as challenges faced in modeling and simulation.

1.5 Contributions

An established model of SiNWFET is presented, including 1D quantum confinement theory as well as a quasi-one-dimensional (Q1D) system which would be useful in evaluating the properties of the Q1D nanowire transistor. As a result, this model can be used to characterize future SiNWFET structures by development of unified-drain current model characteristics before implementation in HSPICE. The SiNWFET model can be simulated in HSPICE by using our very own UTM proprietary library, which may also be used by other researchers to compare their models. SiNWFET is shown to have better Power Delay Product (PDP), Energy Delay Product (EDP) and propagation delay, t_p, when benchmarked with nano-MOSFET.

1.6 Outline of Thesis

This research aims to evaluate the performance and optimization of the SiNWFET model, based on digital circuit design. Literature review on the basic theory of MOSFET and SiNWFETs devices, which provide a foundation to this research is presented in Chapter 2. Methodology will be presented in Chapter 3, in which research activities and expected outcomes are reported. The modeling aspects of Silicon Nanowire (SiNWFET), whilst a small portion of this chapter discusses the definition of non-degenerately and degenerately doped semiconductors, unified drain-current characteristics, and statistical analysis of SiNWFET in term of thickness oxide (T_{OX}), channel length (L) and diameter (D) of nanowire is discussed in Chapter 4. The circuitry and simulation of SiNWFET, it's performance evaluation, as well as drain induced barrier lowering (DIBL) and subthreshold slope (SS) effects in nanowire FET is explained in Chapter 5. Finally, the research works and future recommendation will be summarized in Chapter 6.

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