DESIGN AND MODELING OF ON-CHIP PLANAR CAPACITOR FOR RF APPLICATION

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To my lovely husband, Azrin Ariffin and my daughter, Lya Qistina Azrin

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ABSTRACT

On-chip radio frequency (RF) capacitor is one of the key components for RF integrated circuit (RFIC) designs such as filters and oscillators. Several researches on the design of on-chip planar capacitor have been reported. However there is a need to modify the existing synthesizing procedure; model and optimize the on-chip RF capacitor. Quality factor is the essential parameter as it is an index for the efficiency of a capacitor's performance. This thesis investigates the design of an interdigital capacitor configuration. Geometry design variables include number of fingers, finger length, finger width, finger gap, end gap, terminal width, strip thickness, substrate height, metal types and dielectric constant. The physical model of an interdigital capacitor was determined and its equivalent lumped circuit simulations have been performed. Then the optimum capacitance of the capacitor was determined. Several parameter variations on the interdigital capacitor were investigated. The effects of parameter variations on quality factor and capacitance value were discussed. An optimized interdigital capacitor can be obtained through their performance. The design has sufficient capacitance of 0.09338 pF, quality factor of 240 and operates in the 2 to 5 GHz range.

ABSTRAK

Kapasitor frekuensi radio (RF) adalah satu daripada komponen utama rekabentuk litar bersepadu RF (RFIC) seperti penapis dan pengayun. Beberapa kajian berkaitan rekabentuk kapasitor sesatah atas cip telah dilaporkan. Walau bagaimanapun, terdapat keperluan untuk mengubah prosedur sintesis; permodelan dan pengoptimuman kapasitor RF atas cip. Faktor kualiti adalah parameter penting sebagai indeks kecekapan pretasi pemuat. Tesis ini mengkaji rekabentuk/konfigurasi kapasitor interdigital. Pembolehubah rekabentuk geometri meliputi bilangan jari, panjang jari, lebar jari, sela jari, hujung sela, lebar terminal, ketebalan jalur, ketebalan substratum, jenis logam dan pemalar dielektrik. Model fizikal kapasitor interdigital telah diperolehi dan simulasi litar tergumpal setara telah dilakukan. Kemudian, kapasitan optimum bagi kapasitor ini telah diperolehi. Beberapa variasi parameter terhadap kapasitor telah dikaji. Kesan variasi ini terhadap faktor kualiti dan kapasitan juga dikaji. Kapasitor interdigital yang optimum dihasilkan. Rekabentuk ini mempunyai cukup kapasitan bernilai 0.09338 pF, faktor kualiti bernilai 240 dan berkendali dalam julat 2 hingga 5 GHz.

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LIST OF ABBREVIATIONS

ABS	:	Adaptive Band Synthesis
AL	:	ALUMINUM
Bi-CMOS	:	Bipolar Complementary Metal Oxide Silicon
C	:	Capacitor
CAD	:	Computer-aided design
Cu	:	Copper
CMOS	:	Complementary Metal Oxide Silicon
dB	:	Decibel
DC	:	Direct Current
DUT	:	Device under test
ESR	:	Equivalent series resistance
EM	:	Electromagnetic simulation
F	:	Farad
FFT	:	Fast Fourier Transform
GaAs	:	Gallium Arsenide
GHz	:	Giga-hertz
GND	;	Ground
H	:	Henry
HF	:	High frequency
Hz	:	Hertz
IC	:	Integrated circuit
IDC	:	Interdigital capacitor

Im	:	Imaginary
KHz	:	Kilo-hertz
L	:	Inductor
nH	:	nano Henry
Max	:	Maximum
MHz	:	Mega-hertz
MIC	:	Microwave integrated circuit
MIM	:	Metal insulator metal
Min	:	Minimum
MMIC	:	Monolithic microwave integrated circuit
MOS	:	Metal-oxide-semiconductor
MOSFET	:	Metal-oxide-semiconductor-field effect-transistor
PIP	:	Poly-insulator-poly
PF	:	pico Farad
R	:	Resistor
Re	:	Real
RF	:	Radio frequency
RFIC	:	Radio frequency integrated circuit
SI	:	Standard International
Si	:	Silicon
SiO_2	:	Silicon oxide
Si_3N_4	:	Silicon Nitride
S-parameter	:	Scattering parameter
SPICE	:	General purpose circuit simulation program
SRF	:	Self-resonant frequency
TEM	:	Transverse electromagnetic
Vs.	:	Versus
WBIDC	:	Wire bonded interdigital capacitor
2D	:	Two dimension
3D	:	Three dimension

LIST OF SYMBOLS

A	:	Plate area
A_1	:	Interior capacitance of the finger
A_2	:	Two exterior capacitance of the finger
C	:	Capacitance
C_{eff}	:	Effective capacitance
C_g	:	Static capacitance
C_p	:	Parallel capacitance
C_{p1}	:	The equivalent capacitances of gap discontinuous (port 1)
C_{p2}	:	The equivalent capacitances of gap discontinuous (port 2)
C_{TE}	:	Even mode capacitance
C_{TO}	:	Odd mode capacitance
C_p	:	Parallel capacitance
C1	:	Parasitic capacitance
C2	:	Parasitic capacitance
d	:	Separation between the plates
E	:	Electric field
f	:	Frequency
G	:	Conductance
g_e	:	Finger end gap
h	:	Substrate height
I	:	Electric current
L	:	Inductance

l	:	Finger length
l_T	:	Length of terminal strip
L_{TE}	:	Even mode inductance
L_{TO}	:	Odd mode inductance
n	:	Number of fingers
P#	:	Port number
Q	:	Quality factor
Qc	:	Quality factor due to conductor losses
Qd	:	Quality factor due to dielectric losses
Q_{max}	:	Maximum quality factor
q_{1total}	:	Total charge on the inner conductor (port 1)
q_{2total}	:	Total charge on the inner conductor (port 2)
$q_{1'}$	:	Charge per unit length on the connected transmission lines (port1)
$q_{2'}$	:	Charge per unit length on the connected transmission lines (port2)
R	:	Resistance
R_{DC}	:	DC resistance
R_{RF}	:	Skin effect coefficient
R_s	:	Series resistance
R_T	:	Resistance of the conductors
s	:	Finger spacing
S_{11}	:	Input reflection coefficients
S_{12}	:	Reverse transmission coefficients
S_{21}	:	Forward transmission coefficients
S_{22}	:	Output reflection coefficients
t	:	Strip thickness
V_{in}	:	Input voltage
V_o	:	Peak voltage across the circuit terminal
V_{out}	:	Output voltage
w_t	:	Terminal width

x	:	Finger width
Y_{11}	:	Admittance seen looking into port 1 when port 2 is short-circuit
Y_{12}	:	Transfer admittance when port 1 is short-circuit
Y_{21}	:	Transfer admittance when port 2 is short-circuit
Y_{22}	:	Admittance seen looking into port 2 when port 1 is short-circuit
Z_{in}	:	Input impedance
Z_c	:	Characteristic impedance for series configuration
Z_s	:	Characteristic impedance for shunt configuration
Z_{oo}	:	Even mode impedance
Z_{oe}	:	Odd mode impedance
Z_T	:	Characteristic impedance
Z_{11}	:	Impedance at 1 when port 2 is open
Z_{12}	:	Transition impedance when port 1 is short-circuit
Z_{21}	:	Transition impedance when port 2 is short-circuit
Z_{22}	:	Impedance at 2 when port 1 is open
α_χ	:	Attenuation constant for series configuration
α_σ	:	Attenuation constant for shunt configuration
)	:	Metal resistivity at DC
δ	:	Metal skin depth
μ	:	Permeability
μ_0	:	Free space permeability
μ_r	:	Relative magnetic permeability
ε	:	Real part of dielectric permittivity
ε_c	:	Relative dielectric constant for series configuration
ε_r	:	Relative dielectric constant
ε_o	:	Free space dielectric constant
ε_s	:	Relative dielectric constant for shunt configuration
γ_{TE}	:	Even mode propagation constant
γ_{TO}	:	Odd mode propagation constant
μm	:	Micron meter

η_o	:	Free space impedance
Ω	:	Unit of resistivity, ohm
ω	:	ω radian frequency, rad/s
ϕ	:	Magnetic flux
σ	:	Bulk conductivity
π	:	22/7
λ	:	Unit of wavelength

LIST OF APPRENDICES

Chapter 1

Introduction

Advances in Complementary Metal Oxide Silicon (CMOS) fabrications have resulted in deep submicron transistors with higher transit frequencies and lower noise figure [17]. This advanced performance of Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) is attractive for high-frequency (HF) circuit design in view of a system on-chip realization, where digital, mixed-signal base-band and HF transceiver blocks would be integrated on a single chip. Besides the ability to integrate RF circuit with other analog and logic circuit with the intention of reducing the cost by eliminating the sometimes-expensive packaging, other advantages offered by silicon CMOS technologies are low cost due to the volume of wafers processed and the low power consumption, which makes it suitable for portable applications.

Many research activities are studying the possibilities to migrate the RF circuit to CMOS technology. The on-chip planar capacitor is one of the major areas of such investigation.

1.1 Objective

The objective of this research is to model and design an optimized RF interdigital capacitor for Radio Frequency Integrated Circuit (RFIC) application.

1.2 Scope

The scopes of the research are as follows:

- Determination of the physical model of an interdigital capacitor and its equivalent lumped circuit
- Usage of MathCAD software for mathematical configuration
- Determine the optimum capacitance of the capacitor
- Simulation of the physical layout of the capacitor using SONNET simulation software
- Analyzing the performance of the designed interdigital capacitor
- Thesis writing

The design specification is as follows:

- Quality factor Q : 240 to 250
- Capacitance C : 0.08 to 0.2 pF
- Operating frequency f : 2 to 5 GHz

Figure 1.1 shows as example of the design geometry.

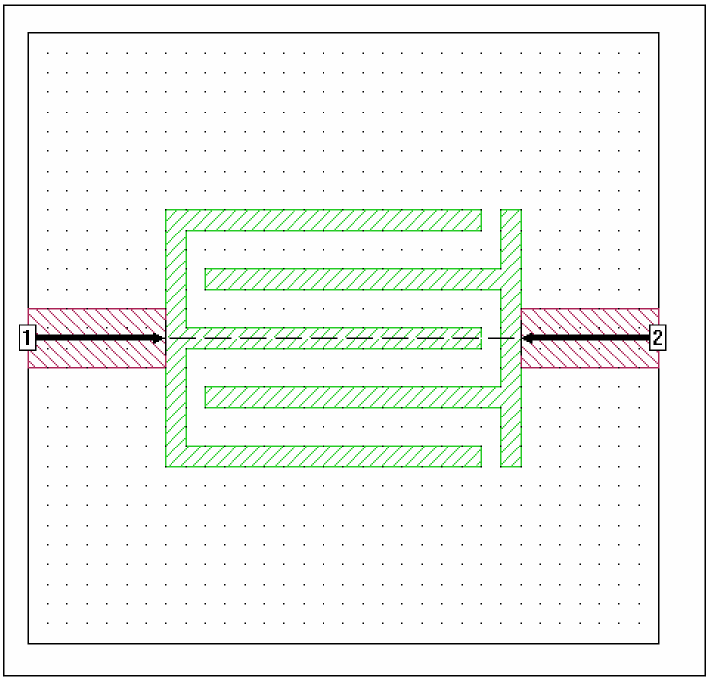


Figure 1.1 An interdigital capacitor geometry

1.3 Problem Statement

In CMOS applications, RFICs are developing a strong presence in the commercial world. The advantages of RF CMOS technology are low cost, low power consumption, small in size, high integration, high reliability and high volume production. However, it has been found that the greatest obstacle for achieving high quality RF system with CMOS technology comes from the passive components. The reliability and the efficiency of CMOS RF system can be improved by realizing on-chip RF passive component, such as on-chip capacitor. Hence, there is need to design and model an optimized on-chip capacitor fabricated on Silicon substrates.

1.4 Project Background

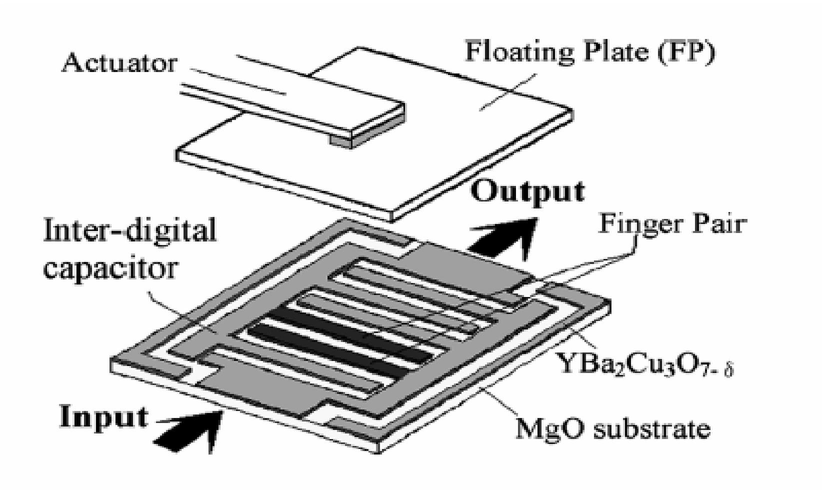
This project investigates the design of an interdigital capacitor. Geometry design variables include number of fingers (n), finger length (l), finger width (x), finger gap (s), end gap (g_e), terminal width (w_t), strip thickness (t), substrate height (h), metal types and dielectric constant. The optimum design of an interdigital capacitor can be identified through contour plot of the quality factor (Q-factor). This project involves mathematical computation using MathCad and electromagnetic simulation using SonnetLite Plus. This optimum design of an interdigital capacitor can be used for RF applications such as filter and oscillator. Microstrip interdigital capacitors (IDCs) have been widely used as a quasi-lumped element in high frequency and high-speed integrated circuits (ICs). [8]

Capacitors have become ubiquitous in analog-integrated circuits particularly owing to the switched capacitor technique for realization of analog-to-digital and digital-to-analog data converters and discrete time filters.

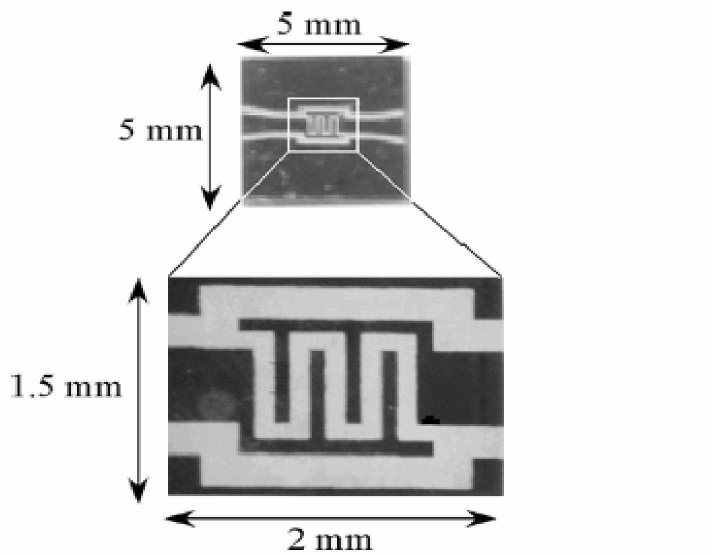
1.5 Application of Interdigital Capacitor in RFIC

Capacitors are one of the most crucial elements in mixed-signal integrated circuits. These are used extensively in many RFIC applications such as RF oscillator, filter, mixer, data converters, sample and holds and switched capacitor circuits.

Figure 1.2 and Figure 1.3 shows a mechanically tunable superconducting microwave filter based on interdigital capacitor an interdigital capacitor bandpass filter, respectively.

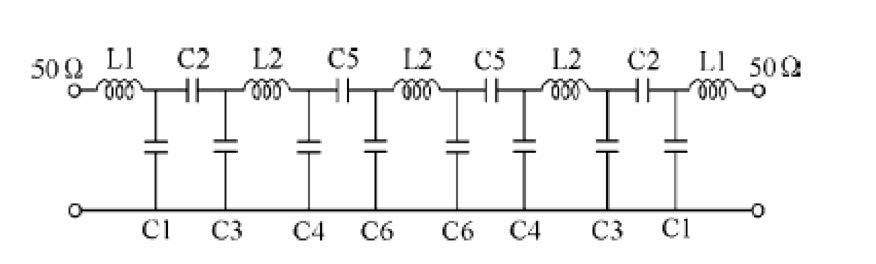


(a)

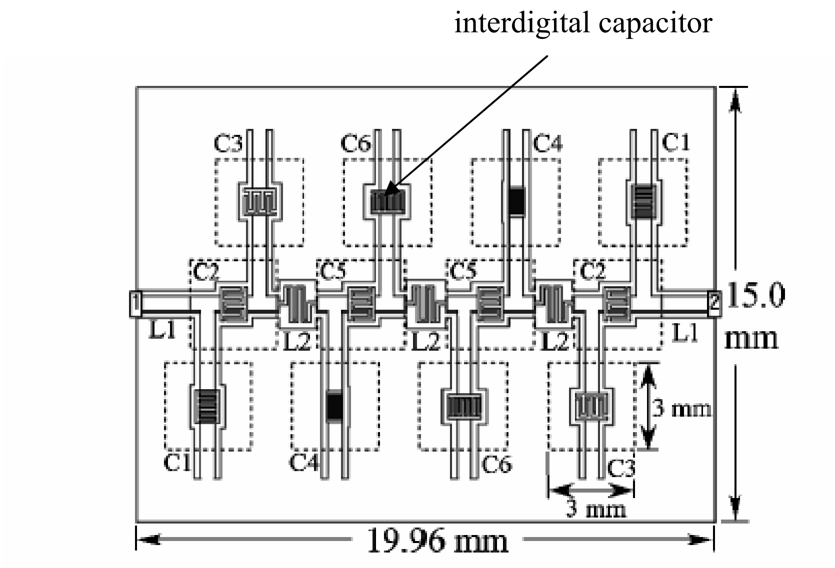


(b)

Figure 1.2 A mechanically tunable superconducting microwave filter based on interdigital capacitor: (a) the view showing a frame format of a mechanical tuning method on interdigital capacitor, (b) photograph of the pre-production interdigital capacitor [11].



(a)



(b)

Figure 1.3 3 poles Chebyshev band pass filter of center frequency 6 GHz: (a) an equivalent circuit structure, (b) layout of the lumped elements band pass filter [11].

1.6 Thesis Organization

Chapter 1 presents the introduction of this project report which includes objective, scope, project background and application of interdigital capacitor in RFIC. Chapter 2 presents the literature review on the characterization of capacitor, types of capacitor and on-chip interdigital capacitor. Chapter 3 is mainly focused on the physical modeling of an interdigital capacitor. It includes the derivation of the equations of capacitance and equation of Q factor. The calculation flow using MathCad software is also been discussed in this chapter. Chapter 4 presents the design procedures of using the electromagnetic simulator and some design loss issues such as metallization and dielectric losses. Chapter 5 is mainly focused on the analysis of results and discussion. The results are presented into two parts. The first part is the mathematical computations using MathCad software while the second part is the electromagnetic simulation result using SonnetLite Plus. The effect on Q factor and capacitance over different designs, varying number of fingers, types of metals and finger lengths are presented and discussed. Chapter 6 concludes the thesis. Also presented in this chapter are recommendations for future work.

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