DESIGN AND IMPLEMENTATION OF OFDM TRANSMITTER AND RECEIVER ON FPGA HARDWARE

KAMARU ADZHA BIN KADIRAN

UNIVERSITI TEKNOLOGI MALAYSIA

DESIGN AND IMPLEMENTATION OF OFDM TRANSMITTER AND RECEIVER ON FPGA HARDWARE

KAMARU ADZHA BIN KADIRAN

A project report submitted in partial fulfillment of the
requirement for the award of the degree of
Master of Electrical Engineering (Electronics and Telecommunication)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

NOVEMBER, 2005

Special dedicated to

My Loving Family,
Father, Beloved Brothers,
All my friends and relatives,
And all my teachers and lecturers,
for the support and care.

ACKNOWLEDGEMENT

Praise to Allah S.W.T the Most Gracious, the Most Merciful, whose blessing and guidance have helped me through my thesis smoothly. There is no power no strength save in Allah, the Highest and the Greatest. Peace and blessing of Allah be upon our Prophet Muhammad S.A.W who has given light to mankind.

I would like to take this opportunity to express my deepest gratitude to my supervisor, Prof. Dr. Norsheila Bt Fisal for his guidance, help and encouragement throughout the period of completing my project.

I would like to thank to Mr Illyassak for all the help and guidance especially in using Apex development board and configuration of the related software.

I also would like to thank to Mr. Muladi for his kind assistant and advice in explaining the theory and concept of OFDM system.

I sincerely thank to all my friends and all those whoever has helped me either directly or indirectly in the completion of my final year project and thesis.

ABSTRACT

Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier modulation technique which divides the available spectrum into many carriers. OFDM uses the spectrum efficiently compared to FDMA by spacing the channels much closer together and making all carriers orthogonal to one another to prevent interference between the closely spaced carriers. The main advantage of OFDM is their robustness to channel fading in wireless environment. The objective of this project is to design and implement a base band OFDM transmitter and receiver on FPGA hardware. This project concentrates on developing Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT). The work also includes in designing a mapping module, serial to parallel and parallel to serial converter module. The design uses 8-point FFT and IFFT for the processing module which indicate that the processing block contain 8 inputs data. All modules are designed using VHDL programming language and implement using Apex 20KE board. The board is connected to computer through serial port and Nios development kit software is used to provide interface between user and the hardware. All processing is executed in Apex board and user only requires to give the inputs data to the hardware throughout Nios. Input and output data is displayed to computer and the results is compared using Matlab software. Software and tools which used in this project includes VHDLmg Design Entry, Synopsys FPGA Express, Altera Maxplus+II and Altera Quartus 3.0. Software tools are used to assist the design process and downloading process into FPGA board while Apex board is used to execute the designed module.

ABSTRAK

Orthogonal Frequency Division Multiplexing (OFDM) adalah salah satu teknik pemodulatan multi-pembawa yang membahagikan satu spektrum frekuensi kepada banyak spektrum pembawa. OFDM menggunakan spektrum dengan lebih effisien berbanding FDMA. OFDM meletakkan saluran berdekatan antara satu sama lain dengan membuatkan setiap pembawa orthogonal dengan yang lain untuk mengelakkan gangguan antara pembawa. Kelebihan OFDM adalah kekuatan signalnya terhadap masalah *channel fading* di dalam persekitaran wireless. Objektif projek ini adalah untuk mereka dan melaksanakan pemancar dan penerima base band OFDM dengan menggunakan perkakasan FPGA. Projek ini menumpukan dalam pembinaan modul *Fast Fourier Transform (FFT)* dan *Inverse Fast Fourier Transform (IFFT*). Selain itu, kerja-kerja merekabentuk modul untuk *mapping*, pengubah sesiri ke selari dan selari ke sesiri juga termasuk dalam skop projek. Semua modul direkabentuk menggunakan bahasa pengaturcaraan VHDL dan dilaksana menggunakan litar Apex 20KE. Litar ini akan disambungkan kepada komputer melalui liang sesiri dan kit perisian Nios digunapakai untuk menyediakan antaramuka kepada pengguna dan perkakasan. Kesemua pemprosessan dilaksanakan oleh litar Apex 20KE yang mana pengguna hanya perlu menmberikan input kepada peranti tersebut. Masukan dan keluaran data akan dipapar melalui skrin komputer dan hasil keputusan akan dibanding dengan perisian Matlab. Antara perisian-perisian yang digunapakai adalah *VHDLmg Design entry, Synopsys FPGA Express, Altera Max+Plus II* dan *Altera Quartus II 3.0*. Perisian yang digunapakai adalah untuk membantu dalam proses merekabentuk modul dan memuat turun program ke dalam peranti manakala litar Apex digunapakai untuk melaksanakan operasi.

TABLE OF CONTENTS

CHAPTER	TITLE	PAGE
	THESIS TITLE	i
	DECLARATION	ii
	DEDICATION	iii
	ACKNOWLEDGMENT	iv
	ABSTRACT	v
	ABSTRAK	vi
	TABLE OF CONTENTS	vii
	LIST OF TABLE	x
	LIST OF FIGURES	xi
	LIST OF APPENDICES	xiv
CHAPTER I	**INTRODUCTION**	
	1.1 Introduction	1
	1.2 Project Background	3
	1.3 Project Objectives	4
	1.4 Project Scope	5
	1.5 Project Outline	6
CHAPTER II	**LITERATURE REVIEW**	
	2.1 Introduction	8
	2.2 Literature Review	8
	2.3 Basic Principles of OFDM	9
	2.4 Orthogonality Defined	10
	2.5 OFDM Carriers	11

	2.6	Generation of OFDM Signals	12
	2.7	Guard Period	14
	2.8	Advantages of OFDM	15
	2.9	The weakness of OFDM	18
	2.10	Applications of OFDM	19
CHAPTER III	**METHODOLOGY**		
	3.1	Introduction	22
	3.2	Study Relevant Topic	23
	3.3	Design Process	24
	3.4	Implementation	25
	3.5	Test and Analysis	25
	3.6	VHDL and VHDLmg Software	25
	3.7	Synopsys FPGA Express Software	27
	3.8	Altera Max+Plus II software	27
	3.9	Matlab	28
	3.10	Apex 20KE Device Board	28
	3.11	Quartus II 3.0	29
CHAPTER IV	**HARDWARE DESIGN**		
	4.1	Introduction	30
	4.2	Simplified Transmitter Block Diagram	31
	4.3	Simplified Receiver Block Diagram	32
	4.4	Mapping Module	32
	4.5	Serial to Parallel Module	33
	4.6	Parallel to Serial Module	34
	4.7	Fast Fourier Transform (FFT)	36
		4.6.1 FFT signal flow graph	39
		4.6.2 FFT scheduling diagram	41
	4.8	Inverse Fast Fourier Transform (IFFT)	43
	4.9	Hardware Module	46
		4.9.1 Fast Fourier Transform	46
		4.9.2 Inverse Fast Fourier Transform	47

4.9.3 Hardware Interfacing 47

CHAPTER V SOFTWARE DESIGN

5.1 Introduction 49
5.2 Hardware Programming 50
5.2.1 Adding user defined logic 50
5.2.2 Setting module properties 51
5.2.3 Complete module integration 52
5.2.4 Generating the files 53
5.2.5 Compiling the system module 54
5.2.6 Download the design into FPGA 55
5.3 Software Design 56
5.3.1 Compiling and downloading control vector program 57

CHAPTER VI RESULTS

6.1 Introduction 62
6.2 How to Conduct Test? 64
6.3 Results obtained for IFFT 66
6.4 Results obtained for FFT 68
6.5 Results obtained for Transmitter and Receiver 71

CHAPTER VII ANALYSIS AND DISCUSSION

7.1 Introduction 79
7.2 Why not Accurate 80
7.3 Multiplication of Twiddle Factor 80
7.4 Division by eight in IFFT module 87
7.5 Overflow 82

CHAPTER VIII CONCLUSION

8.1 Conclusion 83
8.2 Proposed Future Works 84
REFERENCES 86

APPENDICES

APPENDICES A	88
APPENDICES B	89
APPENDICES C	91
APPENDICES D	92
APPENDICES E	95
APPENDICES F	98
APPENDICES G	106
APPENDICES H	117

LIST OF TABLES

NO	TITLE	PAGE
4.0	Twiddle factor value for 8 point FFT	37
4.1	Twiddle factor value for 8 point IFFT	43
4.3	Frequently command used in Linux	38
5.1	Memory address 1	57
5.2	Memory address 2	58
5.3	Memory address 3	58
6.1	Results for FFT	76
6.2	Results for IFFT	77
6.3	Results for Transmitter and receiver	78

LIST OF FIGURES

NO	TITLE	PAGE
2.0	Orthogonality of sub-carriers	11
2.1	OFDM subcarrier in the frequency domain	12
2.2	Binary Phase Shift Key (BPSK) representation	13
2.3	A set of orthogonal signal	13
2.4	Block diagram for OFDM communication	14
2.5	Implementation of cyclic prefix	15
2.6	Two ways to transmit the same four pieces of binary data	17
2.7	Show amplitude varying in OFDM	18
3.1	Flow chart of the projects methodology	23
3.2	Basic modeling structure for VHDL	26
3.3	Show the VHDL design entity	26
4.1	Simplified transmitter block diagram	31
4.2	Simplified receiver block diagram	32
4.3	Mapping module	32
4.4	Block diagram for serial to parallel module	33
4.5	Simulation waveform of the serial to parallel module.	34
4.6	Block diagram for parallel to serial module	34
4.7	Simulation waveform of the parallel to serial module	35
4.8	8 point FFT flow graph using DIF	39
4.9	Scheduling diagram for stage one of 8 point FFT	41
4.10	Scheduling diagram for stage two of 8 point FFT	42
4.11	Scheduling diagram for stage three of 8 point FFT	42
4.12	Scheduling diagram for stage one of 8 point IFFT	44

4.13	Scheduling diagram for stage two of 8 point IFFT	45
4.14	Scheduling diagram for stage three of 8 point IFFT	45
4.15	FFT module	46
4.16	Block diagram of the connection between IFFT/FFT module with Avalon bus system	47
5.1	Interface to the user logic setting on port tab	51
5.2	Interface to the user logic setting on timing tab	52
5.3	SOPC builder with modules	55
5.4	Generate the appropriate files for each module	54
5.5	Compiling the system module	55
5.6	Download the design into development board	55
5.7	The SOPC Builder system contents page	56
5.8	The portion of address mapping in Excalibr.h file generated by SOPC builder	57
5.9	The simplified block diagram of connection between ALU with Avalon bus system	59
5.10	Compiling the C code for test vector program	60
5.11	Downloading C code for test vector program	60
6.1	Apex 20KE development board	63
6.2	Apex 20KE connection with computer	63
6.3	(a) Matlab FFT/IFFT module (b) Apex 20KE FFT/IFFT module	64
6.4	Transmitter module and receiver module	65
6.5	Input value to the IFFT module	66
6.6	Stage 1 and stage 2 operation	67
6.7	Stage 3 and stage 4 operation	67
6.8	The final output from IFFT operation	68
6.9	Input value to FFT module	68
6.10	Stage 1 to stage 2 operation	69
6.11	Stage 3 to stage 5 operation	70
6.12	Stage 6 and final output of IFFT computation	70
6.13	Input to transmitter	71
6.14	Transmitter processing stage 1 to 2	72

6.15	Transmitter processing stage 3 to 4	72
6.16	Output for transmitter module	73
6.17	Receiver buffer	73
6.18	Receiver operation for stage 1 to 2	74
6.19	Receiver operation for stage 3 to 5	74
6.20	Receiver operation for stage 6 and the dinal output for receiver	75
7.1	Example of twiddle factor multiplication	80
7.2	Example of the twiddle factor divisions	81
7.3	Addition of decimal number	82

LIST OF APPENDICES

APPENDICES	TITLE	PAGE
A	VHDL code for Mapper	88
B	VHDL code for serial to parallel	89
C	VHDL code for parallel to serial	91
D	VHDL code for IFFT and interface module	92
E	VHDL code for FFT and interface module	95
F	Test vector program for IFFT module in C	98

CHAPTER I

INTRODUCTION

1.1 Introduction

This chapter covers the material on project background, project objectives, project scope and the thesis outline. Introduction on this chapter covers about the OFDM implementation method and description on the available hardware for implementation. The problem statement of the project will also be carried out in this chapter.

With the rapid growth of digital communication in recent years, the need for high-speed data transmission has been increased. The mobile telecommunications industry faces the problem of providing the technology that be able to support a variety of services ranging from voice communication with a bit rate of a few kbps to wireless multimedia in which bit rate up to 2 Mbps. Many systems have been proposed and OFDM system has gained much attention for different reasons. Although OFDM was first developed in the 1960s, only in recent years, it has been recognized as an outstanding method for high-speed cellular data communication where its implementation relies on very high-speed digital signal processing. This method has only recently become available with reasonable prices versus performance of hardware implementation.

Since OFDM is carried out in the digital domain, there are several methods to implement the system. One of the methods to implement the system is using ASIC (Application Specific Integrated Circuit). ASICs are the fastest, smallest, and lowest power way to implement OFDM into hardware. The main problem using this method is inflexibility of design process involved and the longer time to market period for the designed chip.

Another method that can be used to implement OFDM is general purpose Microprocessor or Micro Controller. Power PC 7400 and DSP Processor is an example of microprocessor that is capable to implement fast vector operations. This processor is highly programmable and flexible in term of changing the OFDM design into the system. The disadvantages of using this hardware are, it needs memory and other peripheral chips to support the operation. Beside that, it uses the most power usage and memory space, and would be the slowest in term of time to produce the output compared to other hardware.

Field-Programmable Gate Array (FPGA) is an example of VLSI circuit which consists of a “sea of NAND gates” whereby the function are customer provided in a “wire list”. This hardware is programmable and the designer has full control over the actual design implementation without the need (and delay) for any physical IC fabrication facility. An FPGA combines the speed, power, and density attributes of an ASIC with the programmability of a general purpose processor will give advantages to the OFDM system. An FPGA could be reprogrammed for new functions by a base station to meet future needs particularly when new design is going to fabricate into chip. This will be the best choice for OFDM implementation since it gives flexibility to the program design besides the low cost hardware component compared to others.

1.2 Project Background

This project is the continuation from the previous master student project which entitled “Design of an OFDM Transmitter and Receiver Using FPGA” by Loo Kah Cheng. The works involved from previous student is focused on the design of the core processing block using 8 point Fast Fourier Transform (FFT) for receiver and 8 point Inverse Fast Fourier Transform (IFFT) for transmitter part. The implementation of this design into FPGA hardware is to no avail for several reasons encountered during the integration process from software into FPGA hardware.

The project was done up to simulation level using Max+Plus II software and only consists FFT and IFFT processing module. Some of the problem encountered by this student is that the design of FFT and IFFT is not fit to FPGA hardware. The design used a large number of gates and causes this problem to arise. Logic gates are greatly consumed if the number of multiplier and divider are increase. One method to overcome this problem is by decreasing the number of multiplier and divider in the VHDL design.

Beside that, the design does not include control signal which cause difficulties in controlling the data processing in FFT or IFFT module. The control signal is use to select the process executed for each computation process during VHDL design. As a result, the design is not applicable for hardware implementation in the FPGA development board. New design is required to overcome this problem. Since the design is not possible to use, this project will concentrate on designing the FFT and IFFT module which can be implement in the dedicated FPGA board. To ensure that the program can be implemented, the number of gates used in the design must be small or at least less than the hardware can support. Otherwise the design module is not able to implement into the dedicated bord.

1.3 Project Objective

The aim for this project is to design a baseband OFDM processing including FFT (Fast Fourier Transform) and IFFT (Inverse Fast Fourier Transform), mapping (modulator), serial to parallel and parallel to serial converter using hardware programming language (VHDL). These designs were developed using VHDL programming language in design entry software.

The design is then implemented in the Apex 20k200EFC484-2X FPGA development board. Description on the development board will be carried out at methodology chapter.

In order to implement IFFT computation in the FPGA hardware, the knowledge on Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) programming is required. This is because FPGA chip is programmed using VHDL language where the core block diagram of the OFDM transmitter implements in this hardware. The transmitter and receiver are developed in one FPGA board, thus required both IFFT and FFT algorithm implemented in the system.

Several tool involved in the process of completing the design in real hardware which can be divided into two categories, software tools and hardware tool. The software which include in this project is using CAD tools software, VHDL module generator v.109, Synopsis FPGA Express v3.31.4719 and Altera Max+plus II. While the hardware use is UP1 board of ALTERA Flex 10K FPGA chip.

1.4 Project Scope

The work of the project will be focused on the design of the processing block which is 8 point IFFT and FFT function. The design also includes mapping block, serial to parallel and parallel to serial block set. All design need to be verified to ensure that no error in VHDL programming before being simulated. Design process will be described on the methodology chapter.

The second scope is to implement the design into FPGA hardware development board. This process is implemented if all designs are correctly verified and simulated using particular software. Implementation includes hardware programming on FPGA or downloading hardware design into FPGA and software programming.

Creating test vector program also include in the scope of the project. Test vector is a program developed using c programming and is intended as the input interface for user as well as to control data processing performed by the hardware. Creating this software required in understanding the operation of the FFT and IFFT computation process. Further chapter will discuss the method on developing the program from mathematical algorithm into behavioral synthesis.

The last works is to verify the result of the output for each module which has been developed. Test vector program is used to deliver the computation result if input value is provided by the user. These computation values should be verified and tested to ensure the correctness of the developed module. Appropriate software is used to compare the computation performed by the FPGA hardware with the software. There are several test performed to the design modules and the test process also will be discuss in the methodology chapter.

1.5 Project Outline.

The project is organized into six chapters, namely introduction, literature review, methodology, hardware design, software design, result, analysis and discussion, and conclusion.

Chapter 1 discusses the general idea of the project which covers the introduction, project objective, project background and scope of the project.

Chapter 2 shows the literature review of the OFDM system, basic principles of OFDM system, advantages and disadvantages of OFDM system, and lastly is the application of the OFDM in recent technology.

Chapter 3 describes the methodology of the project. The project is divided into several stages which basically include study relevant topics, design stage, implementation stage and testing stage. Further description will cover in this chapter.

Chapter 4 explains regarding the hardware design which is developed from mathematical equations. The chapter also includes on the theoretical part of FFT and IFFT and describes until the hardware design.

Chapter 5 enlightens the software design process involved in the project. This part basically discussed on the works involved to download the modules into FPGA board. Besides that, development of test vector which is used to test the modules will be carried out in this chapter.

Chapter 6 shows the results obtained from the FPGA hardware. The results obtained are captured and show in the figure as an examples. Further results will be shown in the tables.

Chapter 7 describes on the analysis and discussion of the result. Some results which gives error output will be discussed in this chapter and provide the reason behind the problem occurred.

Chapter 8 consists of the conclusion and proposed works to enhance the project in the future.

REFERENCES

1. Dusan Matiae, “OFDM as a possible modulation technique for multimedia applications in the range of mm waves”, TUD-TVS, 1998.
2. R.W Chang, “Synthesis of Band limited Orthogonal Signals for Multichannel Data Transmission”, Bell System Tech. J., pp.1775-1776, Dec 1996.
3. B. R. Saltzberg, “Performance of an Efficient Parallel DataTransmission System”, IEEE Trans. Comm., pp. 805-811, Dec 1967.
4. S. B Weinstein and P.M. Ebert, “Data Transmission by Frequency Division Multiplexing Using the Discrete Fourier Transform”, IEEE Transactions on Communication Technology”, Vol. COM-19, pp. 628-634, October 1971.
5. A. Peled an A. Ruiz, “Frequency Domain Data Transmission using Reduced Computational Complexity Algorithms”, In Proc. IEEE Int. conf. Acoust., Speech, Signal Processing, pp. 964-967, Denver, CO, 1980.
6. Uwe Meyer-Baese, Digital Signal Processing with Field Programmable Gate Arrays, second edition, Springer, Berlin, 2004.
7. Paul A. Lynn, Wolfgang Fuerst, Introductory Digital Signal Processing with Computer Application, Second Edition, John Wiley & Sons, England, 1999.
8. Aseem Pandey,Shyam Ratan Agrawalla and Shrikant Manivannan, 2002, “VLSI Implementation of OFDM Modem”, White Paper, Wipro Technologies-Wipro Limited (NYSE:WIT).
9. “An Introduction to OFDM”, International Engineering Consortium (IEC), http://www.iec.org/online/tutorial/ofdm/topic04.html.
10. Brown, Stephen D Zvonko G. Vranesic (2000). “Fundamentalls of Digital Logic with VHDL Design”, McGraw-Hill Higher Education.
11. “Orthogonal Frequency Division Multiplexing (OFDM) Explained”, Magis Networks, Inc., February 8, 2001, www.magisnetworks.com.
12. Erich Cosby, 2001, “Orthogonal Frequency Division Multiplexing (OFDM): Tutorial and Analysis”, www.eng.jcu.edu.au/eric/thesis/Thesis.htm.

13. “Advantages of OFDM” http//pic.qcslink.com/introPLC/AdvOFDM.htm.
14. Fredrik Kristensen, Peter Nilsson and Anders Olsson, “Flexible baseband transmitter of OFDM”, www.sciencedirect.com.
15. “OFDM Tutorial”, Wave Report, www.wave-report.com/tutorials/ofdm.htm.
16. “Wide-Band Orthogonal Frequency Multiplexing (W-Band)”, White Paper by Wireless Data Communications Inc., www.wi-lan.com.
17. Rulph Chassaing, “Digital Signal Processing with C and the TMS320C30”, John Wiley & Sons, Inc., Canada, 1992.
18. Design of an OFDM Transmitter and Receiver using FPGA , Loo Kah Cheng, UTM, 2004.
19. Implementation of 8 point IFFT and FFT for OFDM system, Nor Hafizah Bt Abdul Satar, UTM, 2004.
20. Advanced Electronic Communication Systems, Wayne Tomasi, 5th edition, Prentice Hall 2001.
21. Communication Systems, Simon Haykin, 4th Edition, Wiley 2000.
22. Modulation and Coding for Wireless Communications, Alister Burr, Prentice Hall 2001.
23. VHDL for Designers, Stefan Sjoholm and Lennart Lindh, Prentice Hall 1997.
24. VHDL for Programmable Logic, Kevin Skahill, Addison Wesley 1996.
25. Single and Multi-Carrier Quadrature Amplitude Modulation: principle and Applications for Personal Communications, WLANs and Broadcasting, L.Hanzo, W.Webb and T.Keller, Wiley, 2000.