MECHANISM-BASED RELIABILITY MODEL FOR ELECTRONIC PACKAGES

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ABSTRACT

Mechanism-based reliability model is different from the conventional reliability model. It is generated based on a specific failure. The failure mechanism is studied in detail to obtain a model that incorporates all significant stressing variables. For fatigue driven failure, Coffin-Manson equation is the typical and most favourable model due to its simplicity. However, important variables in thermal cycling which are dwell time and ramp rate are not considered in this model. Studies were carried out to investigate the effects of dwell time and ramp rate on the reliability of electronic packages based on Bump Limiting Metallurgy (BLM) separation failure criterion. The experimental results showed that dwell time and ramp rate significantly affected the reliability performance of the BLM structure in the electronic package. The effect of ramp rate was converted into a newly introduced variable, called effective dwell time, $(t_{dwell})_{eff}$. Earlier failure of the BLM was observed with the increase of the $(t_{dwell})_{eff}$ and temperature change, ΔT. Silicon die side wall delamination (SWD) failure was studied to check the applicability of the same approach used in BLM reliability analysis to other fatigue driven failure in electronic package. The studies showed that the same approach was applicable in reliability modelling based on SWD failure. The increase of ΔT, dwell time and ramp rate could accelerate SWD failure.

ABSTRAK

Model reliabiliti berdasarkan mekanisme adalah suatu model yang khas dan berlainan dengan model reliabiliti tradisional. Ia diterbit berdasarkan satu jenis kegagalan. Mekanisme kegagalan tersebut dikaji untuk memperolehi satu model yang dapat menimbangkan semua permbolehubah yang penting. Persamaan Coffin-Manson merupakan model yang paling popular untuk kegagalan yang berkaitan dengan kegagalan kelesuan kerana ia mudah digunakan. Akan tetapi, dua pembolehubah yang penting telah diabaikan dalam persamaan tersebut, iaitu ‘dwell time’ and ‘ramp rate’. Kajian telah dijalankan untuk mengkaji kesan kedua-dua pembolehubah tersebut terhadap reliabiliti bagi suatu komponen elektrik berdasarkan suatu kegagalan. Kegagalan pada Bump Limiting Metallurgy (BLM) telah dikaji. Daripada eksperimen, didapati ‘dwell time’ dan ‘ramp rate’ dapat mempengaruhi reliabiliti BLM. Kesan ‘ramp rate’ telah ditukar dalam suatu pembolehubah yang baru iaitu ‘effective dwell time’ dalam kajian ini. Peningkatan ‘effective dwell time’ dan ΔT dapat mempercepatkan kegagalan BLM ini. Si-die side wall delamination (SWD) telah dikaji dengan menggunakan cara yang sama seperti yang digunakan dalam kegagalan BLM. Ini adalah untuk menunjukkan cara yang digunakan tersebut boleh digunakan pada kegagalan yang lain. Untuk kegagalan SWD, ΔT, ‘dwell time’ dan ‘ramp rate’ merupakan pembolehubah yang penting yang dapat mempercepatkan kegagalan tersebut.

TABLE OF CONTENTS

2 LITERATURE REVIEW

3 RELIABILITY STUDY FOR BUMP LIMITING METALLURGY (BLM) FAILURE

4 **RELIABILITY STUDY FOR DIE SIDE WALL DELAMINATION FAILURE**

5 **CONCLUSIONS AND RECOMMENDATIONS**

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

N_f - number cycle to failure

ΔT - temperature change

t_{dwell} - dwell time

$(t_{dwell})_{eff}$ - effective dwell time

r - ramp rate

t - time

T - temperature

Q - activation energy

K - Boltzmann's constant

ε - strain

R_t - reliability function

$f(t)$ - probability density function

$F(t)$ - cumulative distribution function

λ - failure rate

α - scale of Weibull distribution

β - shape of Weibull distribution

μ - log mean of Lognormal distribution

σ - shape of Lognormal distribution

Z - acoustic impedance

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

This thesis is presented as a partial requirement for the award of Master of Engineering (Mechanical). The research deals with reliability studies of electronic packages based on different failure mechanisms. This chapter introduces reliability assessment as applied in current electronic industries. The objectives, scope, methodology and layout of this thesis are presented in this chapter.

1.1 Background

In reliability assessment of an electronic package, Accelerated Life Testing (ALT) methods are used to accelerate the onset of failures with the single purpose of quantifying the life characteristics of the product under normal use conditions in a much shorter time. There are various ALT methods used in electronic industries such as Bake, Thermal Cycling, Power Cycling, Highly Accelerated Stress Test (HAST), Bias HAST, Mechanical Shock and Vibration, Temperature Humidity and Steam. (Tobias *et al.*, 1995)

Different ALT method is employed for different types of failure mechanisms in an electronic package. Bake method is used to accelerate diffusion and oxidation failure mechanism, Bias HAST is employed for metal migration and corrosion while vibration technique is utilized for brittle facture mechanism. Fatigue failure in electronic packages is normally predicted using Thermal Cycling tests. (Tobias *et al.*, 1995)

Thermo-mechanical fatigue failure has long been studied with respect to electronic package reliability (Agarwal *et al.*, 1999, Chien *et al.*, 2004, Guzek *et al.*, 1997, Pang *et al.*, 2002 and Sahasrabudhe *et al.*, 2002). The fatigue damage induced by thermal cycling is typically modelled using Coffin-Manson equation:

$$N_f = C(\Delta T)^{-m} \tag{1.1}$$

where N_f is number of cycle to failure, ΔT is temperature change and C and m are the coefficient and exponent, respectively. This Coffin-Manson equation is a favourable model for fatigue failure due to its simplicity. However, important variables in thermal cycling such as hold time at peak temperature and temperature ramp rate are not incorporated in this model. The hold or dwell time is defined as the time during which a package is held at the extreme temperature. Temperature ramp rate refers to how rapidly the temperature change happens in thermal cycling. The lack of dwell time and ramp rate effects in modelling the electronic package failure leads to the inaccuracy of the prediction of package reliability.

In addition to time varying temperature, the package has to endure a period of steady state operation where continuous deformation occurs due to creep and viscoplasticity. Consequently, dwell time is expected to have significant impact on the reliability of the electronic packages.

The ramp rate is directly related to the strain rate effect and affects the mechanical response of the package material. Thus, the ramp rate effect on reliability of electronic packages should be included in reliability model.

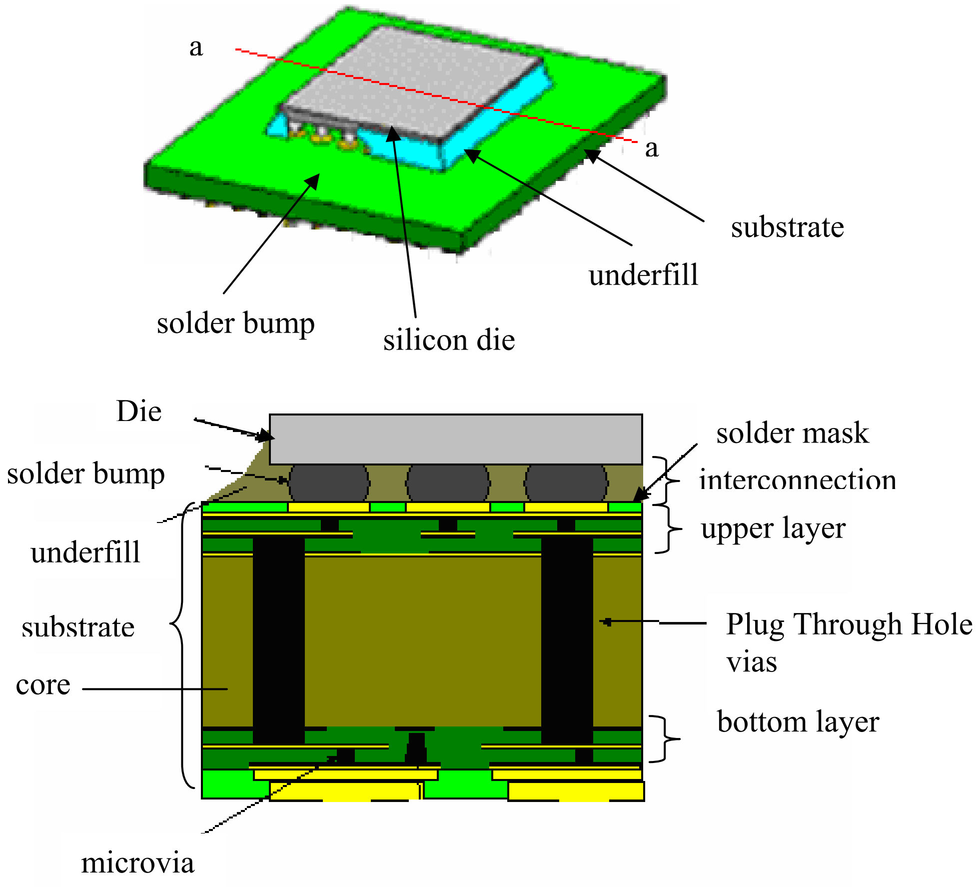
In this study, an experimental research is carried out to incorporate these two variables in modelling thermo-mechanical failures of electronic packages. The conventional Coffin-Manson model (equation 1.1) is modified to incorporate the ramp rate and dwell time effects. The modified model is validated and examined by two different failure mechanisms, namely, solder-related failure and side wall delamination of silicon die and underfill in a flip-chip.

The required thermal profiles with high and low ramp rate are obtained with two different temperature chambers; the air chamber (temperature cycle) and liquid chamber (thermal shock). The liquid medium promotes higher heat transfer rates than air and hence, the heating and cooling ramp rates of thermal shock are significantly higher than temperature cycle. The applicability of thermal shock in assessing electronic package reliability is examined.

1.2 Overview of Flip-Chip Product

In addition to wire-bonding technique, flip-chip is an alternative way to connect a chip/die to an electronic package. The flip-chip technology becomes increasingly popular in the electronic industries due to cost efficiency. Flip-chip technology provides the shortest possible leads, lowest inductance, highest frequency, best noise control, highest density, greatest number of Inputs/Outputs (I/O), smallest device footprints and lowest profile when compared with other popular interconnect method such as wire-bonding and tape automated bonding. (Michealides and Sitaraman, 1998)

Figure 1.1 is schematic of a flip-chip package. It consists of a silicon die, solder bumps, underfill and a substrate. The active surface of the die is mounted face down on the substrate, hence the term flip-chip. Flip-chip has utilized a Controlled Collapse Chip Connection (C4) die bumping technology for its die-to-substrate interconnection. This interconnection technology mounts the die onto the substrate using a matrix of solder bumps on the die surface, matching an array of solder bumps or lands on the substrate. The die is connected to the substrate using a reflow process. The process consists of heating the package to the reflow temperature and cooled down to room temperature in a controlled profile. The solder bumps will be protected by a layer of underfill epoxy. The substrate is a multilayered structure carrying an electrical circuit and provides mechanical and electrical path between the die and the application board or card. The various layers are connected by vias or channels that run perpendicular to the layers. The center layer of the substrate is a glass-fiber reinforced resin core which divides the substrate into upper and bottom layers and these two layers are connected using the Plated Through Hole (PTH) vias.



cross-section a – a

Figure 1.1 Schematic of a flip-chip

This C4 connection has always raised some reliability issues for the electronic packages due to solder bump crack and delamination between underfill and solder mask. These failures are caused by stress and strain due to different type of material Coefficient of Thermal Expansion (CTE) mismatch. Numerous studies on this C4 connection reliability in different aspects have been documented by eg. Bolanos et al., 2001, Chien et al., 2004, Pang et al., 2001, Tien et al., 1989 and Mustain et al., 1997.

1.3 Significance of Study

Although thermal cycling has long been used in reliability assessment of electronic package, it is apparently missing consideration for the dwell time and ramp rate effects. Consideration of these effects in a reliability model is expected to provide a more accurate prediction of package reliability.

Dwell time is incorporated into the analysis because it is one of the variables controlling creep mechanism in the package. The increase of dwell time can lead to larger creep strains in the package, therefore causing earlier failure.

Ramp rate is another considered variable in thermal fatigue failure. Fast ramp rate affects stress-strain response of the package materials. Therefore, its impact on the package reliability has to be investigated in order to have a much better reliability model.

The dwell time and ramp rate are incorporated in the reliability model based on the simple Coffin-Manson equation (1.1). This results in a simple model with physical parameters.

The proposed models are validated with the experimental data so that their predictive capability can be assessed.

1.4 Objectives

The objectives of this study are:

- Introduce dwell time and temperature ramp rate variables into a reliability model based on Coffin-Manson equation.
- Apply the modified Coffin-Manson model to electronic packages for solder fatigue failure.
- Validate the reliability model with experimental data and statistical analysis.
- Apply the methodology for the modified Coffin-Manson model to Si-die/underfill delamination failure.

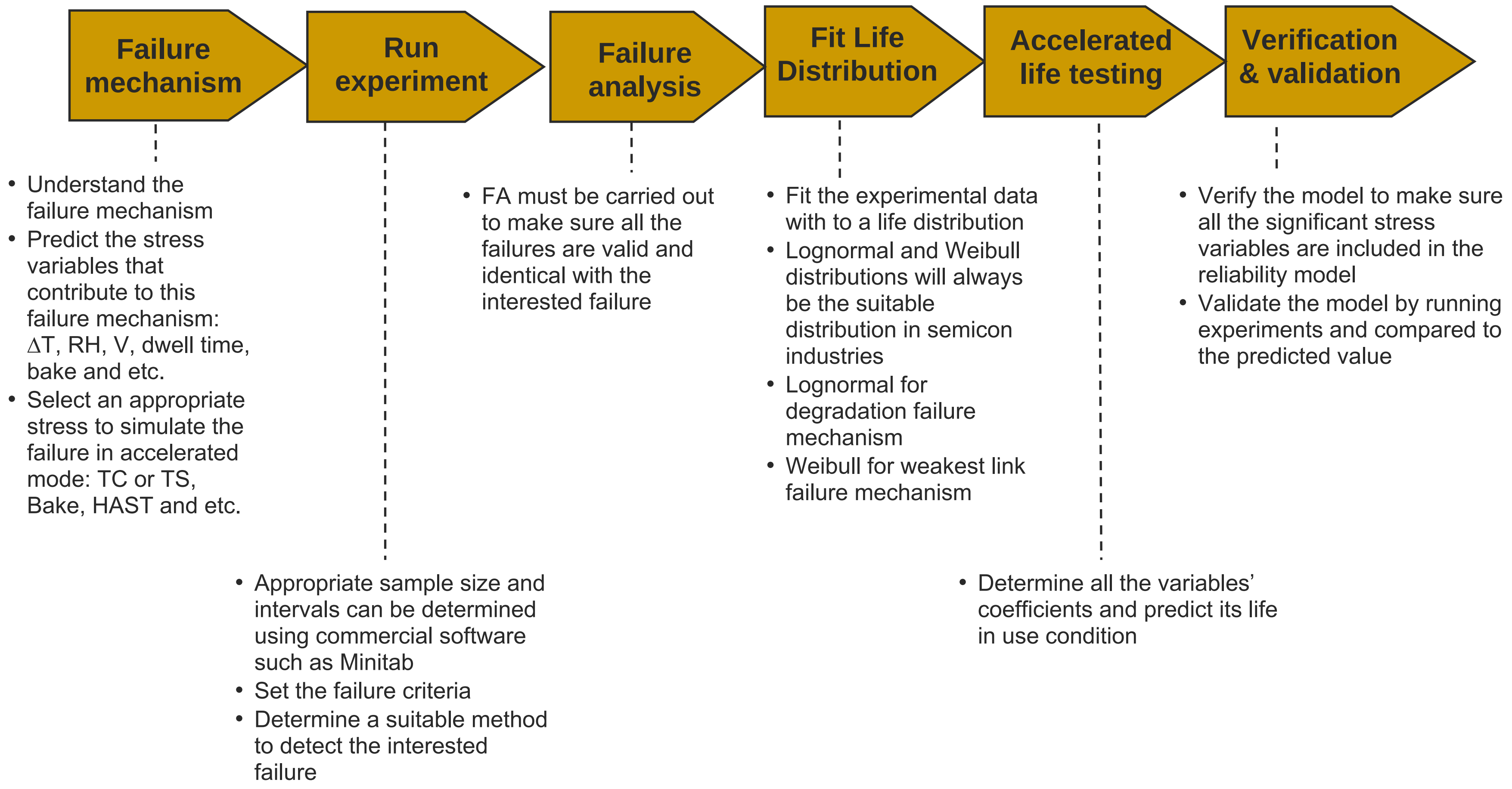
1.5 Scope

The scope of the study is limited to the followings:

- The proposed model is based on Coffin-Manson equation for low cycle fatigue failure
- The model is applied to flip-chip packages provided by the industry
- Temperature cycle and thermal shock profiles with multiple dwell times are used as the stressing method
- Two different failure mechanisms are investigated, namely Bump Limiting Metallurgy (BLM) separation and Side Wall Delamination (SWD) failure

1.6 Methodology

Figure 1.2 shows a step by step methodology in generating a reliability model based on a specific failure mechanism. The methodology is adopted in this research to generate the reliability model for a particular electronic package.



- Understand the failure mechanism
- Predict the stress variables that contribute to this failure mechanism: ΔT, RH, V, dwell time, bake and etc.
- Select an appropriate stress to simulate the failure in accelerated mode: TC or TS, Bake, HAST and etc.

- Appropriate sample size and intervals can be determined using commercial software such as Minitab
- Set the failure criteria
- Determine a suitable method to detect the interested failure

- FA must be carried out to make sure all the failures are valid and identical with the interested failure

- Fit the experimental data with to a life distribution
- Lognormal and Weibull distributions will always be the suitable distribution in semicon industries
- Lognormal for degradation failure mechanism
- Weibull for weakest link failure mechanism

- Determine all the variables' coefficients and predict its life in use condition

- Verify the model to make sure all the significant stress variables are included in the reliability model
- Validate the model by running experiments and compared to the predicted value

Figure 1.2 Methodology of generating reliability model for electronic package

STEP 1 Failure mechanism

The dominant failure mechanism is identified. The two failure mechanisms to be studied are Bump Limiting Metallurgy (BLM) separation and Side Wall Delamination (SWD) failure. The failure mechanisms are studied to determine the significant stressing variables which can accelerate the failure such as temperature change (ΔT), dwell time (t_{dwell}) and ramp rate. A reliability model is suggested to incorporate all significant variables. Then, experiments are planned to verify the suggested model.

STEP 2 Run Experiment

Experiments are carried out to collect the reliability data which is the number of cycle to failure in this case. The experiments are planned so that the effects of every significant stressing variable can be examined. In the experiments, multiple dwell times and ΔT can be easily obtained by changing the setting parameters of the chamber. However, multiple ramp rates with invariant dwell time and ΔT can only be obtained by using different heat transfer medium. In this research, air chamber (temperature cycle) and liquid chamber (thermal shock) are utilized to generate different ramp rates in the experimental profiles. The air chamber can provide 30 – 40 ºC/min ramp rate while the liquid chamber can give 370 – 380 ºC/min ramp rate. The failure criteria have to be set to capture the failed units during the experiments. C-mode Scanning Acoustic Microscopy (C-SAM) is used to detect the BLM separation while electrical testing is used to detect SWD failure. Units with C-SAM or electrical reject are considered as a failed unit in the studies.

STEP 3 Failure analysis

Failure analysis has to be done on the failed unit to make sure that the failure generated in the experiments is similar to the failure found in the use condition. Cross-section and SEM imaging are used to examine and identify the failure features.

STEP 4 Fit life distribution

Experimental data collected in Step 2 is fitted into a statistical life distribution. Weibull and Lognormal distributions are used to fit the reliability data in electronic industries. Lognormal distribution is used to fit BLM separation data while Weibull is used to fit SWD failure data.

STEP 5 Accelerated life testing

With the experimental data from Step 2, all the unknown coefficients in the model suggested in Step 1 can be determined using accelerated life testing technique. The test conditions are correlated to the use condition using the suggested reliability model.

STEP 6 Verification and validation

The generated reliability models are verified to make sure all the significant stressing variables have been included in the models. Extra experiment is carried out to validate the generated model. The experimental results are compared to the prediction from the model.

1.7 Thesis Layout

There are 5 chapters in this thesis. Chapter 1 introduces the topic of the research. The objectives, scope and methodology to generate a reliability model for a failure mechanism in electronic package are presented.

Chapter 2 presents the literature review on the related topics. The review covers electronic packaging, BLM, failure mechanisms in flip-chip, accelerated life testing and reliability model.

Chapter 3 describes the reliability model based on modified Coffin-Manson equation as applied to solder interconnection failure or called as bump limiting metallurgy (BLM) separation.

Chapter 4 demonstrates similar methodology in establishing reliability model but it is applied to Si-die/underfill delamination failure or called as Side Wall Delamination (SWD) failure. The applicability of the approach used in BLM separation on this SWD failure is examined.

The last chapter (Chapter 5) is the conclusions for the thesis. Major findings are summarized. Future works including refinement of the current model is presented.