CENTER OF ARTIFICIAL INTELLIGENCE AND ROBOTICS (CAIRO)

FINAL REPORT

VISION SYSTEM DEVELOPMENT PLATFORM

Project Code: 74504

UNIVERSITI TEKNOLOGI MALAYSIA

BORANG PENGESAHAN
LAPORAN AKHIR PENYELIDIKAN

TAJUK PROJEK : **DESIGN OF AN INTELLIGENT VISION INSPECTION FOR QUALITY CONTROL IN SEMINCONDUCTOR INDUSTRY**

Saya **PROF. DR. SHAMSUDIN HJ. MOHD. AMIN**
(HURUF BESAR)

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☑	TIDAK TERHAD	

TANDATANGAN KETUA PENYELIDIK

PROF DR. SHAMSUDIN H.M. AMIN
Dept. Of Mechatronic & Robotics Engineering
Faculty Of Electrical Engineering
Universiti Teknologi Malaysia
81310 UTM Skudai, Johor, Malaysia

Nama & Cop Ketua Penyelidik

Tarikh : 20/8/09

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ABSTRACT

Program identification: 03-02-06-0051 PR0022/04 - 02 (project 2)

Project title: Design of an Intelligent Vision Inspection System for Quality Control in Semiconductor Industry

This is the second project of the Program entitled "Design and Development of an Intelligent Vision Software with Integrated Automated Systems and their Applications". Unlike the first project of the program (Project Code 74503) the primary objective was to develop a PC-based engine for vision system development. In this project the focus is towards applying the in-house developed image processing library or better known as VSDP for quality control inspection in the semiconductor industry. Other than applying image processing techniques, feature extraction and artificial intelligence techniques were also applied in this project. This project involves research and data collection in identifying faults of semiconductors; especially in 4 key quality aspects of a semiconductor IC, which are (1) Marking Quality, (2) Lead Quality, (3) Package Quality and (4) Post Die Attach Quality.

The initial research approach of this project involved the study on the variety of faults that can occur on semiconductor chips. There are many types of faults that are required to be identified and a collection of database of chips with faults and no-faults have been carried out in the initial phase of this project. Some development of algorithms for fault diagnosis based on the four inspection purposes were carried out. A major part of the project involved in developing a software to acquire the images of the semiconductor chips and processing of the images using he VSDP Image Library. Another major software development is in the feature extractor and the application of neural networks, which is an artificial intelligence technique, in classification of the semiconductor faults. A semiconductor handling machine was also designed and fabricated which was used as a test-bed for the VSDP Image Processing Library and also the fault diagnostic software.

The project has shown the viability of the VSDP software and that it can be used for industrial applications. The semiconductor handling machine can be used as a test-bed for improving the VSDP software and the other algorithms for semiconductor quality inspection. However, in terms of commercialization further funding is required.

ABSTRAK

Program Identifikasi: 03-02-06-0051 PR0022/04-02

Tajuk Projek: Rekacipta Sistem Pemeriksaan Visi Pintar untuk Kawalan Kualiti Dalam Industri Semikonduktor

Ini merupakan projek kedua bagi program bertajuk "Rekacipta dan Pembangunan Perisian Visi Pintar dengan Sistem Integrasi Otomatik dan Aplikasinya" ("Design and Development of an Intelligent Vision Software with Integrated Automated Systems and their Applications"). Berbeza dengan projek pertama dari program ini, (Kod projek 74503), objektif utama projek ini adalah untuk membangunkan enjin berasaskan PC untuk pembangunan sistem visi. Tumpuan projek ini adalah untuk menggunakan perpustakaan pemprosesan imej yang telah dibangunkan iaitu VSDP bagi pemeriksaan kawalan kualiti dalam industri semikonduktor. Selain daripada menggunakan teknik pemprosesan imej, kaedah-kaedah pemetikan wajah dan kecerdikan buatan juga telah digunapakai dalam projek ini. Projek ini melibatkan penelitian dan pengumpulan data dalam mengenalpasti kecacatan semikonduktor terutamanya dalam empat aspek kualiti IC semikonduktor; (1) Marking Quality, (2) Lead Quality, (3) Package Quality and (4) Post Die Attach Quality.

Pendekatan awal penyelidikan dalam projek ini melibatkan kajian tentang kepelbagaian kecacatan yang wujud pada cip semikonduktor. Terdapat banyak jenis kecacatan yang perlu dikenalpasti dan pengumpulan data kajian cip yang cacat dan sempurna telah dilaksanakan pada peringkat awal projek ini. Beberapa pembangunan algoritem untuk dignosis kecacatan berasaskan empat tujuan pemeriksaan telah dijalankan. Sebahagian besar daripada projek ini telah melibatkan pembangunan perisian untuk mendapatkan imej cip semikonduktor dan pemprosesan imej menggunakan perpustakaan imej VSDP. Satu lagi pembangunan perisian utama ialah dalam pemetikan wajah dan aplikasi rangkaian neural iaitu satu teknik kecerdikan buatan dalam mengklasifikasi kecacatan semikonduktor. Satu mesin pengendali semikonduktor telah direkacipta dan dibuat dan telah pun digunakan untuk landasan pengujian perpustakaan pemprosesan imej VSDP serta perisian dignosis kecacatan.

Projek ini bukan sahaja menunjukkan kekuatan dan kewajaran perisian VSDP, malahan juga boleh digunakan dalam pelbagai aplikasi industri. Mesin pengendalian semikonduktor boleh juga digunakan sebagai landasan pengujian untuk memperbaiki lagi perisian VSDP dan lain-lain algoritma untuk pemeriksaan kualiti semikonduktor. Walaubagaimanapun, bagi tujuan mengkomersilkan hasil kajian ini, pembiayaan tambahan adalah diperlukan.

FINAL REPORT

VISION SYSTEM DEVELOPMENT PROGRAM

PROJECT # 2

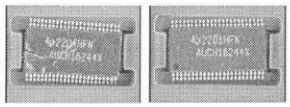
DESIGN OF AN INTELLIGENT VISION INSPECTION SYSTEM FOR QUALITY CONTROL IN SEMICONDUCTOR INDUSTRY

(VOT 74504)
04-02-06-0037PR0022/04-02

PRESENTATION OUTLINE

- **INTRODUCTION TO PROJECT 2**
- **OUR RESEARCH WORKS**
- **PROJECT INTEGRATION (74504 AND 74503)**
- **PROJECT MILESTONE AND PROGRESS**

INTRODUCTION



Images IC bad and good samples

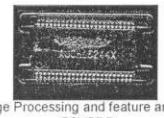


Image Processing and feature analysis Of VSDP

AI or smart Inspection algorithms

RESULTS

PROJECT 2 (VOT 74504) is responsible for researching methods of inspecting Integrated Circuit products through the methods of computer imaging and image processing with the aide of artificial intelligence and other smart algorithms that can measure the deviations between good samples and the bad.

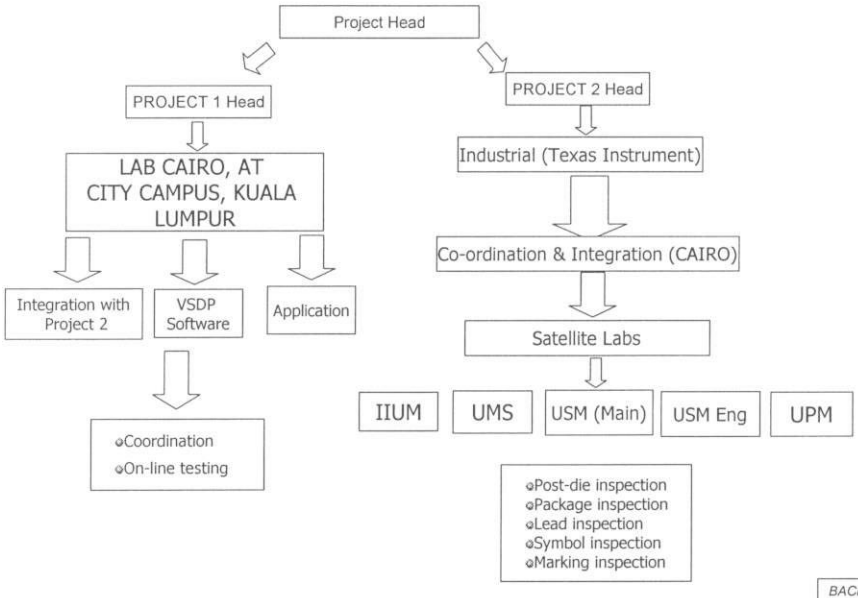
The image processing and image analysis tools will be provided by the group own image processing software **VSDP** developed by Project 1 in CAIRO..

Project 2 is comprised of 5 universities and one semiconductor industry:

1. Universiti Teknologi Malaysia.
2. Universiti Islam Antarabangsa Malaysia
3. Universiti Sains Malaysia (Nibong Tebal & Minden)
4. Universiti Malaysia Sabah.
5. Universiti Putra Malaysia
6. Texas Instruments Kuala Lumpur

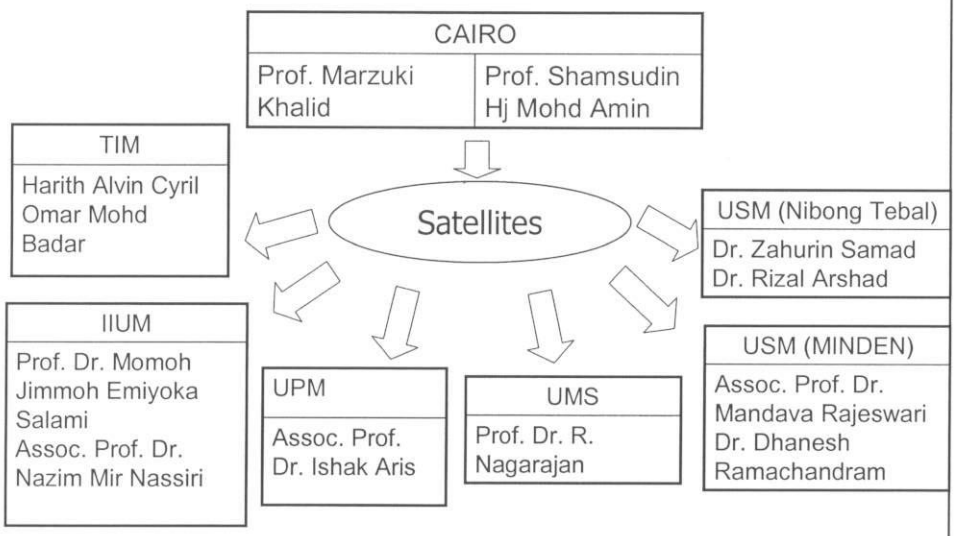
BACK TO MAIN CONTINUE

PROJECT ORGANIZATION



BACK TO MAIN

Team Members



Our Objectives

P*rimary objective is to design and develop the software and hardware components of an automated machine vision system for quality control in a Semiconductor Manufacturing Industry.*

BACK TO MAIN

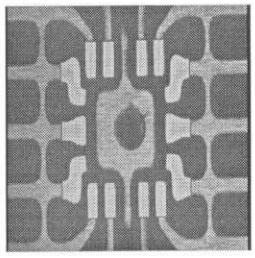
Secondary Objectives are as follows:

- To utilize new techniques in image processing and Artificial Intelligence for optimal system performance and robustness pertaining to semiconductor industry, to enhance quality control.
- To test the capability and efficiency of the system on 4 key quality aspects of a semiconductor IC, which are :
- (1) Marking Quality,
- (2) Lead Quality,
- (3) Package Quality and
- (4) Die Attach Quality

BACK TO MAIN

SATELLITES RESEARCH

UNIVERISITI SAINS MALAYSIA (MINDEN)

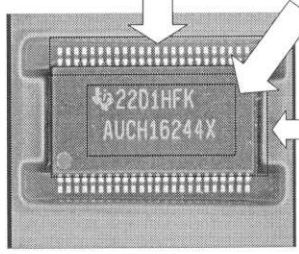


DIE INSPECTION

UNIVERSITI ISLAM ANTARABANGSA MALAYSIA *LEAD QUALITY INSPECTION*

UNIVERISITI PUTRA MALAYSIA & UNIVERSITI MALAYSIA SABAH *MARKING QUALITY INSPECTION*

UNIVERSITI SAINS MALAYSIA (KAMPUS KEJURUTERAAN) *PACKAGE INSPECTION*



IC TERMINAL INSPECTION

BACK TO MAIN

PROJECT OUTLINE

- Title :
  - **Design of an Intelligent Vision Inspection Systems for Quality Control in Semiconductor Industry.**
- Objectives:
  - **Utilize new techniques in IP & AI to enhance the performance and robustness of QC on IC's.**
  - **Test capability on 4 key quality aspect, i.e. Marking, Lead, Package and Post Die Attach.**
  - **To integrate these techniques into the generic vision system developed in Sub Project #1.**

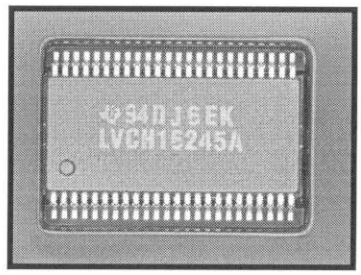
TARGETED PROCESS

- **Saw Process**
- **Die Attach Process**
- **Die Bond Process**
- **Molding Process**
- **Laser/Trim&Form Process**
- **Visual Mechanical Gate Process**
- **Testing Process**
- **T/Reel Process**

Texas Instruments Malaysia
IRPA Top-Down VSDP – Targeted Package.

Why TSSOP-DGG Package?

- Thin (1mm thickness) is prone to package defects, ie cracks,chips,voids and expose wire/expose pad.
- Large Pin Count, challenging to Lead Algorithm, accuracy and speed.
- Large FOV, poor accuracy and limited magnification.
- Large Surface area for marking drift.



48,56,64pins

Targeted Package.

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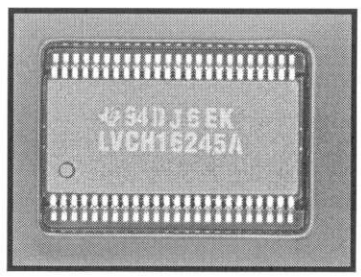
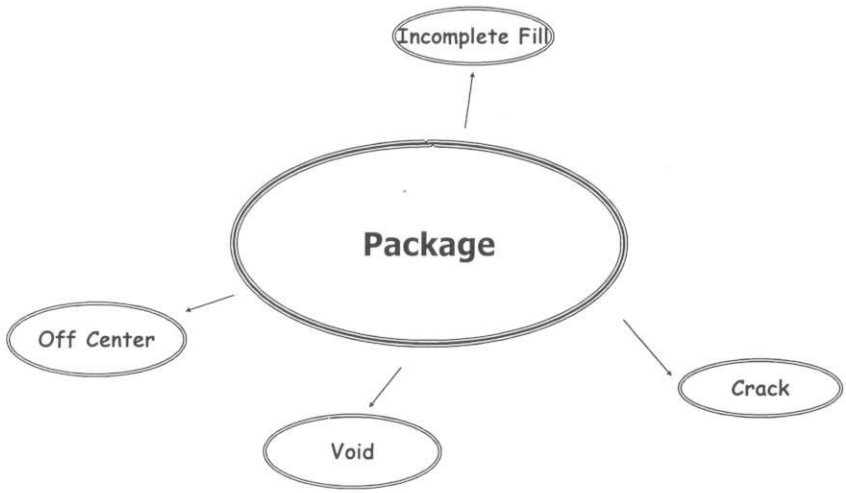


48,56,64pins

Package Quality Features



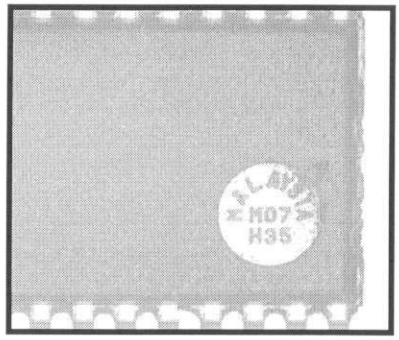
Package Quality Features

Package Specification

- **Critical Package Dimensions.(mm)**
  - i. **Body Width** - 6.0min/6.2max.
  - ii. **Body Length** - 12.40min/12.60max(48pin)
    - 13.90min/14.10max(56pin)
    - 16.90min/17.10max(64pin)
  - iii. **Body Thickness** - 1.20max
  - iv. **Seating Plane** - 0.05min.

Package Quality Features

Package Specification

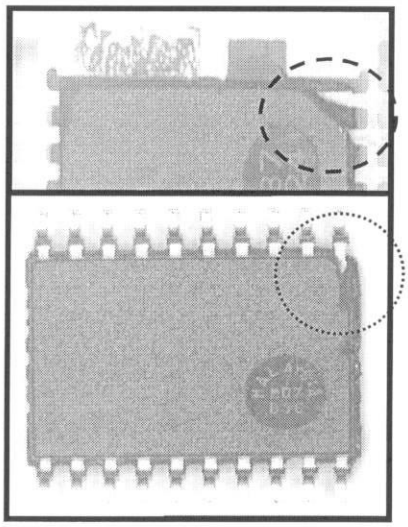


Void

- Irregular imperfections on the surface of the package which has the appearance of a partial hole or an inverted bubble…..
- Max allowable diameter 0.13mm.

Package Quality Features

Package Specification



Incomplete Fill

Missing plastic at a package side or end, or at the package intersection of two or more sides

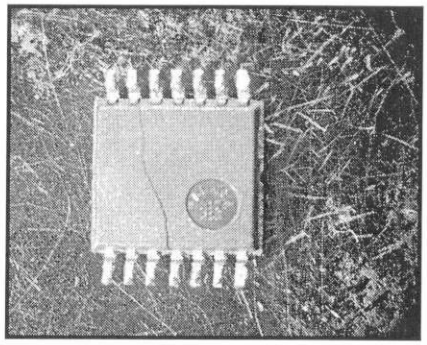
Max allowable long is 0.25mm and max allowable deep is 0.13mm.

Reject if encapsulated parts are exposed.

Max allowable chip is 0.25mm.

Package Quality Features

Package Specification

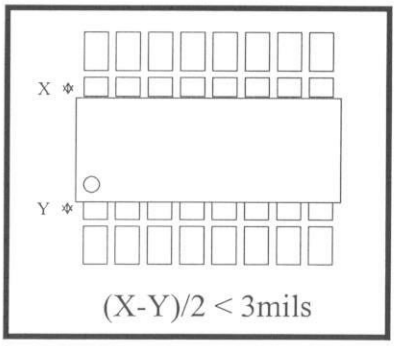


Crack

Reject any part showing signs of crack or broken parts.

Package Quality Features

Package Specification



Offcenter/Offset

Any part of the top or bottom plastic are misaligned either to themselves or to the lead frame.

Max allowable is 0.75mm.

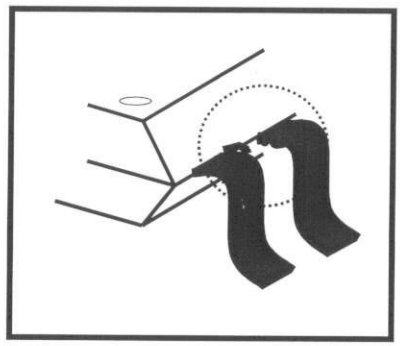
Lead Frame Inspection is required.

Package Quality Features

Package Specification

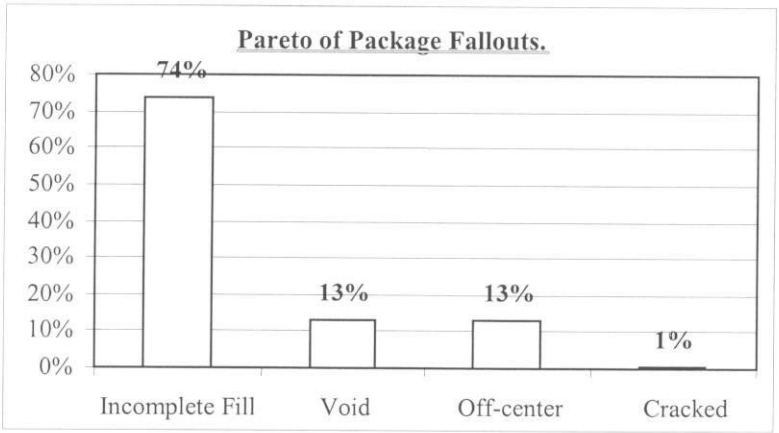
Other Defects....

- Mold Protrusions/Flash,
- Chip....



Surface Flash

Package Quality Features



Package Quality Features

Comments/Recommendations.

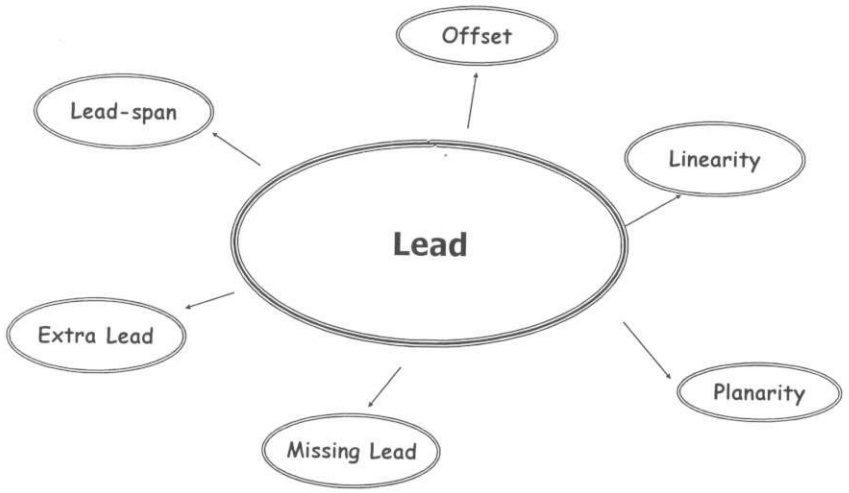
- Vision solution is new in the market. Called Package Inspection or PVI(Package Visual Inspection). Read Brochures
- Ability to detect defects and having low overkill is key within competition. Cosmetic Inspection.
- Competitors have <0.05% overkill and able to detect defects up to 4pixel small with multi camera hook up. Total inspection time <200ms.
- All prefer to use high resolution camera.
- Start off research on top view inspection only and migrate to top and bottom view inspection for final product (lead frame base inspection).
- Require multi camera interface to capture the entire FOV of lead frame.
- Lighting and Optics design is key in highlighting the defects. (Prostar)

Package Quality Features

Success Gauge.

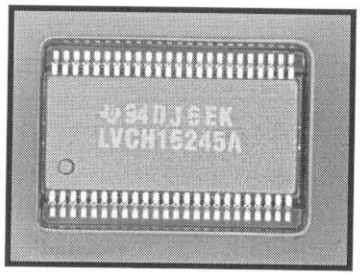
- Feasibility
- Resolution must equal 4pixel.
- Overkill of less than 0.05%.
- Able to differentiate the many different package defects.
- Stage 2 – Top and Bottom Package on Lead Frame Inspection.
    - Multi Camera for entire FOV of leadframe.
    - Inspection time <200ms.
    - Real Time Inspection.

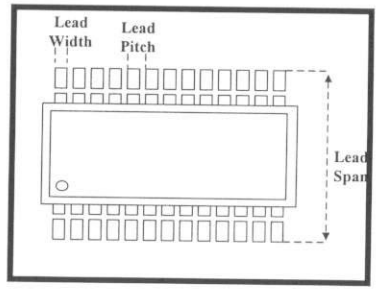
Lead Quality Features



Lead Quality Features

Lead Inspection.

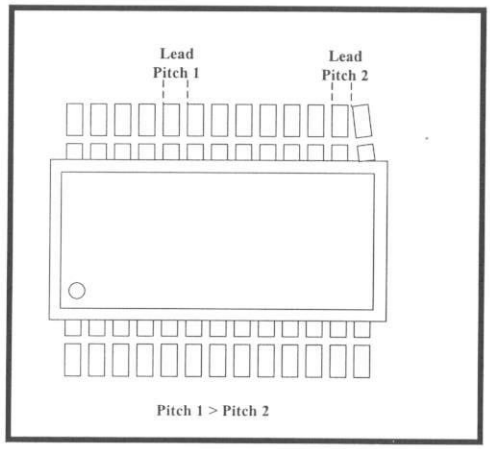




- Critical Lead Dimensions.(mm)
  - i. Lead Pitch - 0.50.
  - ii. Lead Width - 0.17min/0.27max
  - iii. Lead Span - 7.90min/8.30max

Lead Quality Features

Lead Specification

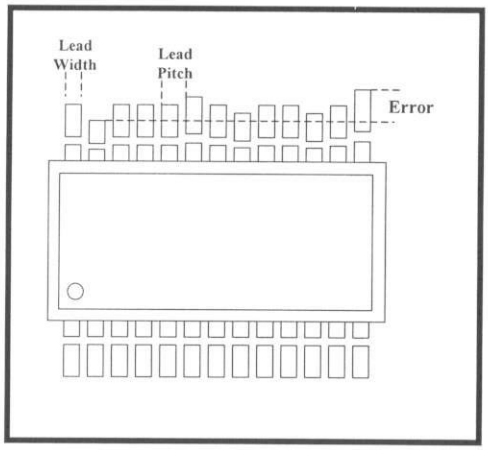


Offset Detection.

- Lateral bent lead.
- Pitch Errors
- Max allowable 0.1mm.

Lead Quality Features

Lead Specification



Implied Planarity

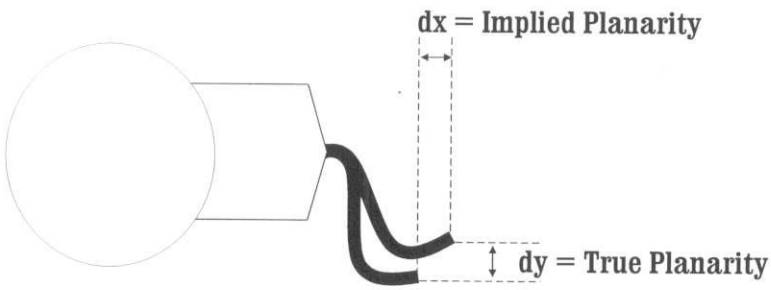
- Vertical bent lead.
- Implied Measurement
- Max allowable 0.1mm.

Linearity.

- Lead Extension out of average.
- Max allowable 0.1mm

Lead Quality Features

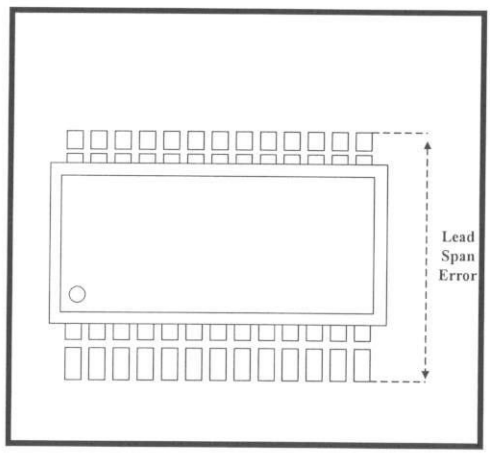
Lead Specification



Note , If *dy*=0 then defect is classified as Linearity Error.

Lead Quality Features

Lead Specification



Lead Span

- Tip to Tip Variation.
- Max allowable 0.375mm.

Lead Quality Features

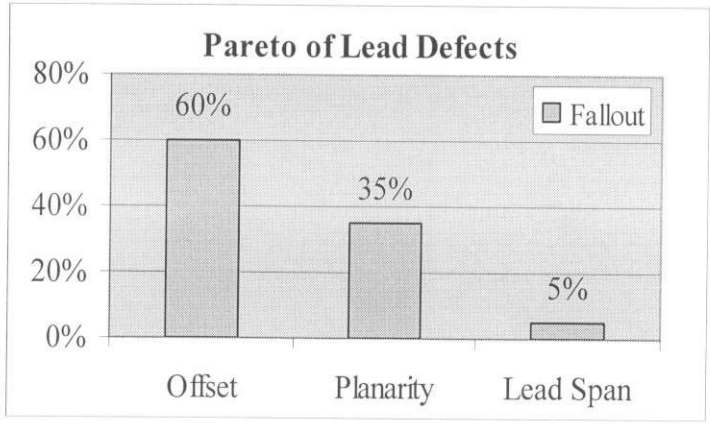
Lead Inspection.

Other Defects....

- **Lead Width – Max 25% of area.**
- **Missing Lead**
- **Extra Lead.**
- **Lead Cosmetics....**

Lead Quality Features

Lead Inspection.



Lead Quality Features

Lead Inspection.

Comments/Recommendations.

- **Vision solution is widely available.**
- **Speed, Accuracy ,Overkill, Cost and Introductions of Special Features are the competitive tools.**
- **Minimize the intervention of operators.**
- **Review brochures on vision system to understand latest offering.**
- **Propose optimized lighting,optics and camera configuration in mid-stage of research.**
- **Ensure package parameters remain a variable for future addition of new packages.**

Lead Quality Features

Lead Inspection.

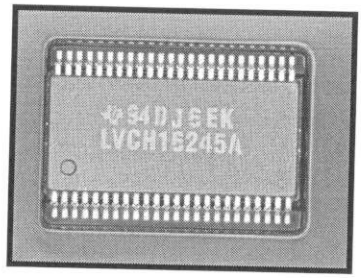
Success Gauge.

- **Feasibility**
- **GRR of <10%.**
- **Accuracy must meet or exceed ½ pixel.**
- **Overkill of less than 0.05%.**
- **Target for Zero Escape.**
- **Full Blown Inspection Time(image accusation and processing) > 20kpph(min)**

Marking Quality Features

Marking Quality Features

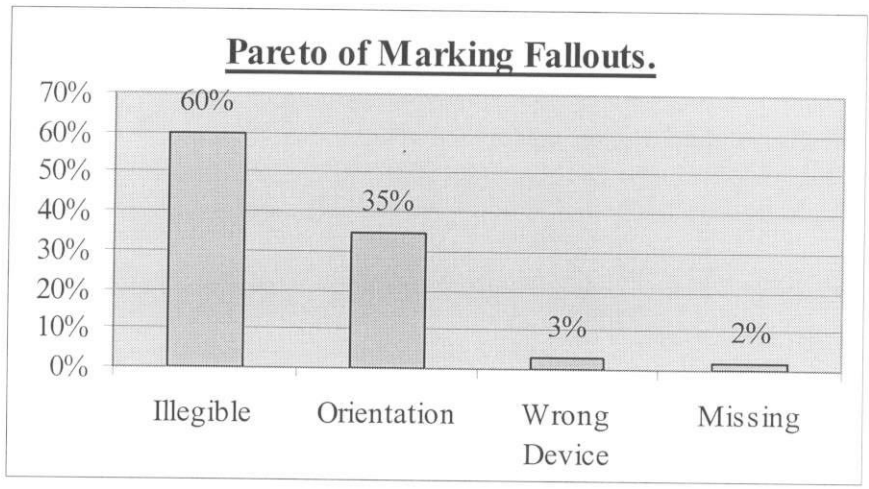
Symbol Inspection.



- Critical Specification.
  - i. Right Marking.
  - ii. Clear and Present and does not leave a doubt to it's identity when read.
  - iii. Orientation with respect to pin 1.

Marking Quality Features

Marking Inspection.



Marking Quality Features

Marking Inspection.

Comments/Recommendations.

- **Solution in the market is mature but prone to high overkills.**
- **OCR is currently being offered but no success rate claim is made.**
- **OCR is however being requested by customers.**
- **Minimize setup time by the operator during teaching.**
- **System must be robust to font variations.**

Marking Quality Features

Marking Inspection.

Success Gauge.

- **Feasibility**
- **Overkill of less than 0.05%**
- **Target zero escape.**
- **100% OCR implementation.**
- **OCR success rate must exceed 95%.**

UTILIZATION OF HUMAN RESOURCE

- Main Lab (CAIRO) – 3 Research officers
- USM Lab (Minden) – 2 Research officers
- USM Lab (Nibong Tebal) – 3 Research officers
- IIUM Lab – 2 Research officers
- UPM Lab – 2 Research officers
- UMS Lab – 2 Research officers

BACK TO MAIN

PROJECT 2 RESEARCH

LEAD INSPECTION
(UNIVERSITI ISLAM ANTARABANGSA MALAYSIA)

MARKING INSPECTION
(UNIVERSITI PUTRA MALAYSIA & UNIVERSITI MALAYSIA SABAH)

DIE INSPECTION
(UNIVERSITI SAINS MALAYSIA, MINDEN)

PACKAGING INSPECTION
(UNIVERSITI SAINS MALAYSIA, KAMPUS KEJURTERAAN)

BACK TO MAIN

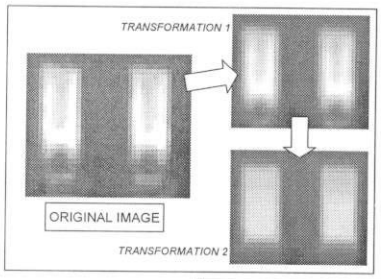
UIAM

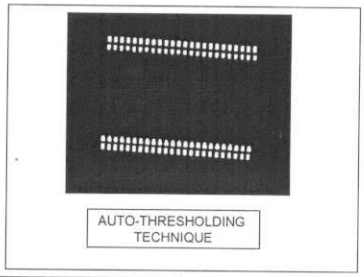
- Title: Development of microchip lead inspection algorithms
- Techniques developed:

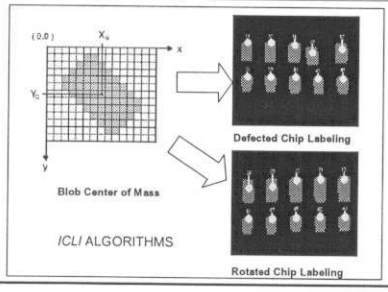
1. Image enhancing algorithms that specifically enhances the IC leads and thus, ensuring the accuracy of the visual inspection.
2. Come up with *ICLI* algorithms. These algorithms can inspect any IC models which come in different sizes and orientations, based on BLOB (Binary Large Objects) analysis technique.
3. Image Auto-thresholding techniques that can discriminately choose only the leads and not other features in an image that similarly in shape.

BACK TO MAIN

TECHNIQUES RESEARCHED







BACK TO MAIN

USM MINDEN

- Title: Development of Intelligent vision system for semiconductor's die inspection.
- Techniques developed :

1. New, faster and more accurate algorithms in detecting four categories of die defects (missing die, misplaced die, broken die, and chipped/crack die.
2. Techniques of inspection:

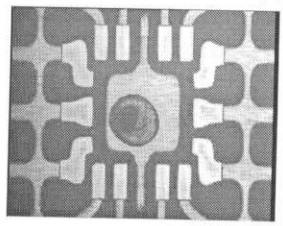
- XOR/ subtraction for missing die detection.
- L1 Norm /K-Means clustering for missing die (void) inspection.
- Pro EDH (Edge Detection Histogram) for broken die detection.
- Template matching and Center of Gravity for misplaced die.

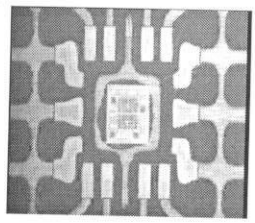
BACK TO MAIN

Major Categories of Defects

Particle	***Pattern***
anomalies, particle contamination	extra, missing, incorrect pattern
Contamination by particles such as epoxy on die, epoxy on lead	Improper handling, non-ideal process (broken die, chips, cracks , scratches etc.)

Missing Die



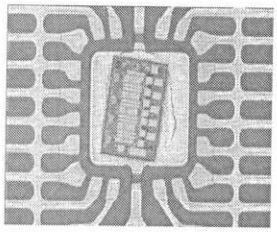


- Die is missing on mount pad
- Good segmentation algorithm required to separate bond pad, epoxy and die
- Inspection can be based on shape parameters or pixel neighborhood intensity analysis

Inspection Methods:

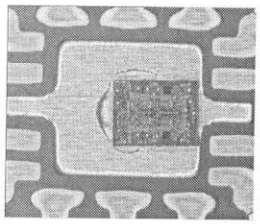
- Subtraction/XOR
- Image Projection Profile - Statistical Values
- Summation of Absolute Valued Differences (SAVD)/ L1 Norm

Misplaced Die



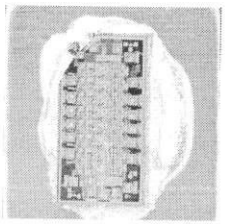
- Die is misplaced during die attach process
- Can materialize as off-center or tilted die
- Offset measurement may be calculated with reference to a good die.
- Therefore a *quantifiable defect*

Inspection Methods :

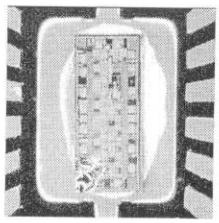


- Based on Image Moments
- Based on Normalized Gray Scale Correlation Template Matching

Broken or Chipped die



- Die is broken or chipped during die attach process
- Can materialize in different shapes and sizes
- Qualitative description for chipped/cracked die
- Quantitative measurement may be performed on broken die



Inspection Methods :

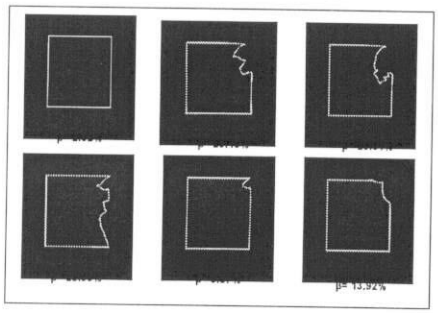
Broken Die

- Based on edge direction histogram
- Based on r-θ profile

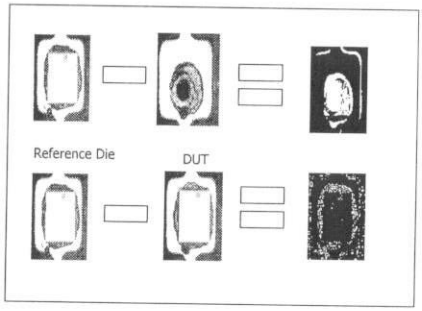
INSPECTION METHODS RESEARCHED

- Subtraction/ XOR.
- L1 Normalization/ K Means.
- Edge Direction Histogram.
- Minimum Enclosing Rectangle.
- Normalized Grayscale Correlation.
- Template matching.

Techniques used for Die Inspection (examples).



Edge Direction Histograms



SUBTRACTION/XOR

BACK TO MAIN

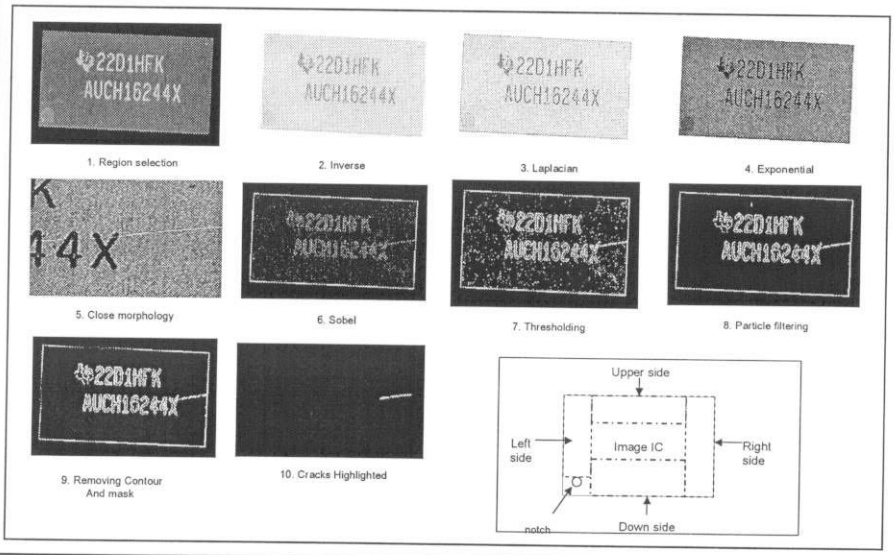
USM (ENGINEERING CAMPUS)

- Title: Design of an Intelligent Vision Inspection Systems for Semiconductor Packaging.
- Techniques developed :

1. Using template matching and image processing to detect 2 types of packaging defects (incomplete fill and cracks).
2. The algorithm even manage to detect the hairline cracks which are almost invincible to human sight.

BACK TO MAIN

INSPECTION METHODS RESEARCHED (CRACKS DETECTION)



INSPECTION METHODS RESEARCHED (IN-COMPLETE FILL DETECTION)

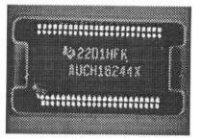
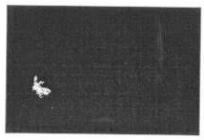


Image after using Look up Table operator:

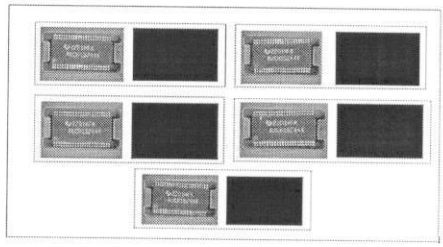
(Transfer function: Square)

Image after using threshold:
(Lower value: 29.11, Upper value: 66)

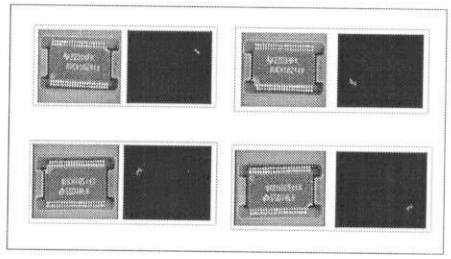
Removing Borders



Removing Particles

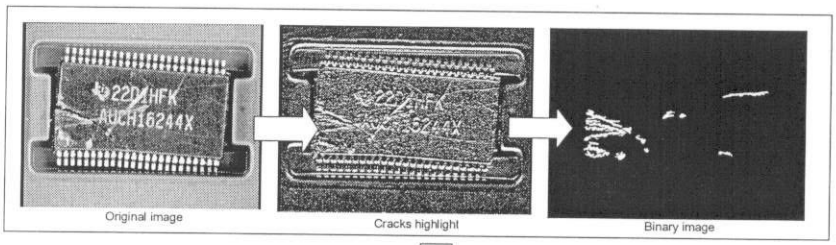


For good parts, no blobs showing up after the processing



For Bad parts, blobs of the in-complete fill showing up after the processing

Packaging crack detection



Original image

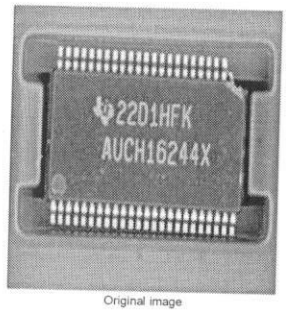
Cracks highlight

Binary image

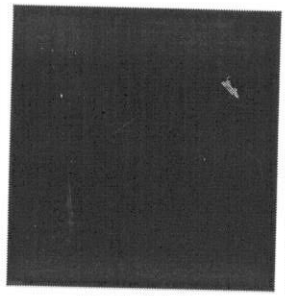
BLOB Analysis
&
Template matching

BACK TO MAIN

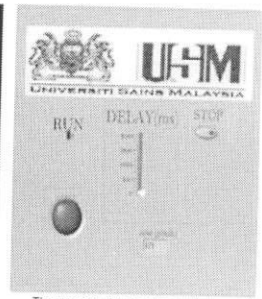
Incomplete fill detection



Original image



Incomplete defect detected



The program developed for this research

BACK TO MAIN

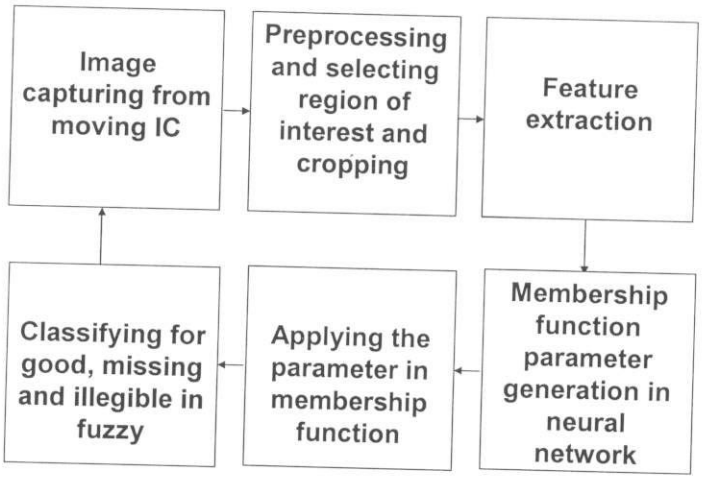
UMS

- Title: Development of a Real time Vision Software for Inspecting The Marking and Symbol on Integrated Circuit Chips.
- Techniques developed:

1. Incorporates VSDP with Neural Networks and Fuzzy-Logic techniques for detecting marking defects.
2. Good accuracy and fast for defects detection.

BACK TO MAIN

The methodology of inspection



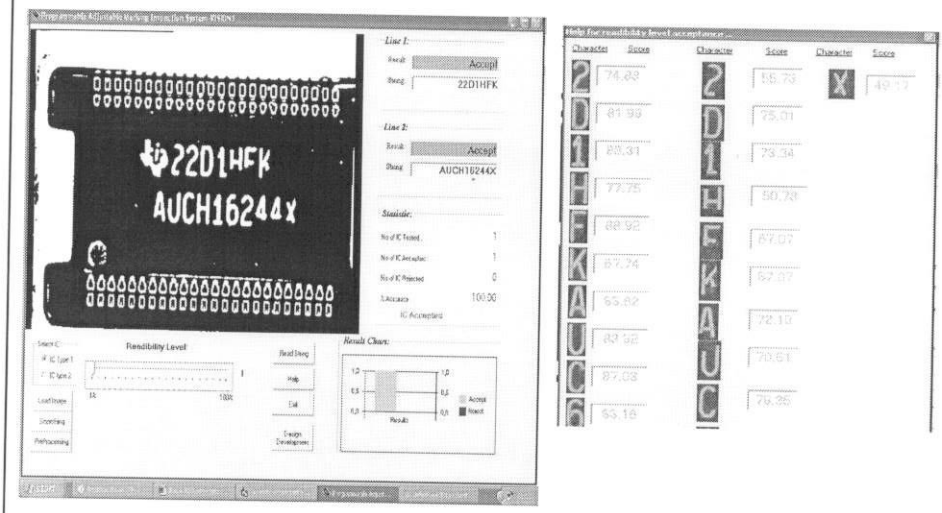
BACK TO MAIN

UPM

- Title: Design and Development of Character and Marking Inspection for Semiconductor Industry
- Techniques developed :

1. Using BLOB (*Binary Large Objects*) analysis and Optical Character Recognition (OCR) to read the marking characters on the IC and check whether the reading is right.
2. Developing the Readability Level technique which increases the OCR accuracy according to the sight of the operators.

BACK TO MAIN



The software developed for the Marking Inspection

BACK TO MAIN

PROJECT INTEGRATION

The 2nd part of the Project 2 task is to integrate all the satellites' research work into a complete system which run VSDP software as the machine vision programming platform. The integration work will take place in CAIRO, UTMKL.

The integration part consist of these tasks:

- Translating the satellites algorithm into VSDP programming.
- Integrating the translated codes into a complete software part of the machine vision system for the automated inspection.
- Designing and fabricating the IC terminal vision inspection machine.
- Integrating the software and the machine into a full automated vision inspection system for both IC and post die inspection.

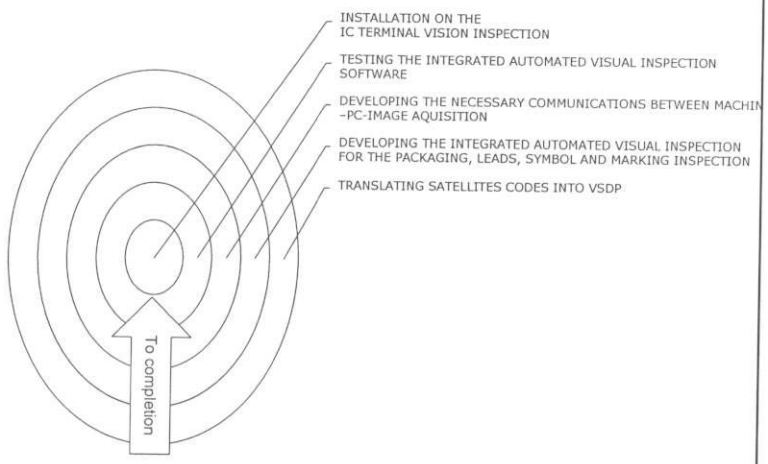
BACK TO MAIN

Project 2 Objectives

- To develop an integrated Automated Vision Inspection system that will be installed in IC terminal vision inspection.
- The inspection software will be using 100% of the in-house produced VSDP software.
- To translate the satellites' research into the VSDP platform.
- To build more features to facilitate the satellites research through Project #1.
- To test the integrated system with IC samples on the IC terminal vision inspection system.

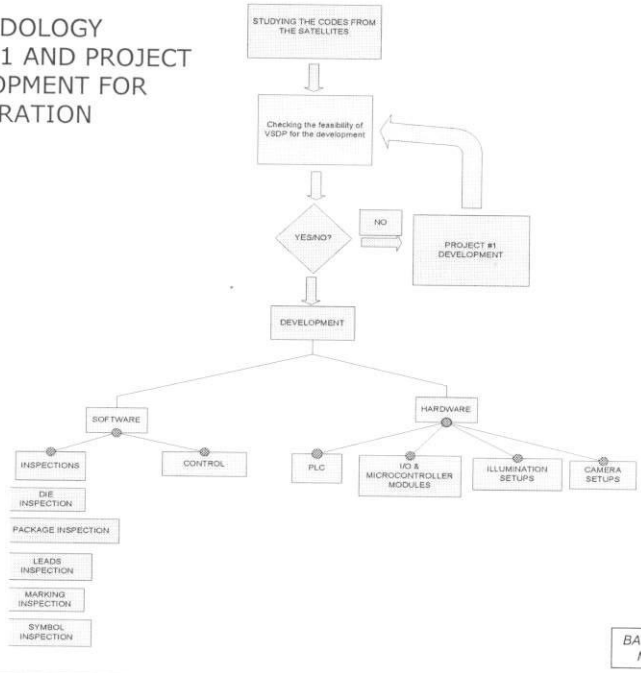
BACK TO MAIN

Development Strategies



BACK TO MAIN

METHODOLOGY
OF PROJECT #1 AND PROJECT #2 DEVELOPMENT FOR INTEGRATION



BACK TO MAIN

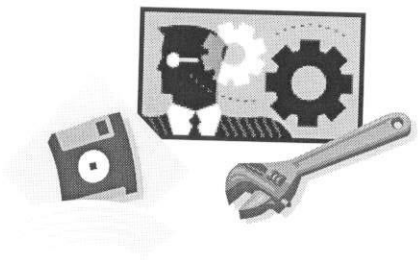
Hardware Setups - System Overview

- Translating codes to VSDP
- IC Handler
- PC-PLC Communication
- Lighting Control

BACK TO MAIN

Design Strategies

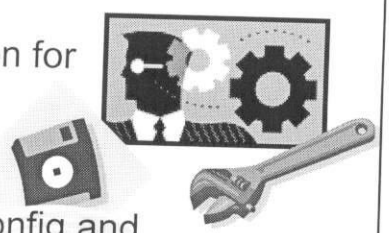
- **Platform:**
  - Wintel (Windows 2000/Intel Pentium)
  - Component Object Models (COM) – ActiveX Control
- **Programming Languages:** C/C+, Visual Basic
- **Target Applications:**
  - Lead inspection
  - Marking inspection
  - Package inspection.
  - Symbol Inspection
  - Die Inspection



BACK TO MAIN

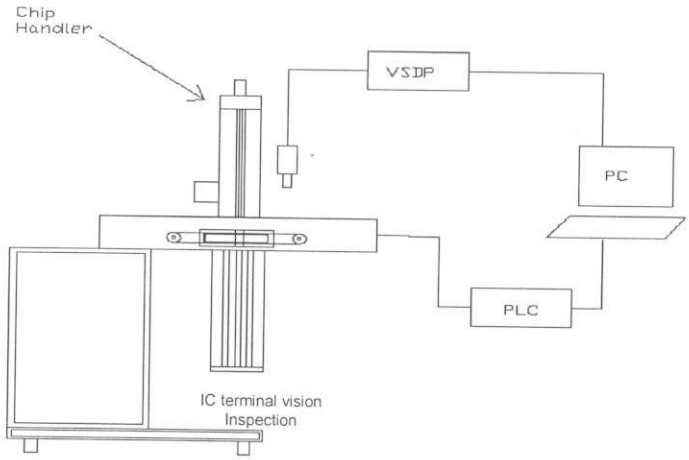
Design Strategies

- Automation design:
  - AutoCAD
  - PLC: Siemens S7-300
- Machine – PC Communication for image acquisition
  - Serial port communication
  - Parallel port communication
  - VsImageBW8u, VsCameraConfig and Image8u from VSDP.



BACK TO MAIN

Overview of the whole system



THE INTEGRATED VISION INSPECTION SYSTEM VSDP

BACK TO MAIN

TRANSLATION
SATELLITES'S CODE – VSDP PLATFORM

- The translation depends on the submission of codes by the satellites.
- Submission of research codes, manual & literature by the satellites→ completed.
- Translation depending on availability of functions on VSDP. Any functions that is unavailable on VSDP will be notified to Project 1 team.

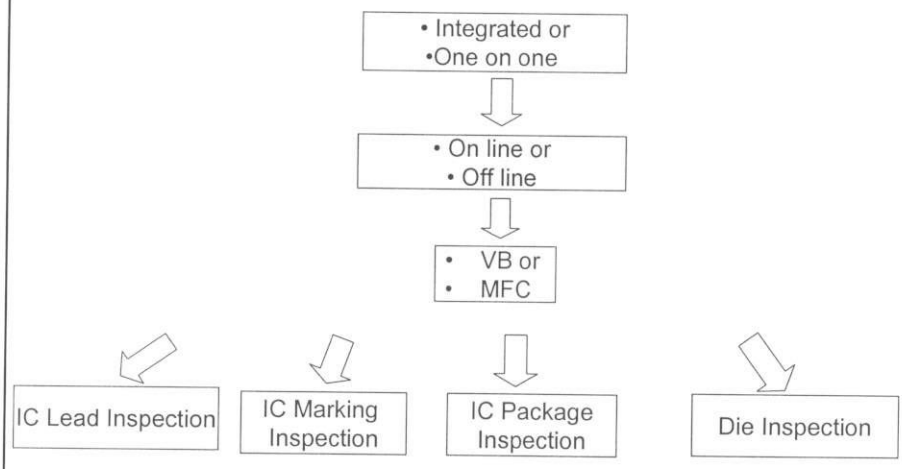
Refer MILESTONE

BACK TO MAIN

VSDP COMPATIBILTY WITH THE SATELLTIES RESEARCH (ON JULY 2004)

INSPECTION	UNIVERSITY	SOFTWARE USED	FEATURES USED	VSDP (SUPPORT?)
LEAD QUALITY	UIAM	LABVIEW with IMAQ VISION	BLOB ANALYSIS	YES
			IMAGE MORPHOLOGY	YES
			IMAGE FILTERS	YES
			IMAGE THRESHOLDING	YES
MARKING & SYMBOL QUALITY	UPM & UMS	MATLAB	OCR	YES
		MATROX	OCV	YES
			BLOB ANALYSIS	YES
			IMAGE THRESHOLDING	YES
			REGION OF INTEREST	YES
PACKAGE QUALITY	USM (ENG CAMPUS)	LABVIEW with IMAQ VISION	PATTERN MATCHING	NO
			BLOB ANALYSIS	YES
			IMAGE THRESHOLDING	YES
			REGION OF INTEREST	YES
DIE ATTACH QUALITY	USM (MINDEN)	MATLAB	PATTERN MATCHING	NO
		MATROX	HISTOGRAM ANALYSIS	YES
			REGION OF INTEREST	YES
			IMAGE THRESHOLDING	YES
			BLOB ANALYSIS	YES

VSDP IC Inspection software system



Styles of Inspection

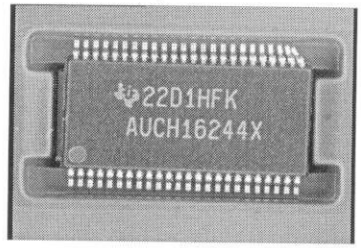
1. Integrated Inspections
   - All inspections (Leads, Marking and Packaging Inspection) will be performed to an image.
   - Inspection routines might drag time.
   - Efficiency will be compromised.
   - Suitable for demo purposes.
2. One on one (One inspection per session)
   - Only one inspection per machine or session.
   - But time and processing efficient.

ON LINE / OFF LINE MODE

- On line mode requires integration with hardware that communicating with the machine vision system. The hardware are, for example: camera, frame-grabbers, lighting controller, I/O communications.
- Off line mode only requires stored image to do the inspection. No hardware is involved.

Designing Illumination for IC Inspection

To avoid from using too much image restoration and image enhancing algorithms to reduce noises and unwanted backgrounds. This can save memories and computation time.



IC being lit with conventional Ring light

The importance of controlled illuminations

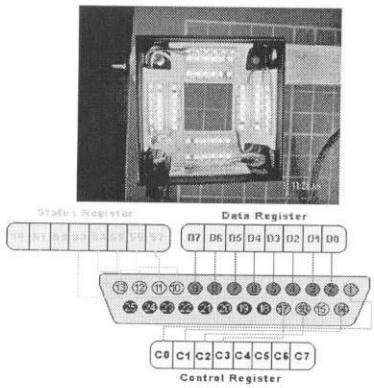
To highlight certain features on the IC while attenuating others (according to the inspection criteria).

To reduce noises at objects Vs background

BACK TO MAIN

Lighting Control

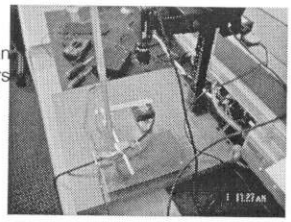
- Lighting consists of 12 rows, each row has 6 LEDs.
- Using parallel port to control each row of light.
- Control through 8 data lines and 4 control lines of parallel port
- Designed interfacing circuit to switch on and off of lights from parallel port.

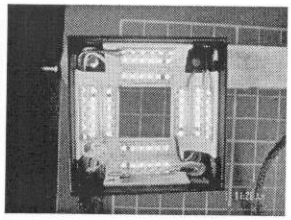


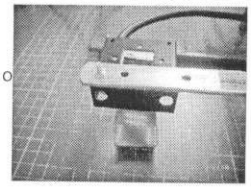
BACK TO MAIN

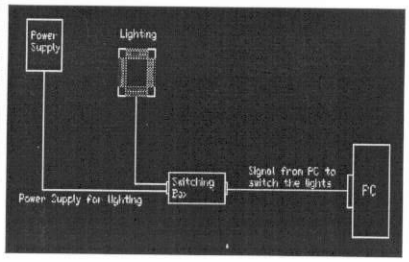
Designing Illumination for IC Inspection

- LED lights. Specification
- 12 panels of illuminators
- Each panel consists of 12 arrays of LED.
- Methods of controlling: Parallel IO and Visual Basic.
- **Objectives:**
- To **ON-OFF** lighting panels which are required for the experiment.
- To investigate combos o light panels which are suited for certain IC inspection criteria.









BACK TO MAIN

Lighting Design Methodology

Identify cable color of each LED panel

Designing switching circuits (relay switches)

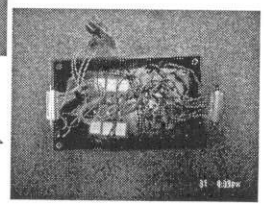
Parallel port communication (reading and writing)

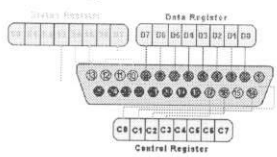
Assembly parts

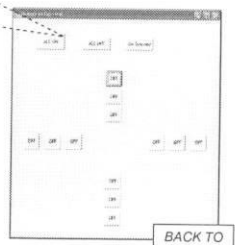
Experiments lights on IC

Deciding combo for each insp. routine

Build the combo into IC terminal

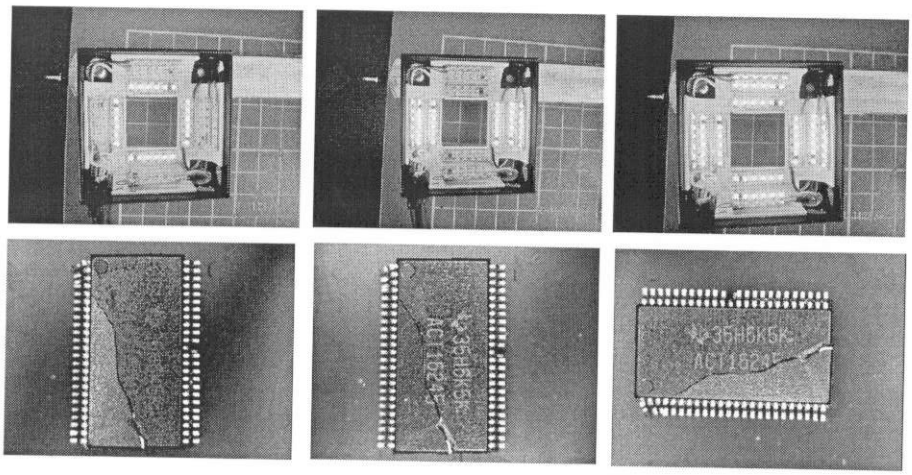






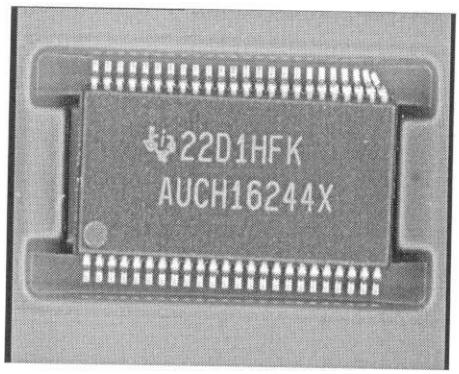
BACK TO MAIN

RESULTS:



BACK TO MAIN

Inspection image from Texas Inst Vs the image from the inspection FOV



Training image given by Texas Instruments

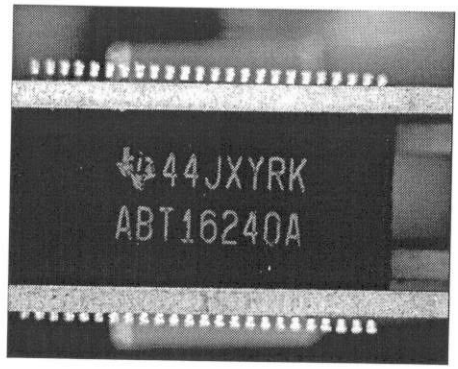
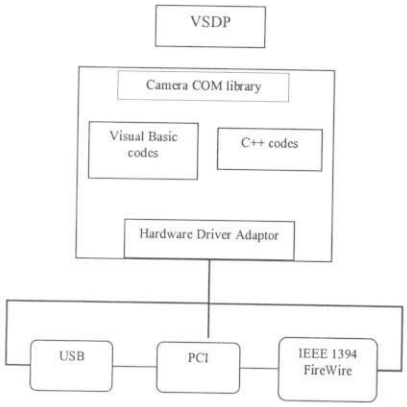


Image from machine FOV

Image Acquisition

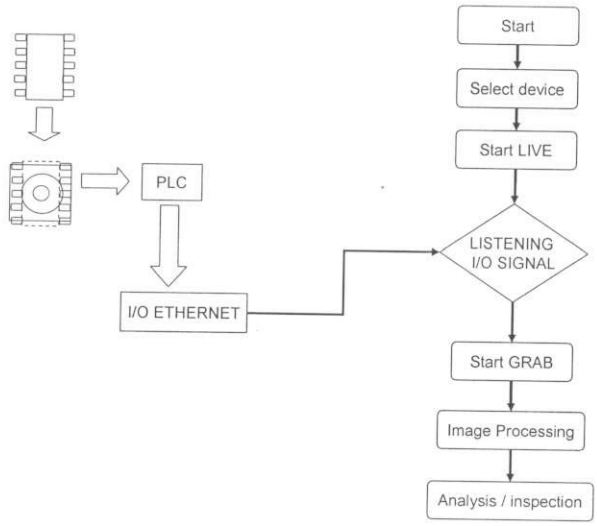


- Image acquisitions controls:
  - Live mode
  - Grab mode
  - End Live mode
    - Camera End Now (No blocking)
    - Camera End When Done (after number of frames have been captured)
- VSDP COM library for controlling acquisition:
- Image acquisition configuration:

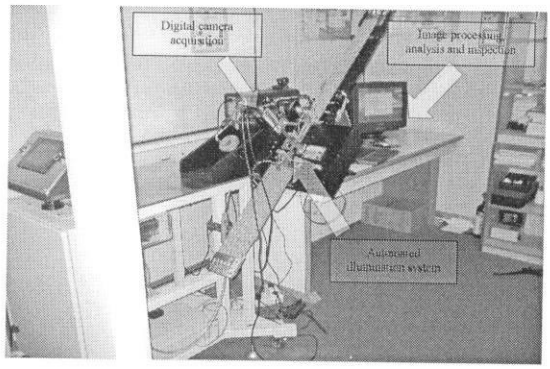
Camera specifications for testing

- Camera : JAI
- Acquisition board: Euresys Domino frame grabber.
- Direct X support = yes

Acquisition control



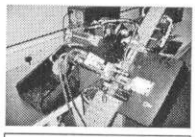
Briefs on Inspection Handler Specifications



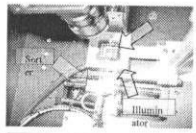
The system comprises of:

- Automated illumination system
- Digital image acquisition system.
- Image processing and;
- Feature extractions and inspection.
- Automated inspection handler machine.

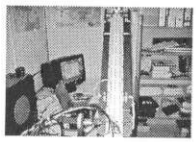
Machine Features



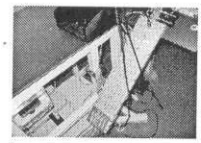
Camera, illuminations mounted on the body where the singulator and inspection zone is situated



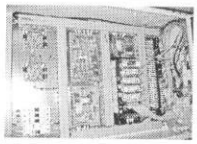
Close-up of the inspection zone. The IC is marked with yellow arrow.



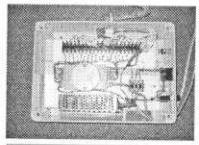
The input buffer



Output/Collecting buffers

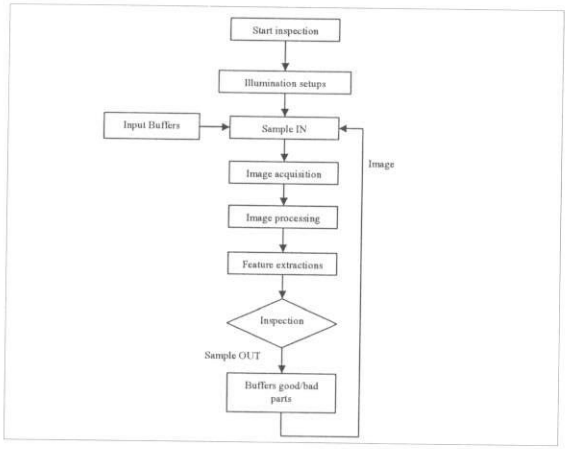


The power supply and PLC control peripherals.



ADAM Ethernet I/O communication circuit.

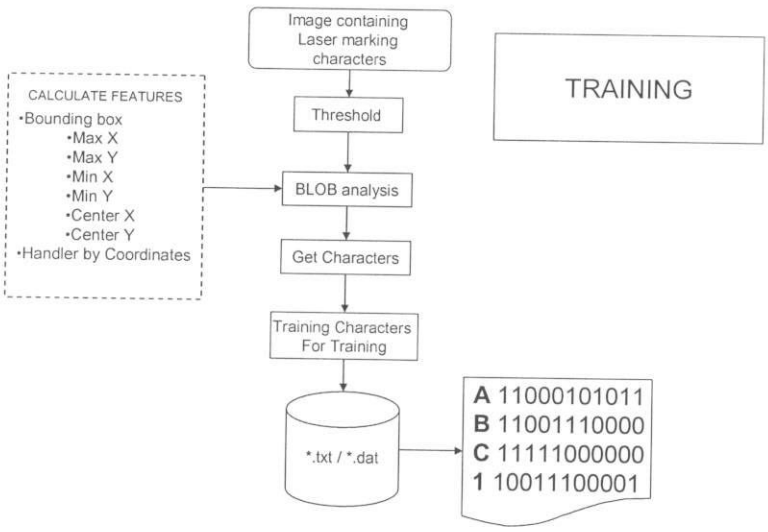
METHODS OF INSPECTION BY USING VISUAL INSPECTION HANDLER MACHINE



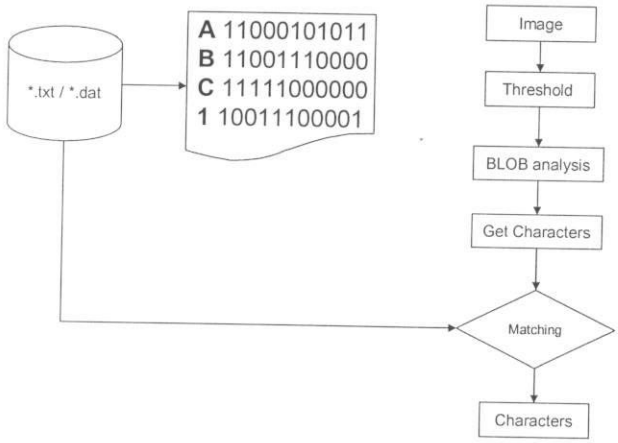
OCR for Marking Inspection

- The OCX for Optical Characters Recognition (OCR) is installed and ready to be tested.
- The OCX & DLL finished in development → 22nd April 2005
- VsOCROCX.dll & VsOCR.dll.
- Can be run for both Visual C++ & Visual Basic development
- First testing → Good result.

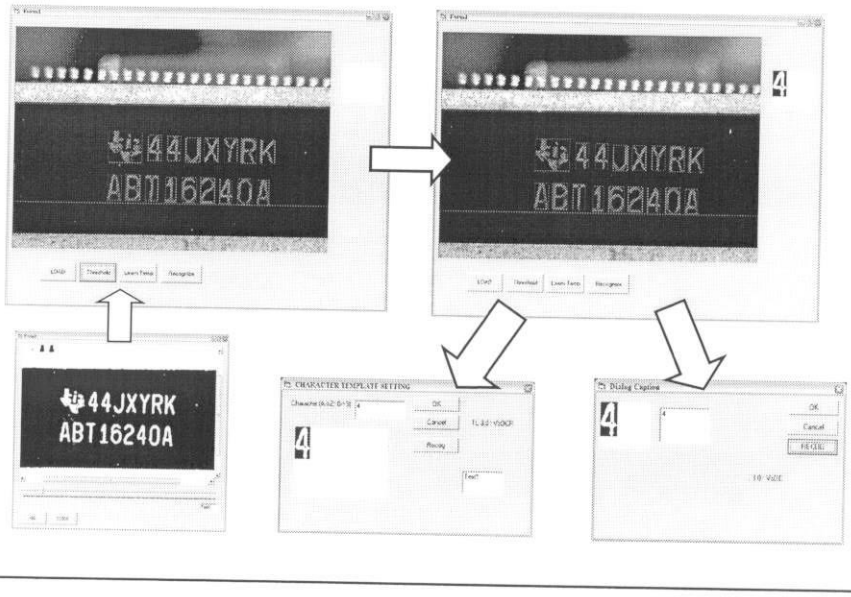
Methodology of VSDP OCR functions for Marking Inspection



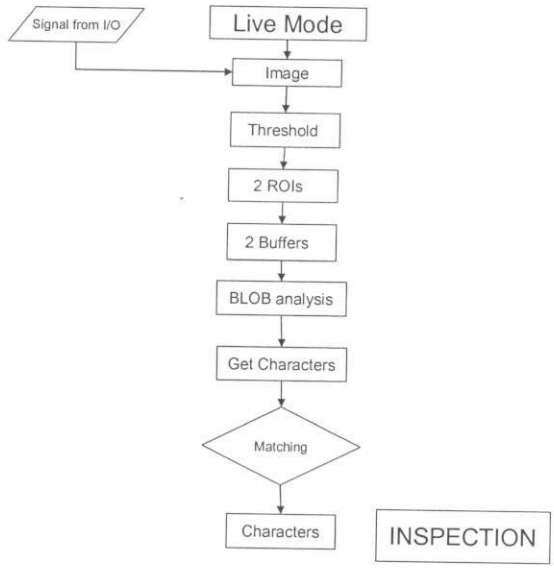
Methodology of VSDP OCR functions for Marking Inspection



OCR For Marking Inspection



OCR ON-LINE IMPLEMENTATION



PLC-PC COMMUNICATION*

- Communication is made possible by using I/O communication.
- I/O devices used: ADAM Ethernet I/O.
- Connection between the I/O to the PLC: 7 inputs and 5 outputs
- Inputs and outputs are for controlling routines such as:
  - Triggering image acquisitions and inspection when an IC hits the light sensor in the singulator.
  - Assigning automated/manual override for inspection.
  - Assigning buffers for collecting IC.

I/O system specifications *

- ADAM Ethernet Digital I/O.
  - Model 6050
  - 18 digital I/O channels
  - I/O type: 12 Inputs & 6 Outputs
  - Digital Input: Dry Contact:
    - Logic level 0: Close to GND
    - Logic level 1: Open
  - Digital Output:
    - Open Collector to 30V
    - 200 mA max. load
    - Optical Isolation: 2000VRMS
  - Power Consumption: 2 W (Typical)

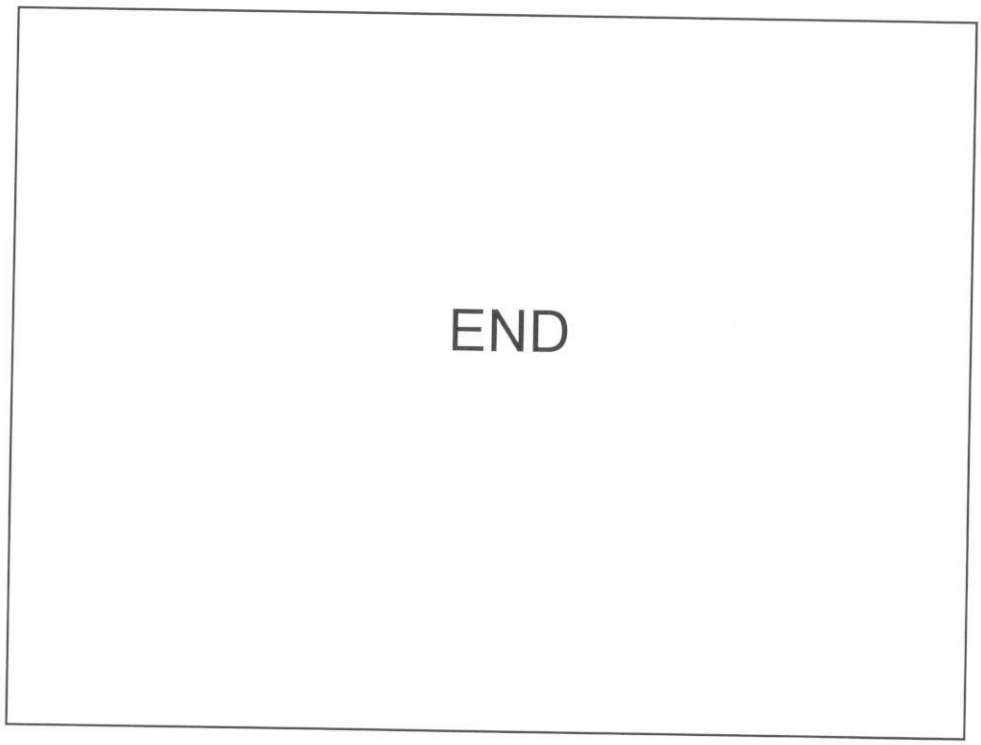
PROJECT 2
Application: Semiconductor Quality Inspection

- Semiconductor Quality Inspection Analysis Reports - Nazri (1 student)
  - Package Inspection - Zahurin
  - Die Inspection - Rajeswari
  - Lead Inspection – Momoh/Nassim
  - Marking (Character) Inspection - Ishak
  - Marking (Symbol) Inspection - Nagarajan

  EMAILS – MK

- Semiconductor Handling Machine (SHM) – Nazri/Ridzuan (1 student)
  - Design specs and features
  - User Manual

- Report on Integration of VSDP with SHM for Semiconductor Quality Inspection and Analysis – Nazri/Fairol (1 student)
  - Description on Machine-VSDP Communication protocols
  - Pattern Recognition modules (Neural networks)
  - Content-based Image Retrieval - Jonathan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