DIGITAL MODELLING TEST TECHNIQUE FOR MIXED MODE CIRCUITS

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A thesis submitted in fulfilment of the
requirements for the award of the degree of
Master of Engineering (Electrical)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

JUNE 2005

Specially dedicated to

My beloved parents and sisters
My Xiao Tian Xin, Yen Nee

ACKNOWLEDGEMENT

I would like to express my deepest gratitude to Assoc. Prof. Dr. Abu Khari b. A'ain (my supervisor) and Dr. Soloman Max who gave me the guidance and supports I needed. Without their continued motivation and interest, this thesis would not have been the same as presented here.

Besides, I am extremely grateful to all the seniors, especially Mr. Ting Hua Nong and Miss Ooi Chia Yee. There are also indebted to technicians such as Kak Nurul, Kak Shuki, Kak Seri and others, whichever playing important roles on the thesis completion; especially to Kak Mas, who represents FKE for SPS to deal with all postgraduate matters.

Finally, I would also like to thank my fellow friends such as Ober, Tai Kuan, Zem Peng, Hwee Ling, Jon Fea and others who have provided me with their helps and views, and make this project a success.

ABSTRACT

Recent demands in mobile communications, process control, automotive ASICs and smart sensors has accelerated the mixed-signal market and escalated the importance of mixed-signal test development. Mixed-signal circuit or mixed mode circuit is normally tested separately based on their core function. However, there is no guarantee that such testing approach would ensure that the system would function perfectly as a single entity. The main objective of this research is to investigate the application of digital modelling testing technique on mixed mode circuits. Digital modelling test technique is a method in which the test vector is simplified as a digital test vector. The investigation examined the suitable defect models as well as test procedures. The research also investigates the effectiveness of employing power supply voltage control (PSVC) testing technique together with the digital modelling. The reason of this test approach is due to independent reports of the effectiveness of these two test techniques. The circuit under test in this work includes a second order Butterworth low pass filter, an ADC and an op-amp. These circuits were chosen to represents a family of mixed – analogue and digital circuits. For comparison purpose, the ADC was tested using code density or histogram test technique. An analysis at bias point is presented to highlight why certain defects are exposed while others are not. The overall results showed that digital modelling test technique is able to model and expose unified analogue and mixed-signal faults. This is supported by the results from testing on discrete and CMOS circuitries. PSVC test coupled with digital model and pulse sampling can increase fault coverage for digital modelling test technique. The main advantages of digital model are it can reduce test time and eliminate circuit partitioning test.

ABSTRAK

Keperluan kini dalam bidang telekomunikasi mudah-alih, kawalan proses, ASICs untuk automotif dan penggesan pintar telah mempercepatkan pasaran isyarat bercampur dan merangsangkan kepentingan bidang perkembangan pengujian isyarat bercampur. Litar isyarat bercampur atau litar mod bercampur adalah diuji secara berasingan mengikut kepada fungsi dasarnya. Bagaimanapun, kaedah pengujian ini tidak dapat memastikan bahawa sistem yang diuji akan berfungsi dengan baik seperti dalam satu unit. Objektif utama dalam penyelidikan ini adalah untuk menyiasat aplikasi teknik pengujian permodelan digit bagi litar isyarat bercampur. Teknik pengujian permodelan digit adalah satu penyelesaian dimana vektor-vektor pengujian disimpifikasi kepada vektor-vektor digit. Kajian ini memeriksa kesesuaian model kecacatan dan prosedur pengujian. Penyelidikan ini juga menyiasat keberkesanan dalam penggunaan teknik pengujian pengawalan voltan bekalan kuasa (PSVC) berserta dengan teknik pengujian permodelan digit. Ini adalah berdasarkan kepada laporan berasingan tentang keberkesanan kedua-dua teknik pengujian. Litar-litar dalam pengujian untuk kerja ini adalah termasuk penapis laluan rendah Butterworth peringkat kedua, penukar analog kepada digit dan penguat operasian. Litar-litar ini dipilih untuk mewakili keluarga litar bercampur – litar-litar analog dan digit. Untuk tujuan perbandingan, penukar analog kepada digit diuji menggunakan densiti kod atau teknik pengujian histogram. Analisis kepada titik bias dipersembahkan untuk menunjukkan kenapa sesetengah kecacatan dapat dikesan dan yang lainnya tidak. Keseluruhan keputusan menunjukkan bahawa teknik pengujian permodelan digit adalah berkebolehan untuk memodel dan mengesan kecacatan kesatuan litar analog dan isyarat bercampur. Ini disokong dengan keputusan pengujian litar diskrit dan CMOS. Teknik PSVC bersama-sama dengan permodelan digit dan persampelan dedenyut dapat meninggikan liputan kecacatan teknik pengujian permodelan digit. Kebaikan utama teknik pengujian permodelan digit adalah ia dapat menggurangkan masa pengujian dan menggelakan pengujian litar secara pengagihan.

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LIST OF SYMBOLS

ASIC	-	Application Specified Integrated Circuit
PGA	-	Programmable Gain Amplifier
GUI	-	Graphic User Interface
LPF	-	Low Pass Filter
ADC	-	Analogue to Digital Converter
DAC	-	Digital to Analogue Converter
PLL	-	Phase locked Loop Circuit
SoC	-	System on Chip
MCM	-	Multi Chip Module
DfT	-	Design for Test
BisT	-	Build in self Test
IEEE	-	Institute of Electrical and Electronics Engineer
SPICE	-	Simulation Program with Integrated Circuit Emphasis
VHDL	-	Verilog High Description Language
$V_{o\text{-}CM}$	-	Common-mode offset
V_{os}	-	Input offset voltage
PSS	-	Power supply sensitivity
ΔV_O	-	Rate of change output voltage
ΔPS^+	-	Rate of change positive power supply
ΔPS^-	-	Rate of change negative power supply
PSRR	-	Power supply rejection ratio
CMRR	-	Common-mode rejection ratio
G_{CM}	-	Common-mode gain (DC)
G_D	-	Differential gain (DC)
V_{CM}	-	Common-mode signal
I_{IH}	-	Input leakage current, logic high

I_{IL}	-	Input leakage current, logic low
V_{IH}	-	Input high voltage
V_{IL}	-	Input low voltage
V_{OH}	-	Output high voltage
V_{OL}	-	Output low voltage
I_{OH}	-	Output high current
I_{OL}	-	Output low current
I_{OSL}	-	Current flowing into the pin
I_{OSH}	-	Current flowing out of the pin
Re	-	Real part
Im	-	Imaginary part
$\tau(f)$	-	Group delay
$G_{cm}(f)$	-	Common-mode gain (AC)
$G_{diff}(f)$	-	Differential gain (AC)
X_{rl}	-	Channel's input
X_{lr}	-	Channel's output
ICN	-	Idle channel noise
INL	-	Integral Nonlinearity
DNL	-	Differential Nonlinearity
ω_o	-	Angular applied frequency
FFT	-	Fast Fourier Transform
I_{DDQ}	-	Quiescent current
I_{DDT}	-	Dynamic/Transient power supply current
PSVC	-	Power Supply Voltage Control
TRT	-	Transient Response Test
CV	-	Coefficient Variation
PRBS	-	Pseudorandom Binary Sequence
LFSR	-	Linear Feedback Shift Register
DM	-	Digital modeling
Op-Amp	-	Operational Amplifier
H(s)	-	Transfer function
K	-	Filter gain
ω_π	-	Natural frequency

Q	-	Quality factor
ξ	-	Damping ratio
Y	-	Detectable
N	-	Not detectable
D	-	Drain open
S	-	Source open
G	-	Gate open
**	-	No repetition
D-S	-	Drain and Source terminal short
G-D	-	Gate and Drain terminal short
G-S	-	Gate and Source terminal short
^	-	Fault detected at (500.06-500.24) us
Θ	-	Fault detected at (1.00002-1.00015) ms
@#	-	Analogue modules (resistor and comparator)
&#	-	Digital module (priority encoder)

LIST OF APPENDICES

LIST OF PUBLICATIONS

NO.	TITLE
1	Leong Mun Hon and Abu Khari bin A'ain. Simple Analogue Active Filter Testing Using Digital Modelling. *Proceeding of the 2003 Third Student Conference on Research and Development (SCOReD 2003)*. August 25-26, 2003. UPM, Malaysia: IEEE. 2003. ELE-5/6.
2	Leong Mun Hon and Abu Khari bin A'ain. An Investigation on ADC Testing Using Digital Modelling. *Proceedings of the 2004 IEEE Region-10 Conference (TENCON 2004)*. November 21-24, 2004. Ching Mai, Thailand: IEEE. 2004. 245-249.
3	Leong Mun Hon and Abu Khari bin A'ain. Digital Modelling for Op-Amp Circuit Testing. *Proceeding of the 2004 International Conference on Semiconductor Electronics (ICSE 2004)*. December 7-9, 2004. UKM, Malaysia: IEEE. 2004. 538-541.

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

The trend towards the implementation of entire systems on chip and growing markets in mobile communications, process control, automotive ASICs and smart sensors has accelerated the mixed-signal market and escalated the importance of mixed-signal test development.

A mixed-signal circuit, or in generally mixed mode circuit, is defined as a circuit consisting of both digital and analogue elements in a single entity. Examples of basic mixed mode realm are CMOS analogue switch, programmable gain amplifier (PGA), analogue-to-digital converter (ADC), digital-to-analogue converter (DAC), phase-locked-loop (PLL), and other complex mixed mode circuits such as System-on-Chip (SoC), Application Specific Integrated Circuit (ASIC) and Multi-chip Module (MCM).

For the current IC trend - increase in the number of circuit nodes and circuit complexity, Design-for-Test (DfT) becomes the mainstream of mixed-signal test development in order to reduce test cost due to test pin limited. There are a variety of DfT and BisT techniques proposed for different mixed mode circuits. One of the current issues is to provide a consistent and structured framework for system-level and board-level test development, and for DfT approaches. Hence, IEEE 1149.4-1999 was born.

Nowadays, many high density and complex mixed mode circuits, for example SoC and MCM, come out with built-in boundary scan path as defined by IEEE 1149.4-1999 (Mixed Signal Test Bus Standard). Under this standardization, digital and analogue circuits are separately in testable modules, called Digital Boundary Module (DBM) and Analogue Boundary Module (ABM). All of these modules enclosed by internal and external test path, and external access by separate test pin. Actually, this standard is a complementary of IEEE 1149.1-1990, and gains extra features (such as ABM, the analogue test bus, an extended Test Access Port (ETAP) and controller, and various register for analogue test bus operation). Figure 1.1 shows the ABM for an analogue pin [1], and Figure 1.2 shows IEEE P1149.4 basic chip structure [2].

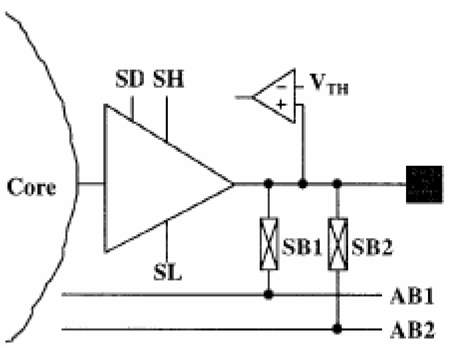

Figure 1.1: ABM of an output pin

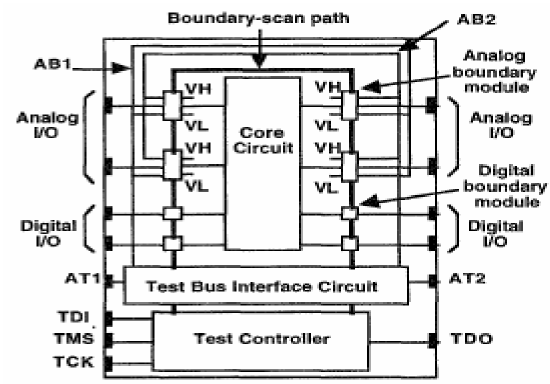

Figure 1.2: Chip structure

However, for those basic cores of mixed mode circuit, such as ADC, DAC, PLL and PGA, each realm has its own test technique differently implemented to and seldom compliance with 1149.4 cells. For example ADC, the conventional test technique used commonly at industry is Code Density test technique or simply Histogram test. Besides, there is still a lot of mixed-signal ASICs that do not facilitate with boundary scan due to trade off with area overhead.

Although analogue circuits such as filter and Op-Amp are widely used in the market and possessed with their own separated conventional functional test (specification-oriented testing), it is much more complex for test development with the same implementation when the input and output share the same signal transmission in mixed mode environment.

In today's highly competitive semiconductor world, it is critical to reduce the actual test time on expensive automatic test equipment (ATE). Test time on high-end mixed-signal tester costs about three to five cents per second [3]. Due to this, most commercial mixed mode ICs are tested by separate testers (digital tester and analogue tester). Mixed-signal tester generally comes in variety of architectures and test routines depend on vendors due to competitive advantage in the market. However, many of these testers consist of useful features that are common among each other.

Test simulation and defect-oriented testing are the two among other cost saving test methodology emerging trends for mixed-signal IC [4]. Test simulation promises the ability to simulate and debug the test program for tester and CUT developed by SPICE, VHDL or others software-modelling languages before actual silicon CUT is received. Defect-oriented testing is based on the mathematical analysis and software modelling of a circuit major failure mechanism that expose the failures in a limited set of measured parameters [4]. Both of these methods not only cut down the production test cost, but also accelerate the time to market for certain product.

Because of a lot of information can be abstracted directly from transient response of a CUT, test researchers work with transient response almost for a decade [5–10], they proposed that analogue and mixed mode CUTs could be unified test by Transient Response analysis with Pseudo Random Binary Sequence (PRBS). The output data are then analyzed and processed using mathematical calculation, such as Sample values, Rate of change, Auto-correlation and Cross-correlation and Response Digitisation. Further studies and researches on Transient Response analysis can be found in [11–22]. They proposed a DfT method - Interface Scan bus in CUT in order to increase fault coverage especially for particular fault. Besides, they categorized any detectable fault using generated Index Functionality from cross-correlation function for the CUT.

1.2 Problem Statement

The number of mixed-signal circuit blocks of an IC is getting more and more. High-density CMOS transistors and limited pin count in mixed-signal chips become a test challenge to semiconductor industry. This will either increase time-to-market or face the risk of decrease quality during early production.

DfT and BisT approach are getting popular in many testing arena. However, with the extra pin overhead and add in extra register, for example DfT approach, cost development increase and die space become limited for application. Besides, for example in BisT approach, extra bus and block partitioning is needed. Then, analogue block and digital block have to be tested separately, and this includes also block interface testing. All of these increases production cost if production volume is in medium or lower scale. According to [23] and [24], the IC designs with a 200 μm pad-pitch, pad limited layout and no boundary scan, adding IEEE P1149.4 test bus and controller will increase the cost by 15-30%, especially for low cost mixed mode ICs (< $2) and low pin count (< 60 pins) ICs will increase the design cost dramatically.

In semiconductor industries, cost for a mixed-signal tester in the market is very expensive compared to digital tester or analogue tester alone. Test time increases if customer tests their product using both analogue and digital testers concurrently. Normally, this ATE is in giant size and not portable. This lead to profit losing if opponent can reach to market earlier. However, most IC industries are accommodated with digital tester. A defect-oriented testing technique, which facilitate the mixed-signal test with minimum modification or make use of digital tester, will be welcomed.

Therefore, the main questions being addressed in this research work are:

a) Is it possible to integrate analogue and digital test as a single entity?
b) Would digitally modelled analogue test help to ease mixed mode test?

1.3 Objective

The objectives of this project are:

a) To facilitate mixed mode circuit test using digital modelling of analogue circuits.
b) To study the feasibility of introducing digital modelling coupled with other test techniques to ease mixed mode test.

1.4 Goal

The goals of the project are:

a) To investigate the effectiveness of digital modelling.
b) To detect faults in mixed mode circuit in transient domain.
c) To unify tests of mixed mode circuit.

1.5 Scope

The scope of the project is as listed below:

a) To study the idea of digital modelling for analogue circuit.
b) To study the idea of Power Supply Voltage Control test technique.
c) To study and analyse characteristics of analogue active filter in discrete level.
d) To test a second order Butterworth low pass filter based on experimental and simulation using digital modelling coupled with Power Supply Voltage Control test technique.
e) To test a flash ADC using digital modelling and Power Supply Voltage Control test techniques, and compare the result to Code Density or Histogram test technique.
f) To test a CMOS Op-Amp at transient level and AC Sweep by digital modelling coupled with Power Supply Voltage Control test technique.

1.6 Thesis Layout

Basically, this thesis can be divided into five chapters as stated below

a) Introduction
b) Literature review
c) Research methodology
d) Results and discussion
e) Conclusion, future work and suggestion

The first chapter gives a brief description of the work and thesis. It includes explanation on mixed-signal background and motivation, as well as the project objectives, goals and scopes.

In the second chapter, the importance of mixed-signal testing and digital modelling test technique is described as well as the different between functional test and parametric test. Literature review on defect oriented tests and, some conventional analogue and mixed-signal parametric tests are also discussed in this chapter. Histogram test, which special to ADC- mixed mode circuit, is also briefly described in this section.

The methodology of the overall project is explained in detail in chapter three. The project approach as well as simulation using PSpice^{TM} is described. Three CUTs as sample study are presented in this chapter. For discrete analogue filter test, explanation is given on how to set up the experimental work that include setting up the equipment, as well as simulation work. Simulation an Op-amp and 3-bit flash ADC are carried at CMOS transient level. Explanation on how to conduct the test in simulation is discussed.

In chapter four, result as well as discussion for the CUT are discussed and analysed. Selected transient and frequency response for discrete analogue filter will be looked in detail. For flash ADC, transient response and bias point analysis as well as Histogram test will be discussed. CMOS bias point for Op-amp as well as transient and frequency response will be collected and analyse. The bias point analysis is based as MATLAB™ test program. All the results, which digital model coupled with PSVC technique, are also collected and will be analysed in this chapter.

Finally, in the last chapter, Chapter five, a conclusion will be drawn along with the suggestion for future development in this subject.

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