CAD SOFTWARE FOR SEMICONDUCTOR DEVICE MODELING

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Specially dedicated to family and friends
who had been supporting me all the while

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I would like to thank my supervisor for allowing and supporting me to explore my own direction for this project. It has opened to me a new area with many possibilities.

ABSTRAK

Pembinaan model untuk bahan semikonduktor adalah bertujuan untuk memahami dan mendalami sifat bahan tersebut. Bidang penyelidikannya merangkumi pembinaan model bahan yang baru hinggalah ke pembinaan perisian yang boleh mensimulasikan model tersebut dengan menggunakan komputer. Perisian itu juga dikenali sebagai "Device CAD" dan ianya telah dipilih sebagai asas penyelidikan tesis ini. Pembinaan model yang paling tepat bagi sesuatu bahan itu boleh dicapai dengan penggunaan model fizikal. Teknik ini menggunakan persamaan matematik sebagai asas pembinaan model untuk dianalisa. "Device CAD" yang menggunakan teknik ini tidak mudah didapati malah mahal harganya. Objektif penyelidikan ini adalah untuk membina perisian tersebut dengan menggunakan model fizikal. Ianya telah direkabentuk dengan berorientasikan objek menggunakan bahasa pengaturcaraan C++ berserta kelas-kelas Antaramuka Pengguna Bergrafik (GUI toolkit). Kerja-kerja yang dijalankan didalam penyelidikan ini mencakupi penyelidikan keatas model fizikal bagi simpang PN, BJT dan MOSFET berserta dengan kerja-kerja penyelidikan untuk membina perisian tersebut. Sebagai hasilnya, sebuah perisian yang mempunyai Antara Muka Bergrafik telah dibina. Ianya mampu untuk mensimulasikan model bahan yang telah dipilih dan keputusannya dipaparkan dalam bentuk graf 2D. Parameter model yang tidak tetap boleh diubah sebelum melakukan simulasi. Perisian ini boleh dijadikan sebagai titik permulaan bagi pembinaan perisian bertahap tinggi untuk menganalisa bahan atau litar.

ABSTRACT

Semiconductor device modeling is concerns with understanding and modeling the behaviour of semiconductor device. Its research area spans from new device model development to building Computer-Aided-Design (CAD) software that implements the model in computer. The software is also known by the term Device CAD. This is the research area of this thesis. The best accuracy of modeling can be obtained through physical modeling. In this technique, mathematical equations representing the device physically are used for analysis. Device CAD that uses this technique is not freely available and costly. The aim of this research is to develop the CAD software by using the physical modeling approach. The software is design based on object-oriented methodology by using C++ programming language and graphical toolkits. Work involves in this project includes research on physical models for PNJ Junction, BJT and MOSFET as well as research and implementation of the software. As a result, a software with graphical user interface has been developed. It is able to simulate chosen model for target device and display it as a 2D characteristic plot. Any non-constant parameter for each model can be modified prior to simulation. The software can be a starting point towards a full-fledged device or circuit analysis tools.

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LIST OF SYMBOLS/ABBREVIATIONS

J	-	Electric current density
J_s	-	Ideal reverse bias saturation current density
e	-	Electron charge magnitude
V_a	-	Forward bias voltage
V_{BE}	-	Base-emitter voltage
V_{BC}	-	Base-collector voltage
V_{bi}	-	Built-in potential barrier with zero applied bias
k	-	Boltzmann constant
T	-	Temperature
N_a	-	Density of acceptor impurities atom
N_d	-	Density of donor impurities atom
n_i	-	Intrinsic concentration of electrons
V_t	-	Thermal voltage
w	-	Space charge width
ε_s	-	Permittivity
ε_r	-	Relative permittivity
ε_o	-	Permittivity of free space

$\delta n_B(x)$	-	Excess electron concentration in n-type base
$\delta p_E(x)$	-	Excess hole concentration in p-type emitter
$\delta p_C(x)$	-	Excess hole concentration in p-type collector
n_{B0}	-	Thermal-equilibrium minority carrier electron concentration in base
p_{E0}	-	Thermal-equilibrium minority carrier hole concentration in emitter
p_{C0}	-	Thermal-equilibrium minority carrier hole concentration in collector
x_B	-	Neutral base region width
x_E	-	Neutral emitter region width
x_C	-	Neutral collector region width
x	-	Width within x = 0 and x = x_b
x'	-	Width within x = 0 and x = x_e
x''	-	Width within x = 0 and x = x_c
L_c	-	Minority carrier diffusion length in collector regions
x_{dT}	-	Maximum space charge width at inversion transition point
Φ_{fp}	-	Potential difference magnitude between intrinsic Fermi energy (E_Fi) and Fermi energy (E_F) in p-type semiconductor
Φ_{ms}	-	Metal-semiconductor work function difference
Φ'_m	-	Modified metal work function, the potential required to inject an electron from the metal into the conduction band of oxide
χ'	-	Modified electron affinity
Q'_{ss}	-	Equivalent trapped oxide charge per unit area
E_g	-	Band gap energy
V_{fb}	-	Flat band voltage
C_{ox}	-	Oxide capacitance

t_{ox}	-	Gate oxide thickness
E_c	-	Conduction energy band
E_v	-	Valence energy band
p	-	p-type semiconductor
n	-	n-type semiconductor
E	-	emitter
B	-	base
C	-	collector
I_E	-	emitter current
I_c	-	collector current
APLAC	-	Analysis Program for Linear Active Circuits
API	-	Application Programming Interface
BJT	-	Bipolar Junction Transistor
CAD	-	Computer Aided Design
FET	-	Field Effect Transistor
MOSFET	-	Metal Oxide Semiconductor FET

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CHAPTER 1

INTRODUCTION

Semiconductor industry is largely driven with the obsession to fit more transistors into a chip area. Number of transistors roughly double every 18 months in accordance to what is known as Moore's Law [1]. As shown in Figure 1.1, the number of transistors per chip embedded within a 64Mb DRAM memory almost reach 100 million transistors. To cope with ever increasing design complexity, circuit design engineer turns to Computer Aided Design (CAD) tools.

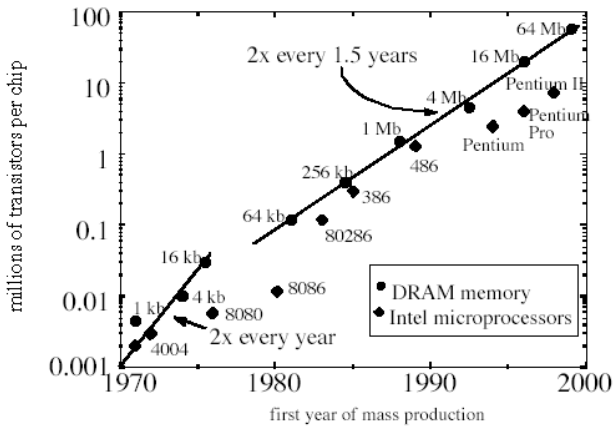

Figure 1.1 Moore's Law effects

Circuit design tool in turn relies on device model to give it an accurate representation of the working of semiconductor device in the real world. Commercial sofware such as Spice [2] includes various device models such as diode, transistors (BJT, MOSFET, GaAsFET, etc) that can be embedded within a circuit model for simulation. Device model is also use in device simulator that allows device engineer to better visualize effects of physical variations on electrical properties of the device before actual fabrication process. Hence device model is a link to physical world for all the CAD tools. Figure 1.2 illustrates the interrelation.

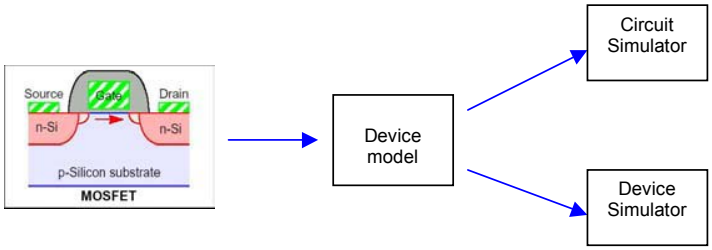

Figure 1.2 Device modeling

An implication of Moore's Law is also that devices are getting smaller. . That is device scaling is what enables the Moore's Law accuracy. Therefore another direct implication of this is an increase in cost of device fabrication. Figure 1.3 shows that a fabrication plant cost exceed 1 billion USD in leading to year 2000. The cost includes the cost for verification and validation of the device. Hence it is imperative that device engineer understand how the devices function to ensure proper performance, reliability and its economic implications. Scaling used to be relatively straightforward but today, it also involves new materials and increased complexity resulting in greatly increasing cost. This greatly underlies the importance of device modeling.

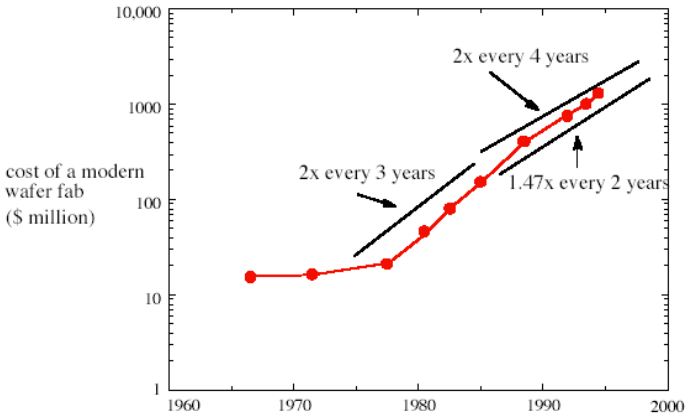

Figure 1.3 Fabrication cost effect as transistor size decreases

Device model can be integrated into the CAD tools in two ways. [3] defined the methods as physical model approach and macromodel approach. Physical modeling of device is based on device physics express in mathematical equations as basis for simulation. Macromodel on the other hand uses empirical based technique. This method makes use of generic device model coupled with subcircuit for simulation. Empirical means the devise model parameters are mainly derived based on measurement and experimentation result rather than theory**.** An example of macromodel is device model implementation in SPICE.

Despite of the advantages inherent in macromodel approach, as it shall be seen later, devise modeling through physical model approach offers superior accuracy. The accuracy factor is becoming much more critical in the advent of high power, high frequency and nanometer semiconductor devices. As concluded by [4], as the devices become more complex, device simulation through physical model is not only essential but also crucial.

1.1 Project Objectives

This project aims to create a software that can simulate semiconductor devices based on physical model. The CAD software to be developed incorporates the device mathematical equations. Its basic function is to enable user to investigate device behaviour through parameter modification and characteristic observation. Simulation result shall conform to theoretical analysis of the device models. The project objectives are then divided into two main areas.

The first objective is to design, develop and test a device simulator software. Besides allowing user to investigate the device behaviour, the software will also allows for relatively easy inclusion of new device model. Relatively easy means that adding new model does not requires major overhaul in the software design. To facilitate ease of use, the software will have a graphical user interface (GUI). The second objective is to include physical models of three main semiconductor devices. The devices are PN Junction, Bipolar Junction Transistor and Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). For each device, three physical models will be implemented.

1.2 Project Scope

This project will not produce any new theoretical physical device model instead it will use existing model for incorporation into the software. It will enable user to modify non-constant parameters of device equation used in simulation and it will present device simulation result in 2D characteristic plot. The physical models chosen for each device are

- PN Junction
  - Ideal Current-Voltage Characteristic (J)
  - Built-in potential barrier (V_{bi}) under equilibrium
  - Space charge width (w) under equilibrium

- Bipolar Junction Transistor
  - Excess minority carrier concentration under forward active mode in base, emitter and collector regions ($\delta n_b(x)$, $\delta p_e(x)$, $\delta p_c(x)$) of NPN BJT

- MOSFET
  - Maximum space charge width (x_{dT})
  - Metal semiconductor work function difference for p-type substrate (ϕ_{ms})
  - Flat band voltage for p-type substrate (V_{FB})

To achieve all the project's objectives, knowledge in the following is necessary

- Commercial device and circuit modeling software like APLAC, Orcad's PSPICE etc
- Theoretical concept of the semiconductor devices and the selected physical models
- Device modeling requirements
- Software development process
- High-level language and software development tool
  - C++, Microsoft Visual C++ Version 6.0, Qt Graphical Library, Qwt Technical Graphical Library

1.3 Thesis Outline

This chapter (Chapter 1) provides an introduction on what is device modeling, its importance and the two main approaches taken for device modeling. Chapter 2 investigates more on device modeling software and future technology challenges. Chapter 3 presents the device model to be implemented into the software. The chapter discusses the theoretical concept behind each model and what parameters to be simulated.

This is followed by discussion on software implementation in Chapter 4. It includes explanation on the software development approaches, methods taken to validate the result and also discussion on how to include new device model. Chapter 5 presents discussion on the simulation result of the software against its theoretical concept along with the project conclusion and recommendations for future works. The mathematical equations, simulation related information and source code listing of the software are attached in appendices.