

THE DESIGN AND SIMULATION OF 8×1 PASSIVELY QUENCHED SINGLE
PHOTON AVALANCHE DIODE (SPAD) ARRAY

AZMAN BIN MOHAMED EUSOFF

UNIVERSITI TEKNOLOGI MALAYSIA

THE DESIGN AND SIMULATION OF 8×1 PASSIVELY QUENCHED SINGLE
PHOTON AVALANCHE DIODE (SPAD) ARRAY

AZMAN BIN MOHAMED EUSOFF

A project report submitted in partial fulfilment of the
requirements for the award of the degree of
Master of Engineering (Electrical - Computer and Microelectronic System)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

JUNE 2013

*Specially dedicated to my beloved family, lecturers and friends
for the guidance, encouragement and inspiration
throughout my journey of education*

ACKNOWLEDGEMENT

First and foremost, I would like to take this opportunity to express my deepest gratitude to my project supervisor, Dr. Suhaila Isaak for her great encouragement, guidance and sharing of knowledge during the process of completing this project. Without her constant motivation and supervision with valuable suggestion, this project would not been a success.

In addition, I wish to thank my postgraduate course-mates for their cooperation and information sharing in completing this project. Yet, not to forget my fellow friends for their care and moral support when it was most required.

Last but not least, my highest appreciation goes to my beloved family for their understanding and blessing from the beginning up to now. Special thanks to my wife, Mrs. Saliza Rozelee, who always been there and stood by me through the good and bad times. The precious support and encouragement will be fondly remembered.

ABSTRACT

This project report reports the development of The design and simulation of 8×1 passively quenched Single Photon Avalanche Diode (SPAD) array. This research is covered on the development and characterization of a passive quenching circuit by using Silterra 180nm CMOS technology. The main motivation of this research is to design a passive quenching circuit using thin gate devices with low voltage technology design on-chip with 4-bit counter to improve the counting rate. Hence, the passive quenching circuit design on-chip would enable the capability to perform at higher speed which is more than 100MHz. The simulation and design of the passive quenching circuit will be accomplished using CADENCE tools. To perform the simulation of a passive quenching circuit in Cadence, Single Photon Avalanche Diode (SPAD) simulation model circuit is adopted and designed in CADENCE Virtuoso Schematic to generate the photon detector signal to the passive quenching circuit. The simulation characterization is implemented on single SPAD pixel and 8×1 SPAD array. The dead time for a single pixel is 9.524ns. Therefore, the circuit would promise at high frequency rate at 106MHz.

ABSTRAK

Tesis ini melaporkan mengenai penyelidikan tentang “*The design and simulation of 8×1 passively quenched Single Photon Avalanche Diode (SPAD) array*”. Kajian ini meliputi kepada penyelidikan dan pencirian litar “*quenching*” pasif dengan menggunakan teknologi CMOS Silterra 180nm. Motivasi utama kajian ini adalah untuk mereka bentuk litar “*quenching*” pasif menggunakan peranti “*thin-gate*” dengan reka bentuk teknologi voltan rendah pada cip dengan kaunter 4-bit untuk meningkatkan kadar pengiraan foton. Oleh itu, reka bentuk litar “*quenching*” pasif pada cip akan membolehkan keupayaan untuk dilaksanakan pada kelajuan yang lebih tinggi melebihi frekuensi 100MHz. Simulasi dan reka bentuk litar “*quenching*” pasif akan dicapai menggunakan perisian CADENCE. Untuk melakukan simulasi litar “*quenching*” pasif dalam perisian CADENCE, “*Single Photon Avalanche Diode*” (SPAD) perlu dimodelkan dengan terperinci untuk hasil simulasi yang tepat dan direka dalam *CADENCE Virtuoso Schematic* untuk menjana isyarat pengesan foton kepada litar “*quenching*” pasif. Pencirian simulasi dilaksanakan pada piksel SPAD tunggal dan piksel SPAD bersiri 8×1. “*Dead time*” piksel tunggal ialah 9.524ns. Oleh itu, litar “*quenching*” pasif djanjikan boleh beroperasi pada frekuensi yang tinggi iaitu pada kadar 106MHz.

TABLE OF CONTENTS

| CHAPTER | TITLE | PAGE |
|----------|--|------|
| | DECLARATION | ii |
| | DEDICATION | iii |
| | ACKNOWLEDGEMENT | iv |
| | ABSTRACT | v |
| | ABSTRAK | vi |
| | TABLE OF CONTENTS | vii |
| | LIST OF TABLES | ix |
| | LIST OF FIGURES | x |
| | LIST OF ABBREVIATIONS | xiii |
| | LIST OF APPENDICES | xiv |
| 1 | INTRODUCTION | 2 |
| | 1.1 Project Objective | 3 |
| | 1.2 Scope Of Work | 4 |
| | 1.3 Project report Outline | 4 |
| 2 | LITERATURE REVIEW | 5 |
| | 2.1 Spad Operation | 5 |
| | 2.1.1 Geiger Mode | 6 |
| | 2.1.2 SPAD Circuit Model for Simulations | 6 |
| | 2.2 Passive Quenching Circuit | 9 |
| | 2.3 QUENCHING, RECHARGE AND Dead time | 11 |

| | | |
|----------|--|----|
| 3 | RESEARCH METHODOLOGY | 13 |
| 3.1 | The Overall Circuit | 13 |
| 3.2 | Single Pixel Array Circuit | 14 |
| 3.3 | quenching circuit | 15 |
| 3.4 | Spad Model | 16 |
| 3.5 | Pulse Discriminator Circuit | 17 |
| 3.6 | 4-bit counter | 18 |
| | 3.6.1 D Flip-Flop | 20 |
| 3.7 | Multiplexer (MUX) | 23 |
| | 3.7.1 Pass Gate | 25 |
| 3.8 | Address Decoder | 25 |
| 4 | DESIGN IMPLEMENTATION & RESULTS | 27 |
| 4.1 | Design Implementation | 27 |
| | 4.1.1 Single Pixel Array Circuit | 27 |
| | 4.1.2 SPAD Model | 28 |
| | 4.1.3 Quenching Circuit | 31 |
| | 4.1.4 Pulse Discriminator | 34 |
| | 4.1.5 4-bit Counter | 35 |
| | 4.1.6 8to1 Multiplexer | 41 |
| | 4.1.7 3to8 Decoder | 44 |
| 4.2 | Results | 44 |
| 5 | CONCLUSION AND FUTURE PROPOSAL | 48 |
| 5.1 | Conclusion | 48 |
| 5.2 | Future Proposal | 49 |
| | REFERENCES | 50 |

LIST OF TABLES

| TABLE NO. | TITLE | PAGE |
|------------------|---|-------------|
| 4-1 | Dead time (t_d) and operating frequency with different V_{bd} | 30 |
| 4-2 | Quenching circuit specification | 34 |

LIST OF FIGURES

| FIGURE NO. | TITLE | PAGE |
|------------|--|------|
| 2.1 | Basic SPAD model | 7 |
| 2.2 | The electro-optical model by Stoppa et al. [19] | 8 |
| 2.3 | Basic passive quenching circuit (left) and traditional SPAD model (right). The transistor switch mimics the avalanche triggering | 9 |
| 2.4 | Configuration of passive quenching circuit | 10 |
| 2.5 | Voltage pulse for passive quenching SPAD | 12 |
| 3.1 | Overall schematic view for 8×1 Passively Quenched Single Photon Avalanche Diode (SPAD) Array with a 4-Bit Counter | 14 |
| 3.2 | Single pixel array circuit | 15 |
| 3.3 | Passive quenching circuit | 16 |
| 3.4 | SPAD model | 17 |
| 3.5 | Pulse discriminator circuit | 18 |
| 3.6 | Pulse discriminator symbol | 18 |
| 3.7 | 4-bit counter symbol | 19 |
| 3.8 | 4-bit counter using D flip-flop | 19 |
| 3.9 | Schematic view for D flip-flop | 20 |
| 3.10 | Symbol view for D flip-flop | 20 |
| 3.11 | 2-Input Nand gate (a) Schematic view (b) Symbol view | 21 |
| 3.12 | 2-Input Nand Truth Table | 21 |
| 3.13 | 3-Input Nand gate (a) Schematic view (b) Symbol view | 22 |
| 3.14 | 3-Input Nand Truth Table | 22 |

| | | |
|------|--|----|
| 3.15 | Inverter (a) Schematic view (b) Symbol view | 23 |
| 3.16 | 8-to-1 multiplexer schematic view | 24 |
| 3.17 | 8-to-1 multiplexer symbol view | 24 |
| 3.18 | Pass Gate (a) schematic view (b) symbol view | 25 |
| 3.19 | 3-to-8 address decoder schematic view | 26 |
| 3.20 | 3-to-8 address decoder symbol view | 26 |
| 3.21 | Truth table for 3-to-8 decoder | 26 |
| 4.1 | Single array pixel circuit | 28 |
| 4.2 | SPAD model based on Dalla Mora[6] model | 29 |
| 4.3 | Quenching and recharge graph with different breakdown voltage | 30 |
| 4.4 | Passive quenching circuit with SPAD | 31 |
| 4.5 | Quenching and recharge graph for different transistor length | 32 |
| 4.6 | Quenching operation graph | 33 |
| 4.7 | Reference current, I_D in quenching circuit | 33 |
| 4.8 | Pulse discriminator circuit | 34 |
| 4.9 | Voltage transfer characteristic for pulse discriminator | 35 |
| 4.10 | 4-bit counter schematic | 36 |
| 4.11 | Simulation output on negative edge triggered counter | 36 |
| 4.12 | Edge triggered D flip-flop | 37 |
| 4.13 | Edge triggered D Flip-Flop simulation result | 37 |
| 4.14 | Inverter (a) schematic view (b) symbol view | 38 |
| 4.15 | Inverter simulation result | 39 |
| 4.16 | 2-Input Nand schematic and symbol | 40 |
| 4.17 | 2-input Nand simulation result with transistor mult=20 | 40 |
| 4.18 | 3-Input Nand schematic and symbol | 41 |
| 4.19 | 3-input Nand simulation result with transistor mult=20 | 41 |
| 4.20 | 8to1 multiplexer schematic (left) and symbol (right) | 42 |
| 4.21 | 8to1 multiplexer symbol | 43 |
| 4.22 | Single stage multiplexer | 43 |
| 4.23 | Mux input output delay result | 43 |
| 4.24 | 3-to-8 decoder schematic | 44 |
| 4.25 | Overall schematic | 45 |

| | | |
|------|--|----|
| 4.26 | Full circuit simulation result | 46 |
| 4.27 | Simulation result with SPAD input and multiplexer output | 47 |

LIST OF ABBREVIATIONS

| | | |
|--------|---|---|
| OTDR | - | Optical Time-domain Reflectometry |
| SPAD | - | Single Photon Avalanche Diode |
| NIR | - | Near Infrared |
| PMT | - | Photomultiplier Tubes |
| MCP | - | Multichannel Plates |
| CMOS | - | Complementary metal–oxide–semiconductor |
| APD | - | Avalanche Photodiode |
| AQRC | - | Active Quenching and Reset Circuit |
| MOSFET | - | Metal–Oxide–Semiconductor Field-Effect Transistor |
| SNR | - | Signal to Noise Ratio |
| IC | - | Integrated Circuit |
| FPGA | - | Field-Programmable Gate Array |
| MUX | - | Multiplexer |
| TG | - | Transmission Gate |
| CAD | - | Computer-aided design |
| CEDEC | - | Collaborative micro-Electronic Design Excellence Centre |
| USM | - | Universiti Sains Malaysia |
| VPN | - | Virtual Private Networking |
| VNC | - | Virtual Network Computing |
| UTM | - | Universiti Teknologi Malaysia |
| IT | - | Information Technology |
| OEM | - | Original Equipment Manufacture |
| IBM | - | International Business Machines |
| nm | - | nanometer |

LIST OF APPENDICES

No appendices attached.

CHAPTER 1

INTRODUCTION

In recent years, sensors capable of detecting single photons are required for imaging systems in, for example, astronomy, laser ranging, optical time-domain reflectometry (OTDR), single molecule detection, fluorescence decay and biomedical imaging[1]. In response to a single photon arriving, the detector must provide a high output signal due to an internal high multiplication mechanism to allow easy recognition of the event by subsequent electronic circuits. The Single Photon Avalanche Diode (SPAD) is operated in the Geiger mode where the applied reverse bias voltage (V_R) is greater than the breakdown voltage (V_{BD}) overcome the limitations of fragile, high voltage ($\sim 2\text{kV}$), and bulky devices with photomultiplier tubes (PMTs), and multichannel plates (MCPs). Silicon SPADs made in standard CMOS processes have been implemented and arrays of Silicon SPADs, integrated with readout electronics, have also been made for imaging applications [2].

CMOS SPAD detectors so far reported can be divided in two groups, according to the size of the depletion layer of the p-n junction. The depletion layer can be thin, typically $1\mu\text{m}$, or thick, from $20\mu\text{m}$ to $150\mu\text{m}$ [3, 4]. The main features of thin junction SPADs are breakdown voltage (V_{BD}) of 10-50V. They have a small active area, diameter between $5\mu\text{m}$ to $150\mu\text{m}$ and have fairly good quantum efficiency in the visible range, (45% at 500nm) but this declines to 32% at 630nm and to 15% at 730nm, they are still useful in NIR, where the quantum efficiency is

about 10% at 830nm and a few 0.1% at 1064nm. In comparison, thick junction silicon SPADs has a higher breakdown voltage V_B of 200-500V and a fairly wide active area, with diameter from 100 μm to 500 μm . The quantum efficiency is very high in the visible region; better than 50% over all the range from 540nm to 850nm wavelength, but declines in the NIR, but it is still about 3% at 1064nm.

1.1 PROJECT OBJECTIVE

The objective for this project is to design a passive quenching circuit adopting Silterra 180 nm CMOS technology utilizing thin gate technology devices and to be operated in low voltage environment mainly 1.8 V. The passive quenching circuit is integrated with a pulse discriminator circuit and also a 4-bit counter, called a “Pixel Array” which is designed on chip using Cadence tools [31]. The objective for this research are listed as follows:

- (i) To design a SPAD simulation model using Silterra 0.18 μm technology
- (ii) To design an on-chip 8 \times 1 array passive quenching circuit as readout circuit to quench the signal
- (iii) To design fully integrated on-chip 4 bit counter associate with 8x1 array

In previous researches, a ballast resistor were used as passive quenching circuit to quench the SPAD in order to detect the arrival of a photon, however, the photon count is limited to 25 MHz and 33.33MHz [6] respectively. These findings are detailed in Section 2.1.2.

This new approach of passive quenching is to obtain higher number of photon counting greater than 100 MHz by integrating the SPAD, quenching circuit and the counter on a single chip. The SPAD model, passive quenching circuit and pulse discriminator are adopted from previous research, which is developed using UMC 0.18 μm CMOS technology [32]. The problem with this previous study is the SPAD simulation model is generated using Agilent ADS. Hence, there is no evidence on SPAD simulation model performance on the same circuit design with passive quenching circuit prior fabrication using Cadence tool.

1.2 SCOPE OF WORK

The scope of work on this project report is to design a single pixel on-chip solution for a passive quenching circuit and a 4-bit counter. A SPAD model is adopted from Dalla Mora [1] is used to inject the signal for simulation purpose. To characterize the performance of the SPAD simulation model and also to define the specification of 8×1 passively quenched SPAD array. The circuit simulation performance is used to determine the capability of the array prior fabrication.

The main contribution of the author on this project report was developed a working SPAD simulation model in Cadence using Silterra 180 nm technology. Furthermore, the dead time (t_d) measured is ~ 10 ns (100Mhz) to improved Dr. Suhaila Isaak's 20ns dead time using off chip simulator SPAD model using Agilent ADS Simulator [32].

1.3 PROJECT REPORT OUTLINE

There are 5 chapters in this project report report. Chapter 1 described the introduction of the author's objective on this research including the scope of work. Chapter 2 covered on the literature review of the quenching circuit and also on SPAD model. Chapter 3 mainly focus on the research methodology which describes the overall circuitry. Chapter 4 reports on the design implementation and result and finally chapter 5 is on conclusion and future proposal.

CHAPTER 2

LITERATURE REVIEW

This chapter will discuss briefly about the theory and research from other researches related to this title. Single Photon Avalanche Diode (SPAD) mode of operations and also types of quenching circuits will be explained in details.

2.1 SPAD OPERATION

The detection of single photon is widely employed when weak and ultrafast optical signals are to be measured. The intensity of slowly varying optical signals is measured by counting detected photons during measurement time slots (photon counting). Many fields of industry and science demand suitable photon-counting modules: fluorescence spectrometry, quantum cryptography, single-molecule detection, etc. [7].

Single Photon Avalanche Diodes (SPADs) is an avalanche photodiode (APD) operated in Geiger mode [8]. SPAD are modified p-n junctions that are biased a few volts over its breakdown voltage. In this bias condition, a single photon arriving in the active region can trigger avalanche breakdown and hence generate a large number of electrons and holes in a very short time. If the bias voltage across the SPAD remains unchanged, the generated electrons and holes can themselves initiate

an avalanche and this process will continue indefinitely. In order to detect a single photon this avalanching must be quenched a short time after the photon is detected by reducing the voltage applied to the SPAD. Quenching can be achieved by connecting a MOSFET acting as a constant current source in series with the SPAD. If the avalanche process creates a current pulse that is larger than the current that the MOSFET can supply, then the voltage across the SPAD will fall quickly. If this fall is large enough the voltage across the SPAD will be too small to sustain avalanching, and the SPAD will be quenched. The bias voltage across the SPAD is then returned to its usual value by the MOSFET so that the SPAD is ready to detect the next photon [9].

2.1.1 Geiger Mode

In Geiger mode, a p-n junction is biased above V_{BD} which is dependent on the doping level of the lighter doped region [10]. The absorption of single photon initiates avalanche breakdown which is easily detected. When an APD detects a photon and it is biased over the breakdown voltage, it will create electron-hole pairs in the depletion region, which can gain sufficient energy to create more electron hole pairs. As a result, a large number of secondary carriers are generated and the diode is switches on, generating an avalanche current. The duration of avalanche current must be limited because it can lead to excessive power dissipation and could damage the device.

2.1.2 SPAD Circuit Model for Simulations

In order to define the operation on p-n junction diode of the quenched SPAD circuit above breakdown voltage, a detailed simulation model of the SPAD is required during the design phase [6, 11]. As reported earlier, a reverse biased p-n junction operating in Geiger mode is characterized by an avalanche breakdown event cause by microplasma effect [12-14]. In the following subsection, the findings with

recent and previous research on SPAD simulation model are summarized to assist to improve the current to voltage conversion SPAD simulation model in this thesis.

2.1.2.1 SPAD Model for passive quenching circuit

A simplified SPAD simulation model with passive quenching circuit was first introduced by S. Cova et. al [15] is shown in Figure 2.1. An avalanche current caused by the arrival of a photon is initiated by the closing of the switch, SW. SW represent the ON and OFF state of the SPAD [16]. The diode series resistance is limiting the avalanche region produce by avalanche current [17]. The turn-on probability is governed by the availability of carried for triggering and the probability that a carrier on space-charge layer will cause and avalanche [14]. The turn-off probability is determine by the probability of the number of carriers fluctuates to zero. Parasitic components, C_D as the junction capacitor and C_P as the total parasitic capacitance (typically in picofarads) must be considered in order to accurately model the quenching and recovery time.. An avalanche current is limited by the diode series resistance of the avalanche region itself [17].

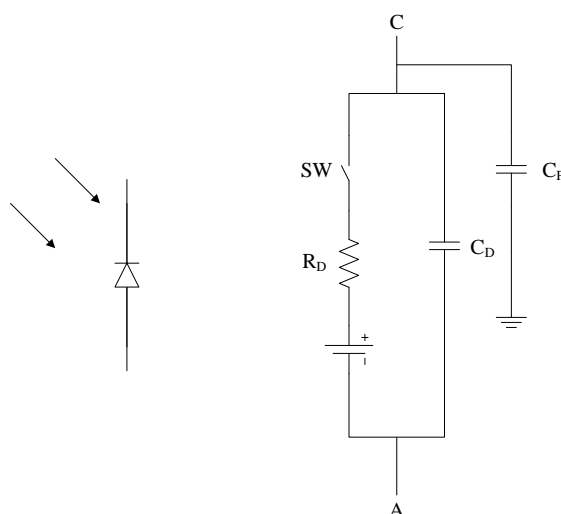


Figure 2.1 : Basic SPAD model

In figure above, an avalanche caused by the arrival of a photon is initiated by the closing of the switch, SW. SW represent the ON and OFF state of the SPAD [16]. The turn-on probability is governed by the availability of carried for triggering and

the probability that a carrier on space-charge layer will cause an avalanche [14]. Parasitic components shown in the figure must be considered in order to accurately model the quenching and recovery time. C_D is the junction capacitor and C_P is the total parasitic capacitance (typically in picofarads). An avalanche current is limited by the diode series resistance of the avalanche region itself [17]. The turn-off probability is determined by the probability of the number of carriers fluctuating to zero. However, this SPAD model is restricted to passive quenching circuit usage.

2.1.2.2 Electro-optical SPAD model

The electro-optical model to improve the performance of the SPAD model by S. Cova et al. [15] was proposed by Stoppa et al. [19] as shown in Figure 2.2. This model is modified from the basic SPAD simulation model introduced by Cova et al. [15] by the addition of the AND block and the voltage comparator to assure a fast convergence of the simulator. The circuit consists of the SPAD capacitance (C_{SPAD}), a leakage current (I_{leak}), resistor (R) to limit the maximum current flowing into the device, and the series of a voltage source and a voltage controlled switch driven by the Light Pulse signal. The capability of this SPAD model is able to observe the timing of the digital phases for a typical measurement window of 40 ns with the detection of a single light pulse.

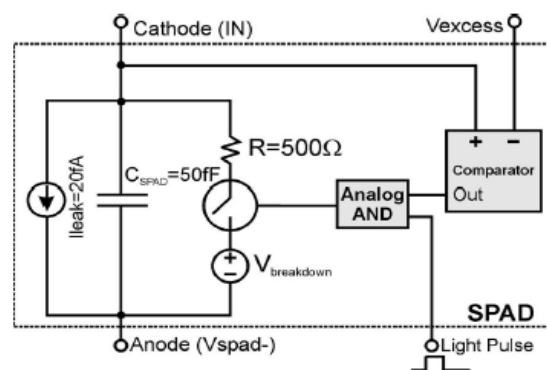


Figure 2.2 : The electro-optical model by Stoppa et al. [19]

2.1.2.3 SPAD Model by using transistor switch

Dalla Mora [6] is introduced a SPAD model in simulating the simplest quenching circuit (PQC) as shown in Figure 2.3 (left). In order to properly account for the quenching and recovery times, some parasitic components must be considered, as in the traditional basic SPAD model Figure 2.3 (right). C_{AC} is the junction capacitance and C_{AS} and C_{CS} are the stray capacitance from anode and cathode to substrate (typically few picofarads) the diode resistance R_D is given by the sum of the space-charge resistance of neutral regions crossed by the avalanche current. V_B is the breakdown voltage and the transistor controls the avalanche triggering.

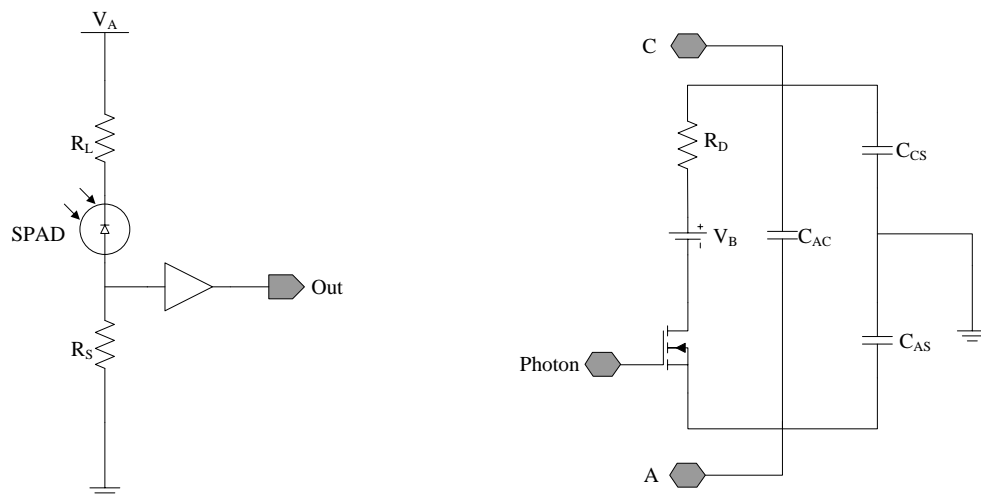


Figure 2.3 : Basic passive quenching circuit (left) and traditional SPAD model (right). The transistor switch mimics the avalanche triggering

2.2 PASSIVE QUENCHING CIRCUIT

The operation of SPAD with avalanche quenching circuits generated from the equivalent circuit model of the p-n junction reports in this thesis is based on passive quenching circuit. Passive quenching is the simplest way to quench and reset the SPAD by connecting a single high load quenching resistor, R_L between the bias voltage and the cathode of SPAD [3, 4, 21]. To ensure reliable quenching of breakdown, the value of R_L should be very large. The disadvantage of passive

quenching is that it is very slow due to the large recovery t_r and influences the size (duration) of the t_D , which limits the maximum count rate of the SPAD [4]. The capacitance of SPAD capacitance (C_D), R_L and parasitic capacitance (C_P) all contribute to a large t_D . In practice, the maximum count rates achievable with off-chip passive quenching circuits do not exceeded 100,000 Cps [3]. In addition, passively quenched SPAD do not have a well-defined t_D because of the slow increase of the detection probability during the recharge process [22]. However, most of developments of passively quenched SPAD are experimentally characterized. In this paper, the generation of a numerical model analysis based on passively quenched SPAD is discussed to obtain a small value of t_D , hence high count rates.

SPAD is biased above breakdown, V_B and gets triggered then current keeps flowing until the avalanche process is quenched by lowering the bias voltage down to V_B or below. The operating voltage must be restored after the t_D in order to make the Si APD able to detect another photon. Figure 2.4 show configuration of passive quenching circuit for photon detection [5].

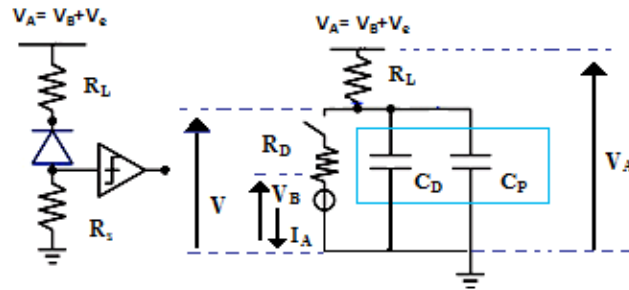


Figure 2.4 : Configuration of passive quenching circuit

In addition, total capacitance is given by $C=C_D+C_P$ and V_e is the excess voltage. When $V=V_A$, no current flows in the diode. From the passive quenching circuit above, before the arrival of photon the avalanche current, I_A and the voltage, V change with time according to:

$$I_A(t) = \frac{V_e}{R_D} \exp\left(-\frac{t}{R_D C}\right) \quad (2.1)$$

$$V(t) = V_B + V_e \exp\left(-\frac{t}{R_D C}\right) \quad (2.2)$$

During this operation, the avalanche current and the voltage across the diode follow respectively equation (1) and (2) until the quenching state. At quenching state, V is assumed equal to V_B , and C start to be recharged across R_L . The experimental value for lowering the bias voltages are implemented by using various value of R_L with fixed total capacitance value of 100 fF.

The recharge process of time-constant is given by:

$$V(t) = V_B + V_e \left[1 - \exp\left(-\frac{t}{R_L C}\right) \right] \quad (2.3)$$

$$V_e = V_{RB} - V_{BD} \quad (2.4)$$

2.3 QUENCHING, RECHARGE AND DEAD TIME

The Geiger mode pulse consists of two distinct time durations, quenching time (t_q) and recovery or recharge time (t_r). These two time durations are important because they determine the dead time of the SPAD. It is possible to compensate for the effect of dead time.

The dead time (t_D) is defined as from the moment of an avalanche event is quenched (quenching time) below V_{BD} until the moment the SPAD recovers 90% (recharge time) of its operating voltage. It depends on the SPAD capacitance and electronic circuit, which is used to quench the SPAD and the readout of the output of SPAD [24-26]. t_D should be as low as possible as it restricts the maximum rate of photon detections, and limits the dynamic range of the image sensor in imaging applications. Depending on the types of quenching circuit, the recharge period may exhibit slowly defined edges [4, 27].

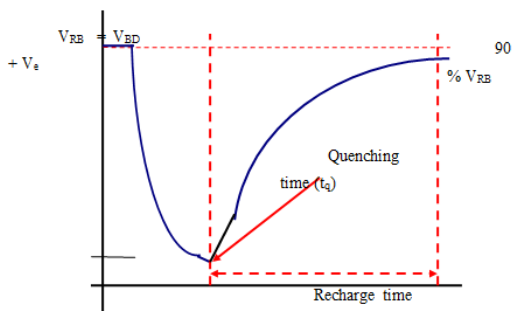


Figure 2.5 : Voltage pulse for passive quenching SPAD

Where, t_d is the dead time of the detector. The dead time (t_D) is also considered as the summing of recharge time, t_r and quenching time, t_q .

$$t_D = t_r + t_q \quad (2.5)$$

REFERENCES

1. Rochas, A., et al., *Low-noise silicon avalanche photodiodes fabricated in conventional CMOS technologies*. Electron Devices, IEEE Transactions on, 2002. **49**(3): p. 387-394.
2. Isaak, S., et al. *Fully integrated linear single photon avalanche diode (SPAD) array with parallel readout circuit in a standard 180 nm CMOS process*. in *Enabling Science and Nanotechnology (ESciNano), 2010 International Conference on*. 2010.
3. A. Rochas, *Single Photon Avalanche Diodes in CMOS technology*, 2003, EPFL: Switzerland.
4. S. Cova, M.G., A. LAcaita, C. Samori, and F.Zappa, *Avalanche photodiodes and active quenching circuits for single photon detection*. Journal of Applied Optics, 1996. **35**(12): p. 1956-1976.
5. Faramarzpour, N., et al., *Fully Integrated Single Photon Avalanche Diode Detector in Standard CMOS 0.18- μm Technology*. Electron Devices, IEEE Transactions on, 2008. **55**(3): p. 760-767.
6. Dalla Mora, A., et al., *Single-Photon Avalanche Diode Model for Circuit Simulations*. Photonics Technology Letters, IEEE, 2007. **19**(23): p. 1922-1924.
7. Zappa, F., A. Lotito, and S. Tisa, *Photon-counting chip for avalanche detectors*. Photonics Technology Letters, IEEE, 2005. **17**(1): p. 184-186.
8. Dimler, S.J., et al., *Capacitive Quenching Measurement Circuit for Geiger-Mode Avalanche Photodiodes*. Selected Topics in Quantum Electronics, IEEE Journal of, 2007. **13**(4): p. 919-925.

9. Chitnis, D. and S. Collins. *Compact readout circuits for SPAD arrays*. in *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*. 2010.
10. H.N.Becker, T.F. Miyahira, and A.J. Johnston, *The Influence of Structural Characteristics on the Response of Silicon Avalanche Photodiodes to Proton Irradiation*.
11. Cronin, D., A.M. Moloney, and A.P. Morrison. *Simulated monolithically integrated single photon counter*. in *High Frequency Postgraduate Student Colloquium, 2004*. 2004.
12. Kindt, W.J. and H.W. Van Zeijl, *Modelling and fabrication of Geiger mode avalanche photodiodes*. Nuclear Science, IEEE Transactions on, 1998. **45**(3): p. 715-719.
13. Haitz, R.H., *Model for the Electrical Behavior of a Microplasma*. Journal of Applied Physics, 1964. **35**(5): p. 1370-1376.
14. McIntyre, R.J., *On the avalanche initiation probability of avalanche diodes above the breakdown voltage*. Electron Devices, IEEE Transactions on, 1973. **20**(7): p. 637-641.
15. Cova, S., et al., *Avalanche photodiodes and quenching circuits for single-photon detection*. Applied Optics, 1996. **35**(12): p. 20.
16. Haitz, R.H., *Mechanisms Contributing to the Noise Pulse Rate of Avalanche Diodes*. Journal of Applied Physics, 1965. **36**(10): p. 3123-3131.
17. Becker, H.N., T.F. Miyahira, and A.H. Johnston, *The influence of structural characteristics on the response of silicon avalanche photodiodes to proton irradiation*. Nuclear Science, IEEE Transactions on, 2003. **50**(6): p. 1974-1981.
18. Mita, R. and G. Palumbo, *High-Speed and Compact Quenching Circuit for Single-Photon Avalanche Diodes*. Instrumentation and Measurement, IEEE Transactions on, 2008. **57**(3): p. 543-547.
19. Stoppa, D., et al. *A CMOS Sensor based on Single Photon Avalanche Diode for Distance Measurement Applications*. in *Instrumentation and Measurement Technology Conference, 2005. IMTC 2005. Proceedings of the IEEE*. 2005.

20. Zappa, F., et al., *Monolithic active-quenching and active-reset circuit for single-photon avalanche detectors*. Solid-State Circuits, IEEE Journal of, 2003. **38**(7): p. 1298-1301.
21. R.Haitz, *Model for the electrical behavior of a microplasma*. Journal of Applied Physics, 1964. **35**(5): p. 1370-1376.
22. W.J. Kindt and H.W. Van Zeijl, *Geiger mode avalanche photodiode arrays for spatially resolved single photon counting*, 1999., Delft University Holland.
23. F.Zappa, et al., *Principles and features of single photon avalanche diode arrays*. Sensors and Actuators A 2007. **140**: p. 103-112.
24. R.G. Brown, et al., *Characterization of silicon avalanche photodiodes for photon correlation measurements.2: active quenching*. Applied Optics, 1987. **26**(12): p. 2383-2389.
25. S. Tisa, F. Guerrieri, and F.Zappa, *Variable-load quenching circuit for single-photon avalanche diodes*. Optic Express, 2008. **16**(3): p. 2232-2244.
26. R.G.W.Brown, K.D.Ridley, and J.G. Rarity, *Characterization of silicon avalanche photodiodes for photon correlation measurements. 1: Passive quenching*. Applied Optics, Nov 1986. **25**(22): p. 4122-4126.
27. W. G. Odham, R.R. Samuelson, and P. Antognetti, *Triggering phenomena in avalanche diodes*. IEEE Transactions on Electron Devices, 1972. **19**(9): p. 1056-1060.
28. Dean, T., *Network+ guide to networks*. 2nd ed. 2002, Cambridge, Mass. ; London: Course Technology. xxiii, 948 p.
29. Horowitz, P. and W. Hill, *The art of electronics*. 2nd ed. 1989, Cambridge England ; New York: Cambridge University Press. xxiii, 1125 p.
30. Cahill, S.J., *Digital and microprocessor engineering*. 2nd ed ed. 1993, New York etc.: Ellis Horwood. XI, 687 p.
31. Cadence; <http://www.cadence.com/us/pages/default.aspx>
32. `Isaak, S., et al. *Design and characterisation of 16 parallel outputs SPAD array in 0.18 um CMOS technology*. in *Circuits and Systems (APCCAS), 2010 IEEE Asia Pacific Conference on*. 2010.