A HIGH SPEED 2D CONVOLUTION HARDWARE MODULE FOR IMAGE PROCESSING APPLICATIONS IN FPGA

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Specially dedicated to my family, lecturers, fellow friends and those who have guided and inspired me throughout my journey of education

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ABSTRACT

Visual information plays an essential role in almost all areas of our life, hence making image processing a very important subject of research. Image processing can be divided into digital image processing and analog image processing. Various applications including video surveillance, target recognition, and image enhancement requires digital image processing. In such applications, for functions like image filtering, image restoration, object tracking, template matching and many others, the spatial domain two-dimensional (2D) convolution plays a pivotal role. These functions are usually implemented in software previously but are slowly moving towards hardware for speed, as hardware allows pipelining and parallelism. The main objective of this project is to develop an image processing algorithm, 2D convolution. This project starts with architecture definition, followed by design implementation, verification and burning the design on FPGA. At the architecture definition stage, two different datapaths architectures are explored, Barrel Shifter and Multiplier. Basic design specifications are set and then design implementation is pursued. Verilog HDL is used to code the design; Quartus II tool is used for compilation and synthesis. The functionality and timing of the design is then verified using Modelsim tool before bringing the design to FPGA and tested using Quartus II's SignalTapII Logic Analyzer. Additionly, the design is further verified with real image pixels and compared the output pixels with that obtained from software (MATLAB). Altera Quartus II compilation report shows the 2D convolution design with Barrel Shifter can run at higher frequency compared to multiplier, and the design with off chip RAM runs faster than the design with on chip RAM.

ABSTRAK

Maklumat visual memainkan peranan yang penting dalam hampir semua aspek kehidupan kita, dengan it menjadikan pemprosen subjeck yang sangat penting dalam penyelidikan imej. Pemprosesan imej boleh dibahagikan kepada pemprosesan imej digital and pemprosesan imej analog. Pelbagain aplikasi termasuk pengawasan video, pengiktirafan sasaran, dan peningkatan imej menggunakan teknologi pemprosesan imej digital. Dalam aplikasi yang disebutkan, untuk fungsi seperti penapisan imej, pemulihan imej, pengesanan objek, padanan dan lain-lain lagi, convolution dua-dimensi (2D) memainkan peranan yang amat penting. Fungsi-fungsi ini biasanya direalisasikan dalam perisian(software) sebelum ini, tetap kini perkakasan (hardware) menjadi alternatif yang popular untuk tujuan kelajuan, kerana parallelism dan pipelining boleh dieksploitasi apabila menggunakan perkakasan. Objektif utama projek ini adalah untuk membangunkan algoritma pemprosesan imej convolution dua-dimentsi(2D). Projek ini bermula dengan definisi seni bina, diikuti oleh pelaksanaa reka bentuk, pengesahan dan akhirnya projeck dibawa ke FPGA. Di peringkat definisi seni bina, dua datapath berbeza diterokai untuk direalisasikan, Barrel Shifter and Multiplier. Spesifikasi reka bentuk asas ditetapkan dan kemudian reka bentuk dilaksanakan. Verilog HDL digunakan untuk kod reka bentuk; perisian Quartus II untuk membantu kod and sintesis. Fungsi reka bentuk kemudian diuji menggunakan perisian Modelsim sebelum dibawa ke FPGA dan diuji menggunakan SignalTapII logik Analyzer daripada perisian Quartus II. Selain itu, reka bentuk disahkan dengan membandingkan piksel imej daripada simulasi dengan piksel imej sebenar yang diperolehi daripada perisian MATLAB. Laporan sintesis perisian Altera Quartus II membuktikan bahawa reka bentuk convoler dua-dimensi(2D) berasakan Barrel Shifter lebih pantas daripada Multiplier, dan reka bentuk dengan cip RAM diluar lebih pantas daripada rekabetuk dengan RAM terbenam di dalam.

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LIST OF ABBREVIATIONS

ASIC	-	Application Specific Integrated Circuit
ASM	-	Algorithmic State Machine
CAD	-	Computer Aided Design
CB	-	Computation Block
CLB	-	Configurable Logic Block
CPU	-	Central Processing Unit
CU	-	Control Unit
DFG	-	Data Flow Graph
DIP	-	Digital Image Processing
DSP	-	Digital Signal Processor
DU	-	Datapath Unit
FIFO	-	First In First Out
FIR	-	Finite Impulse Response
FPGA	-	Field Programmable Gate Array
FSM	-	Finite State Machine
HDL	-	Hardware Description Language
IC	-	Integrated Circuit
LAB	-	Logic Array Block
RAM	-	Random Access Memory
RTL	-	Register Transfer Level
RTL-CS	-	RTL Control Sequence
Verilog	-	Verilog HDL
VHDL	-	Very High Speed Integrated Circuits HDL
VLSI	-	Very Large Scale Integration

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CHAPTER 1

INTRODUCTION

This project is about the hardware architecture design of a 2D convolution for spatial domain filter. The 2D convolution algorithm is implemented on the Field Programmable Gate Array (FPGA). This chapter gives an overview of the whole project, starts with a brief introduction to the background, followed by the problem statement, project objectives, scope of work and report outline.

1.1 Background

Visual information plays an essential role in almost all areas of our life. Hence, image processing becomes one of the highly researched subjects by many researchers around the world. Image processing can be divided into digital image processing and analog image processing. Digital image processing, has an obvious advantage as it allows a wider range of algorithms to be applied to the input data and can avoid problems like build-up of noise and signal distortion during processing. Over years, with the evolving technology of computers, digital image processing has become the most common form of image processing.

Various real time applications ranging from television to tomography, from photography to printing and from remote sensing to robotics requires digital image processing. Many of the applications require high computational capability, especially when high resolution images needs to be elaborated under real-time

requirements. In such applications, for functions like image filtering, image restoration, object tracking, template matching and many others, the spatial domain two-dimensional (2D) convolution plays a pivotal role. Hence a lot of weight is given on 2D convolution studies and design improvements.

2D convolution algorithm can be realized on hardware using either one of the methods: Full custom hardware design (ASIC) or Semi-custom hardware devices which are programmable devices. ASIC definitely has an upper hand as it fully customized, hence able to deliver high performance. However, being costly, complex and less flexible for iterations as it comes with large costs of fabrication makes it a less popular choice for algorithm development. It is normally used in high volume commercial applications after the design is confirmed with it's functionally and performance via Semi-custom hardware devices.

Semi-custom hardware devices further can be divided into two different categories, Digital Signal Processor (DSP) and Field Programmable Gate Array Logic (FPGA). Often, commercial DSPs are unable to support image convolution efficiently. For example, the TMS320C40 DSP microprocessor requires about 20 instructions per pixel when a 3x3 kernel is used [3]. Hence the need of parallelism and pipelining hardware is obvious.

FPGA as a programmable device which supports parallelism and pipelining hardware becomes an excellent choice. Adding on is the flexibility to change and modify the design at any point of time and reprogramming the device. Therefore FPGAs are ideal choice for hardware implementation of real-time image processing algorithms.

1.2 Motivation and Problem Statement

The very fact that digital image processing applications has real-time requirements and the general purpose DSP controllers are unable to support the 2D

convolution efficiently, there is a need to have special purpose parallel hardware circuit for convolution that runs on high frequency and can be tested on FPGA. However in most designs, the multiplier operating frequency becomes the bottleneck. Besides that, in order to support real-time system, 2D convolution also requires an effective memory access algorithm so that all neighborhood pixels can be accessed within one clock cycle [1].

Various studies have been done on how to implement an algorithm on FPGA. However, there is always a lack of step by step documentation on how to do so specially for new students, besides the user manuals from the respective tools used. It is crucial to have such documents for educational purposes.

1.3 Objectives

The main objective of this project is to propose an enhanced version of hardware architecture design of 2D convolution for Gaussian filter in spatial domain. The 2D convolution algorithm is implemented on FPGA using Verilog HDL. This project designs a FPGA friendly 2D convolution design, while applying the concept of datapath pipelining. This project also implements parameterization to a certain level for design modularization. Efficient algorithms are implemented to access the entire neighborhood pixels defined by the convolution kernel within one clock cycle for real-time applications. In this project, two design options and architectures are explored for performance trade-off analysis.

1.4 Scope of Work

In this project, a 2D convolution algorithm is implemented having Altera DE2 Development and Education Board as the target board in mind. Hence, the target library is Cyclone II – EP2C35F672C6 to match the Cyclone II EP2C35 (672-

pin package) FPGA that sits on the DE2 board. The design will be realized on FPGA with the help of Altera Quartus II version 12.1sps as a compiler and Modelsim version 10.1b as simulator. The design will be accomplished using Verilog HDL. A pipelined architecture is proposed to produce the output on every clock cycle.

The golden results will be obtained from MATLAB. This tool will be used to produce the software version results of the algorithm, and also to extract the input pixels of the image used. The design functionality will be verified by comparing the pixel output from the hardware simulation using Quartus II tool and the software version pixel output from MATLAB.

A performance difference measure is done to compare the two design options and architectures implemented.

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