

A HIGH SPEED 2D CONVOLUTION HARDWARE MODULE FOR IMAGE  
PROCESSING APPLICATIONS IN FPGA

BEENAL BABA

UNIVERSITI TEKNOLOGI MALAYSIA

A HIGH SPEED 2D CONVOLUTION HARDWARE MODULE FOR IMAGE  
PROCESSING APPLICATIONS IN HARDWARE

BEENAL BABA

A project report submitted in partial fulfilment of the  
requirements for the award of the degree of  
Master of Engineering (Electrical - Computer and Microelectronic System)

Faculty of Electrical Engineering  
Universiti Teknologi Malaysia

JUNE 2013

*Specially dedicated to my family, lecturers, fellow friends and those who have guided  
and inspired me throughout my journey of education*

## **ACKNOWLEDGEMENT**

Foremost, I would like to express my sincere gratitude to my advisor, Prof. Dr. Mohamed Khalil bin Hj Mohd Hani for the continuous support, patience, motivation, enthusiasm and immense knowledge. His guidance helped me in all the time of this project and writing of this thesis.

I would also like to extend my appreciation to Intel Microelectronics (M) Sdn. Bhd. for funding my studies. Special thanks to my manager as well as my colleagues who had provided me with help and support throughout the duration of my studies.

Last but not least, I would like to thank my family for giving me the support and encouragement as well as for being understanding throughout my studies.

## ABSTRACT

Visual information plays an essential role in almost all areas of our life, hence making image processing a very important subject of research. Image processing can be divided into digital image processing and analog image processing. Various applications including video surveillance, target recognition, and image enhancement requires digital image processing. In such applications, for functions like image filtering, image restoration, object tracking, template matching and many others, the spatial domain two-dimensional (2D) convolution plays a pivotal role. These functions are usually implemented in software previously but are slowly moving towards hardware for speed, as hardware allows pipelining and parallelism. The main objective of this project is to develop an image processing algorithm, 2D convolution. This project starts with architecture definition, followed by design implementation, verification and burning the design on FPGA. At the architecture definition stage, two different datapaths architectures are explored, Barrel Shifter and Multiplier. Basic design specifications are set and then design implementation is pursued. Verilog HDL is used to code the design; Quartus II tool is used for compilation and synthesis. The functionality and timing of the design is then verified using Modelsim tool before bringing the design to FPGA and tested using Quartus II's SignalTapII Logic Analyzer. Additionally, the design is further verified with real image pixels and compared the output pixels with that obtained from software (MATLAB). Altera Quartus II compilation report shows the 2D convolution design with Barrel Shifter can run at higher frequency compared to multiplier, and the design with off chip RAM runs faster than the design with on chip RAM.

## ABSTRAK

Maklumat visual memainkan peranan yang penting dalam hampir semua aspek kehidupan kita, dengan it menjadikan pemrosen subjeck yang sangat penting dalam penyelidikan imej. Pemprosesan imej boleh dibahagikan kepada pemprosesan imej digital and pemprosesan imej analog. Pelbagai aplikasi termasuk pengawasan video, pengiktirafan sasaran, dan peningkatan imej menggunakan teknologi pemrosesan imej digital. Dalam aplikasi yang disebutkan, untuk fungsi seperti penapisan imej, pemulihan imej, pengesanan objek, padanan dan lain-lain lagi, convolution dua-dimensi (2D) memainkan peranan yang amat penting. Fungsi-fungsi ini biasanya direalisasikan dalam perisian (software) sebelum ini, tetapi kini perkakasan (hardware) menjadi alternatif yang popular untuk tujuan kelajuan, kerana parallelism dan pipelining boleh dieksploitasi apabila menggunakan perkakasan. Objektif utama projek ini adalah untuk membangunkan algoritma pemrosesan imej convolution dua-dimensi (2D). Projek ini bermula dengan definisi seni bina, diikuti oleh pelaksanaan reka bentuk, pengesahan dan akhirnya projek dibawa ke FPGA. Di peringkat definisi seni bina, dua datapath berbeza diterokai untuk direalisasikan, Barrel Shifter and Multiplier. Spesifikasi reka bentuk asas ditetapkan dan kemudian reka bentuk dilaksanakan. Verilog HDL digunakan untuk kod reka bentuk; perisian Quartus II untuk membantu kod and sintesis. Fungsi reka bentuk kemudian diuji menggunakan perisian Modelsim sebelum dibawa ke FPGA dan diuji menggunakan SignalTap II logik Analyzer daripada perisian Quartus II. Selain itu, reka bentuk disahkan dengan membandingkan piksel imej daripada simulasi dengan piksel imej sebenar yang diperolehi daripada perisian MATLAB. Laporan sintesis perisian Altera Quartus II membuktikan bahawa reka bentuk convolver dua-dimensi (2D) berasaskan Barrel Shifter lebih pantas daripada Multiplier, dan reka bentuk dengan cip RAM diluar lebih pantas daripada rekabentuk dengan RAM terbenam di dalam.

## TABLE OF CONTENTS

CHAPTER	TITLE	PAGE
	<b>DECLARATION</b>	ii
	<b>DEDICATION</b>	iii
	<b>ACKNOWLEDGEMENT</b>	iv
	<b>ABSTRACT</b>	v
	<b>ABSTRAK</b>	vi
	<b>TABLE OF CONTENTS</b>	vii
	<b>LIST OF TABLES</b>	x
	<b>LIST OF FIGURES</b>	xi
	<b>LIST OF ABBREVIATIONS</b>	xiv
	<b>LIST OF APPENDICES</b>	xv
<b>1</b>	<b>INTRODUCTION</b>	1
	1.1 Background	1
	1.2 Motivation and Problem Statement	2
	1.3 Objectives	3
	1.4 Scope of Work	3
<b>2</b>	<b>THEORY AND LITERATURE REVIEW</b>	5
	2.1 Convolution Operation	5
	2.2 Gaussian Kernel	8
	2.3 Literature Review	10
<b>3</b>	<b>METHODOLOGY AND DESIGN TOOL</b>	17

3.1	Design Methodology	17
3.2	Design Tools	21
3.2.1	MATLAB	21
3.2.2	Verilog HDL	22
3.2.3	Quartus II 12.1sp1	23
3.2.4	Modelsim 10.1b	25
3.2.5	DE2 Development and Education Board	26
<b>4</b>	<b>DESIGN IMPLEMENTATION</b>	<b>29</b>
4.1	Design Specification	29
4.2	Software Design using Matlab	31
4.3	2D Convolution Designs	34
4.3.1	Barrel Shifter based 2D convolution	35
4.3.1.1	1D convolution with Barrel Shifter DU	35
4.3.1.2	Barrel Shifter based 2D convolution	41
4.3.1	Multiplier based 2D convolution	50
4.3.2.1	1D convolution with Multiplier DU	50
4.3.2.2	Multiplier based 2D convolution	55
<b>5</b>	<b>DESIGN VERIFICATION AND PERFORMANCE ANALYSIS</b>	<b>64</b>
5.1	1D Convolution Quartus II Simulation	64
5.2	2D Convolution Quartus II Simulation	67
5.4	Performance Analysis	74
<b>7</b>	<b>CONCLUSION AND FUTURE WORK</b>	<b>76</b>
7.1	Conclusion	76
7.2	Future Work	77

**REFERENCES**

79

Appendix A-C

80-101

**LIST OF TABLES**

<b>TABLE NO.</b>	<b>TITLE</b>	<b>PAGE</b>
4.1	RTL-CS Table for Control Unit of Barrel Shifter Based 1D Convolution Unit	40
4.2	RTL-CS Table for 2D Convolution Control Unit	47
4.3	RTL-CS Table for Control Unit with Multiplier in DU	54
4.4	RTL-CS Table for 2D Convolution Control Unit	60
5.1	Performance Analysis	75

## LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
2.1	Moving Kernel from Point to Point on an Image	6
2.2	(left) 3x3 Kernel, (right) Kernel Coincides with Image, (bottom) 2D Convolution Equation Based on the Image and Kernel Coordinates	7
2.3	2D Convolution	8
2.4	Bell Shaped Gaussian Function	9
2.5	Log Based Convolution Model	11
2.6	Kernel Architecture for 3x3 kernel	11
2.7	2D Convolution Architecture	12
2.8	2D Convolution Represented by 1D Convolution	13
2.9	Multiplier Based 1D Convolver	14
2.10	Barrel Shifter Based 1D Convolver	14
2.11	Barrel Shifter Based 2D Convolver	15
2.12	2D Convolution on GPU, CPU and FPGA	15
2.13	SRAM-based FPGA Design	16
3.1	2D Convolution Design Flow	18
3.2	RTL Design Design Flow	19
3.3	Verilog HDL Design Flow	23
3.4	Quartus II Design Flow	24
3.5	Quartus II Compilation Flow	25
3.6	Modelsim Simulation Flow	26
3.7	DE2 Board	27
3.8	SignalTapII Logic Analyzer Flow	28
4.1	3x3 Kernel and Co-Efficient	30

4.2	Gaussian Filter Matlab Code	32
4.3	(left) Original Image with Gaussian Noise (right) Gaussian Filtered Image	33
4.4	T Input Image Matrix from Matlab	33
4.5	Input Image in .mif File Format	33
4.6	Moore Model Control Unit(CU)	35
4.7	DFG for (left) [1 2 1] Kernel (right) [2 4 2] Kernel	37
4.8	Barrel Shifter based 1D Convolution ASM Chart	38
4.9	IO Block Diagram for Barrel Shifter Based 1D Convolution	39
4.10	Datapath Unit(DU) for Barrel Shifter Based 1D Convolution	39
4.11	Control Unit (CU) for Barrel Shifter Based 1D Convolution	41
4.12	Barrel Shifter Based 1D Convolution Top ModuleI	41
4.13	Barrel Shifter based 2D Convolution ASM Chart	43
4.14	Block Diagram for Barrel Shifter Based 2D Convolution	44
4.15	Functional Block Diagram of Sub-Module shift_121	45
4.16	Functional Block Diagram of Sub-Module shift_242	45
4.17	Datapath Unit(DU) for Barrel Shifter Based 2D Convolution	46
4.18	Control Unit (CU) for Barrel Shifter Based 2D Convolution	48
4.19	FPGA Friendly Block Diagram for Barrel Shifter Based 2D Convolution	49
4.20	Quartus II Compilation for Barrel Shifter Based 2D Convolution	50
4.21	DFG for both [1 2 1] and [2 4 2] Kernel	51
4.22	Multiplier based 1D Convolution ASM Chart	52
4.23	IO Block Diagram for Multiplier Based 1D Convolution	53
4.24	Datapath Unit(DU) for Multiplier Based 1D Convolution	53
4.25	Control Unit (CU) for Barrel Shifter Based 1D Convolution	55
4.26	Multiplier Based 1D Convolution Top Module	55
4.27	Multiplier based 2D Convolution ASM Chart	57
4.28	Block Diagram for Multiplier Based 2D Convolution	58
4.29	Multiplier module for 1D Kernel	59
4.30	Datapath Unit(DU) for Multiplier Based 2D Convolution	60
4.31	Control Unit (CU) for Barrel Shifter Based 2D Convolution	61

4.32	FPGA Friendly Block Diagram for Multiplier Based 2D Convolution	62
4.33	Quartus II Compilation for Barrel Shifter Based 2D Convolution	63
5.1	Input Pixels with the Expected Output Pixels	65
5.2	Testbench for Barrel Shifter based 1D convolution module	66
5.3	Waveform for Barrel Shifter based 1D convolution module	66
5.4	Testbench for Multiplier based 1D convolution module	66
5.5	Waveform for Multiplier based 1D convolution module	66
5.6	Process to Validate 2D Convolution Module on Modelsim tool	67
5.7	5x10 Random Input Pixels	68
5.8	Expected Output Pixels	68
5.9	Waveform for Barrel Shifter Based 2D Convolution Module	68
5.10	Waveform for Multiplier Based 2D Convolution Module	68
5.11	Dummy Memory Created for Testing	69
5.12	Expected Output Pixels	69
5.13	Waveform for Barrel Shifter Based 2D Convolution Module	69
5.14	Waveform for Multiplier Based 2D Convolution Module	69
5.15	Waveform for Barrel Shifter Based 2D Convolution Module	70
5.16	Waveform for Barrel Shifter Based 2D Convolution Module	70
5.17	(left) input image with Gaussian Noise (middle) output image from MATLAB (right) output image from Barrel Shifter/Multiplier	71
5.18	Pin assignment for Barrel Shifter Based 2D Convolution Design	71
5.19	Waveform for Barrel Shifter Based 2D Convolution Design	72
5.20	2D convolution Design as Part of Altera Avalon Fabric	72
5.21	Figure 5.21: 2D convolution Design as Part of Altera Avalon Fabric	73

**LIST OF ABBREVIATIONS**

ASIC	-	Application Specific Integrated Circuit
ASM	-	Algorithmic State Machine
CAD	-	Computer Aided Design
CB	-	Computation Block
CLB	-	Configurable Logic Block
CPU	-	Central Processing Unit
CU	-	Control Unit
DFG	-	Data Flow Graph
DIP	-	Digital Image Processing
DSP	-	Digital Signal Processor
DU	-	Datapath Unit
FIFO	-	First In First Out
FIR	-	Finite Impulse Response
FPGA	-	Field Programmable Gate Array
FSM	-	Finite State Machine
HDL	-	Hardware Description Language
IC	-	Integrated Circuit
LAB	-	Logic Array Block
RAM	-	Random Access Memory
RTL	-	Register Transfer Level
RTL-CS	-	RTL Control Sequence
Verilog	-	Verilog HDL
VHDL	-	Very High Speed Integrated Circuits HDL
VLSI	-	Very Large Scale Integration

**LIST OF APPENDICES**

<b>APPENDIX</b>	<b>TITLE</b>	<b>PAGE</b>
A	Barrel Shifter Based 2D Convolution Verilog Program	80
B	Multiplier Based 2D Convolution Verilog Program	90
C	PERL Script for Data Post-Processing	101

## **CHAPTER 1**

### **INTRODUCTION**

This project is about the hardware architecture design of a 2D convolution for spatial domain filter. The 2D convolution algorithm is implemented on the Field Programmable Gate Array (FPGA). This chapter gives an overview of the whole project, starts with a brief introduction to the background, followed by the problem statement, project objectives, scope of work and report outline.

#### **1.1 Background**

Visual information plays an essential role in almost all areas of our life. Hence, image processing becomes one of the highly researched subjects by many researchers around the world. Image processing can be divided into digital image processing and analog image processing. Digital image processing, has an obvious advantage as it allows a wider range of algorithms to be applied to the input data and can avoid problems like build-up of noise and signal distortion during processing. Over years, with the evolving technology of computers, digital image processing has become the most common form of image processing.

Various real time applications ranging from television to tomography, from photography to printing and from remote sensing to robotics requires digital image processing. Many of the applications require high computational capability, especially when high resolution images needs to be elaborated under real-time

requirements. In such applications, for functions like image filtering, image restoration, object tracking, template matching and many others, the spatial domain two-dimensional (2D) convolution plays a pivotal role. Hence a lot of weight is given on 2D convolution studies and design improvements.

2D convolution algorithm can be realized on hardware using either one of the methods: Full custom hardware design (ASIC) or Semi-custom hardware devices which are programmable devices. ASIC definitely has an upper hand as it fully customized, hence able to deliver high performance. However, being costly, complex and less flexible for iterations as it comes with large costs of fabrication makes it a less popular choice for algorithm development. It is normally used in high volume commercial applications after the design is confirmed with its functionality and performance via Semi-custom hardware devices.

Semi-custom hardware devices further can be divided into two different categories, Digital Signal Processor (DSP) and Field Programmable Gate Array Logic (FPGA). Often, commercial DSPs are unable to support image convolution efficiently. For example, the TMS320C40 DSP microprocessor requires about 20 instructions per pixel when a 3x3 kernel is used [3]. Hence the need of parallelism and pipelining hardware is obvious.

FPGA as a programmable device which supports parallelism and pipelining hardware becomes an excellent choice. Adding on is the flexibility to change and modify the design at any point of time and reprogramming the device. Therefore FPGAs are ideal choice for hardware implementation of real-time image processing algorithms.

## **1.2 Motivation and Problem Statement**

The very fact that digital image processing applications has real-time requirements and the general purpose DSP controllers are unable to support the 2D

convolution efficiently, there is a need to have special purpose parallel hardware circuit for convolution that runs on high frequency and can be tested on FPGA. However in most designs, the multiplier operating frequency becomes the bottleneck. Besides that, in order to support real-time system, 2D convolution also requires an effective memory access algorithm so that all neighborhood pixels can be accessed within one clock cycle [1].

Various studies have been done on how to implement an algorithm on FPGA. However, there is always a lack of step by step documentation on how to do so specially for new students, besides the user manuals from the respective tools used. It is crucial to have such documents for educational purposes.

### **1.3 Objectives**

The main objective of this project is to propose an enhanced version of hardware architecture design of 2D convolution for Gaussian filter in spatial domain. The 2D convolution algorithm is implemented on FPGA using Verilog HDL. This project designs a FPGA friendly 2D convolution design, while applying the concept of datapath pipelining. This project also implements parameterization to a certain level for design modularization. Efficient algorithms are implemented to access the entire neighborhood pixels defined by the convolution kernel within one clock cycle for real-time applications. In this project, two design options and architectures are explored for performance trade-off analysis.

### **1.4 Scope of Work**

In this project, a 2D convolution algorithm is implemented having Altera DE2 Development and Education Board as the target board in mind. Hence, the target library is Cyclone II – EP2C35F672C6 to match the Cyclone II EP2C35 (672-

pin package) FPGA that sits on the DE2 board. The design will be realized on FPGA with the help of Altera Quartus II version 12.1sps as a compiler and Modelsim version 10.1b as simulator. The design will be accomplished using Verilog HDL. A pipelined architecture is proposed to produce the output on every clock cycle.

The golden results will be obtained from MATLAB. This tool will be used to produce the software version results of the algorithm, and also to extract the input pixels of the image used. The design functionality will be verified by comparing the pixel output from the hardware simulation using Quartus II tool and the software version pixel output from MATLAB.

A performance difference measure is done to compare the two design options and architectures implemented.

## REFERENCES

- [1] Ng Bee Yee, "FPGA Implementation of Image Processing 2D Convolution for Spatial Filter", Universiti Teknologi Malaysia, June 2012.
- [2] Anthony Edward Nelson, "Implementation of Image Processing Algorithms on FPGA Hardware", Vanderbilt University, May 2000.
- [3] Bernard Bosi, Guy Bois, Yvon Savaria, "Reconfigurable Pipelined 2-D Convolvers for Fast Digital Signal Processing", *IEEE Transaction on Very Large Scale Integration (VLSI) Systems*, Vol. 7, No. 3, September 1999.
- [4] Ben Cope, "Implementation of 2D Convolution on FPGA, GPI and CPU," Department of Electrical & Electronic Engineering, Imperial College London.
- [5] Ming Z. Zhang, Hau T. Ngo and Vijayan K. Asari, "Design of an Efficient Multiplier-less Architecture for Multi-Dimensional Convolution", Old Dominion University, 2005.
- [6] Ming Z. Zhang, Vijayan K. Asari, "An Efficient Multiplier-less Architecture for 2-D convolution with quadrant symmetric kernels", INTEGRATION, the VLSI Journal 40 (2007) 490-502, July 2006.
- [7] S. Perri, M. Lanuzza, P. Corsonello, G. Cocorullo, "SIMD 2-D Convolver for Fast FPGA-based Image and Video Processors", Perri et al., Paper D2.
- [8] Francisco Fons, Mariano Fons, Enrique Canto, "Run-time self-configurable 2D Convolver for adaptive image processing," *Microelectronics Journal*, August 2010.
- [9] DE2 Development and Education Board User Guide.
- [10] Quartus II Handbook Version 12.1