RADIO FREQUENCY CIRCUIT DESIGN BASED ON VARIABLE RESISTANCE ACTIVE INDUCTOR

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To My beloved Mother, Father and Wife.

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ABSTRACT

Amongst design challenges in designing Complementary Metal-Oxide-Semiconductor (CMOS) active inductors are to produce high inductance and high tune-ability within an acceptable quality factor in a specific frequency range. The need for these design qualities is apparent in Radio Frequency (RF) circuits such as filters, Low Noise Amplifiers (LNAs) and Voltage-Controlled Oscillators (VCOs). This thesis focuses on the above issues to design tunable active inductor circuits and offers a design approach which partially solves some of the design challenges. Three active inductor circuits with comparable or better performance in terms of high inductance and tune-ability are produced from this research work. These active inductors which have been designed using Cadence Spectra based on CMOS 0.18 µm Silterra process have high tune-ability, high quality factor and wide tuning range. Their inductance tune-ability ranges from 5 nH to 500 nH with a frequency range of 1 GHz to 7 GHz and the quality factor range of 30 to 700. The power dissipation is from 1.9 mW to 6.5 mW from a 1.8 V DC power supply. The inductance can be tuned by tuning the variable resistance within the active inductor itself. The active inductors have been employed in LNA and VCO circuits where their output frequency range is changed by tuning the variable resistor. The simulation result for the LNA shows a frequency range of 1 GHz to 2.5 GHz with high gain (S_{21}), low input return loss (S_{11}), low output return loss (S_{22}) and low noise figure. For the VCO, the oscillating frequency ranges from 0.5 GHz to 2.2 GHz with low chip size, high K_{VCO} and high output power.

ABSTRAK

Antara cabaran dalam reka bentuk Pelengkap Semikonduktor-Oksida- Logam (CMOS) pengaruh aktif adalah untuk menghasilkan kearuhan dan keboleh talaan yang tinggi bagi faktor kualiti yang boleh diterima dalam julat frekuensi yang tertentu. Keperluan untuk kualiti reka bentuk ini dapat dilihat jelas dalam litar Frekuensi Radio (RF) seperti penapis, Penguat Rendah Bunyi (LNAs) dan Pengayun Voltan-Kawalan (VCOs). Tesis ini memberi tumpuan kepada isu-isu di atas dan menawarkan sebahagian penyelesaian kepada cabaran reka bentuk. Tiga litar pengaruh aktif dengan prestasi yang setanding atau lebih baik dari segi kearuhan dan talaan yang tinggi dihasilkan dari kerja-kerja penyelidikan ini. Pengaruh aktif ini telah direka dengan menggunakan Cadence Spectra berdasarkan proses Silterra CMOS 0.18 μm. Pengaruh aktif ini mempunyai keupayaan talaan dan faktor kualiti yang tinggi disamping julat talaan yang lebar. Keupayaan talaan kearuhan litar ini adalah dari 5 nH hingga 500 nH dengan julat frekuensi dari 1 GHz hingga 7 GHz dan faktor kualiti diantara 30-700. Pelesapan kuasa adalah dari 1.9 mW hingga 6.5 mW dari bekalan kuasa DC 1.8 V. Kearuhan boleh ditala dengan penalaan rintangan boleh ubah dalam pengaruh aktif itu sendiri. Pengaruh aktif ini telah digunakan dalam litar LNA dan VCO di mana julat frekuensi keluaran boleh diubah deang penalaan perintang bolehubah. Hasil simulasi menunjukkan keupayaan julat frekuensi dari 1 GHz hiagga 2.5 GHz dengan gandaan yang tinggi (S_{21}), pekali pantulan voltan masukan (S_{11}), dan pekali pantulan voltan keluaran (S_{22}) yang rendah dan nilai bunyi yang rendah. Untuk VCO, julat ayunan frekuensi adalah dari 0.5 GHz hingga 2.2 GHz dengan saiz cip yang kecil, K_{VCO} dan kuasa keluaran yang tinggi.

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LIST OF SYMBOLS

A	-	Ampere
A_v	-	Voltage Gain
C	-	Capacitor
C_p	-	Parallel Capacitance
C_{gs}	-	Transistor gate-source capacitance
dB	-	Decibel
dBc/Hz	-	Phase noise unit
dBm	-	Decibel of power referenced to one milliwatt
f	-	Frequency
f_r	-	Resonance frequency
fF	-	Femto Farad
F	-	Noise factor
g	-	Conductance
g_{ds0}	-	g_{ds} at V_{DS}=0V
g_{ds}	-	Output conductance
g_m	-	Transconductance
Hz	-	Hertz
I	-	Current
i_{in}	-	Input AC current
$\overline{I_{n,R_L}^2}$	-	Thermal noise of Load resistor R_L
$\overline{I_{n,M_i}^2}$	-	Thermal noise of transistor M_i
GHz	-	Giga Hertz
K	-	Boltzmans's constant
K_{VCO}	-	gain of the VCO
kΩ	-	Kilo Ohm

L	-	Inductance
MHz	-	Mega Hertz
mV	-	Milli volt
mW	-	Milli watt
MΩ	-	Mega Ohm
M_i	-	Transistor Number i
nH	-	Nano-Henry
nF	-	Nano-Farad
nm	-	Nano-meter
pF	-	Pico-Farad
Q	-	Quality Factor
R	-	Resistance
R_t	-	Tuning Resistor
R_s	-	Serial resistance
R_p	-	Parallel resistance
R_f	-	Feedback resistance
r_o	-	Output resistance of transistor
S	-	Scattering Parameters or S-parameters
S_{22}	-	Output return loss
S_{21}	-	power gain
S_{12}	-	reverse isolation
S_{11}	-	input return loss
T	-	Temperature (Kelvin)
t	-	Time
V	-	Volt
V_{DD}	-	Voltage Supply
v_{in}	-	Input AC voltage
V_t	-	Tuning Voltage
V_{Bi}	-	Bias voltage at node i
V_i	-	Voltage at node i
$\overline{V_{o,n}^2}$	-	Output referred noise voltage
$\overline{V_n^2}$	-	Voltage noise
W	-	Watt

W_t/L_t	-	Transistor width and length
Y	-	Admittance
Y_{in}	-	Input Admittance
Z_{in}	-	Input Impedance
ω	-	Angular frequency
ω_0	-	Resonance angular frequency
γ	-	Fitting parameter for the noise model
Γ	-	Reflection Coefficient
Ω	-	Ohm
$\boldsymbol{\pi}$	-	Pi
μm	-	Micro Meter
μA	-	Micro Ampere
Δf	-	Noise bandwidth
[Z]	-	Impedance Matrix

LIST OF ABREVIATIONS

AC	-	Alternative current
AI	-	Active Inductor
BiCMOS	-	Bipolar CMOS
CD	-	Common Drain
CMOS	-	Complementary Metal-Oxide-Semiconductor
CS	-	Common Gate
DAI	-	Differential Active Inductor
DC	-	Direct Current
FFT	-	Fast Fourier Transform
GPS	-	Global Positioning System
GSG	-	Ground-Signal-Ground
GSM	-	Global System for Mobile communications
KCL	-	Kirchhoff's Current Low
KVL	-	Kirchhoff's Voltage Low
LAN	-	Local Area Network
LNA	-	Low Noise Amplifier
LO	-	Local Oscillator
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect-Transistor
NF	-	Noise Figure
NFmin	-	Minimum Noise Figure
NMOS	-	N-channel MOSFET
NR	-	Negative Resistance
OTAs	-	Operational Transconductance Amplifiers
PLL	-	Phase Locked Loop
PMOS	-	P-channel MOSFET
RF	-	Radio Frequency

RFIC	-	Radio Frequency Integrated Circuit
SiGe	-	Silicon Germanium
SOC	-	System-On-a- Chip
VCO	-	Voltage-Controlled Oscillator
WCDMA	-	Wideband Code Division Multiple Access
WLAN	-	Wireless Local Area Network

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CHAPTER 1

INTRODUCTION

1.1 Background

Wireless communication systems are changing fast due to the increasing the demands for high quality wireless devices. Nowadays, the feature sizes of the CMOS devices are decreasing while the operating frequencies of the CMOS devices are increasing. And for CMOS designers, the cost and integration of chip regarding higher performance, small chip area and lower power consumption are challenging task. The expansion of wireless communication systems demands for low cost, high performance and small chip size RF transceivers.

CMOS spiral inductors have effective applications in RF circuits, signal processing and data communications. These applications include Voltage Controlled Oscillator (VCOs), Low Noise Amplifier (LNAs), filters, Phase Locked Loops (PLLs), RF phase shifts and so many applications. But these inductors have some disadvantages. The most important disadvantages are:

1- Low Quality Factor:

The inductance of a spiral inductor is fixed and depend on the number of the turns of spiral is set. The only way to increase the inductance of the spiral inductor is to increase the number of the turns of the spiral or use a stacked configuration. By

increasing the number of turn the chip size and spiral substrate capacitance will be increased dramatically.

2- Large silicon area:

The inductance of a spiral inductor is directly proportional to the number of turns of the spiral of the inductors. For high value of inductor we have to increase the number of turn, and it increases that the chip size. For example, for 8 nH inductance we need 6 turns with d_{out}= 400 μm. The chip area is larger than 400×400 μm^2.CMOS active inductors composed of CMOS transistors in special topology that have the inductive characteristic in a specific frequency range.

Active Inductors (AI) in comparison with spiral inductors have advantages such as low chip size, tunable inductance and tunable Q factor. Designing high inductance and high Q factor AI is a challenging task.

If these design issues are solved, the applications of active inductor will be expanded in CMOS RF circuit such as: VCO, LNA, PLL, RF band pass filters, and in many other applications. The applications of active inductors are affected by problems that come from the intrinsic characteristics of MOS devices. The most important of these problems is high sensitivity to noise. It should be considered that this limitation is related to all CMOS devices.

1.2 Problem Statement

The most challenging tasks in designing active inductors are high inductance, high tune ability and reconfigure ability within an acceptable Q factor in specific frequency range. Tune ability of active inductors is the main advantage of active inductors that qualified it to be used in RF circuits. This is because most of the RF circuits such as filters and VCOs need to use a tunable inductor for frequency band selections. This issue is apparent as some of recently published active inductor

circuits do not have a capability of tune ability and reconfigure ability. This is clearly the weakness of these active inductors circuits. Some research work may have improved Q, but circuits do not have tune ability and reconfigure ability. In this case, this active inductor circuit can be used just in specific applications for a fixed value of Q factor and inductance value.

The other important characteristic of active inductors is designing active inductor with high inductivity. In some circuit such as LNA, filter and VCO, using a high inductance inductor is necessary. In designing LNA, the gain is directly related to output inductance. By using active inductor with a high inductance, the total gain will be high and also the frequency range will be reconfigurable. For example, the Q factor could be around 40, but the inductance is low (around 2 nH). In another work, the Q factor is high (around 340), but the inductance is also low (around 1.5 nH). In this case, these active inductor circuits cannot be used in an application such as LNA. Because in some LNA circuit, we need high inductance value. (For example higher than 10 nH).

Q factor is another important parameter in active inductors circuit. In some case, there is a trade of between high Q factor and high inductance value. But the most important aims are high inductance and high tunable active inductors with acceptable Q factor.

The low power dissipation is the another characteristic of the active inductor that should take it to account in designing active inductor circuit. Because, the active inductor power dissipation will be added to the applied circuit power consumption and caused that the total power dissipation to increase. The power dissipation of the active inductor circuit is depended on the structure of the active inductor and designing process. In some topologies because of structure, the power dissipation is high and in some cases it is low. By designing active inductor circuit based on low power dissipation, it is possible to decrease active inductor's power consumption.

Based on the above design issues, the problem statement of this research can be summarized as: Designing high inductance, high tune ability, high Q factor and low power active inductor circuit.

1.3 Objective of Research

The main objectives of this research are three:

1- Designing high tunable active inductor

2- Increase the quality factor

3- Employ the designed active inductors in RF modules, which are VCO or LNA

Design and characterize active inductor circuits which high inductance (from a few nH up to 100 nH) and high tune ability with acceptable Q factor (Maximum value of Q up to 400) and low power dissipation. In the first stage, a study will be conducted on methods to design active inductor circuit and analysis will be carried out on the active inductor's performance such as inductance, Q factor, tune ability and dc power consumption.

For achieving high inductance value active inductor circuit; we should survey on active inductor structures that have high impedance value. After designing active inductor architecture, we have to set bias condition of active inductor circuit to have a high impedance value.

The tune ability and reconfigure ability is the other performance that should be considered in designing process. The active inductor circuit that has the capability of tune ability, can be used in so many applications such as VCO and reconfigure able LNA. The high Q factor is the other performance of active inductor circuit that should be considered in the design process to achieve acceptable value.

By using the designed active inductor circuits in applications such as VCO and LNA, we can show the capability of these active inductor circuits and we can

prove that these active inductors are employable. For example, in VCO circuit, we can explain the tune ability of frequency range by tuning active inductor circuit. In the LNA circuit we can show the tune ability of frequency range and reconfigure ability of the circuit by tuning the active inductor circuit core.

1.4 Scope of Study

The scopes of study are as follows:

1. In the first stage of the work, there is a crucial need to make a literature review of up to date active inductors. After surveying all previous designed and published active inductors, an analysis of major active inductor's performances will be carried out, and it is the task of this research to come out with at least comparable or better performance in terms of high inductance, tune ability, high Q factor and low power dissipation.

The review and analysis could be grouped in to 3 categories:

1- Designing active inductor circuit using reported active inductors topology with improve characteristics. This is possible by changing the active inductors circuit biasing. Because dc biasing is one of the important parts of active inductor design schedules. In active inductor circuit, dc biasing has directly an effect on g_m of transistors and g_m of transistors have most effect on Q factor and inductance parameters. With this reason, by improving the bias condition we can design active inductor circuit with best performance with previously published topology.

2- Designing active inductor circuit using reported topology but by changing or adding some elements to improve the performance of the circuit. By changing some part of topology in sometimes it is possible to improve the performance.

3- Designing new active inductor circuit topology.

In some case, after surveying all active inductors topologies, it is possible to design active inductor circuit with new topology. By knowing the base of active inductor circuit and by respect to the gyrator concept, it is possible to build new architecture to work as active inductor circuit. In some case, we can conflict two active inductor circuit to make a new architecture with improved performance.

By using one of this three method the active inductors circuit characteristics can be improved.

2. Design Active Inductor architecture

After choosing active inductor design method and architecture, the design process will be started. For analysis of the proposed active inductor circuit, the Cadence software using 0.18 µm Silterra process was used. During this process all the performances of the designed active inductor will be checked to reach the desired performance of active inductor circuit. If the desired performance of the active inductor is achieved, this step will be finished.

3. Apply the designed active inductor in RF modules.

In this step, the designed active inductors will be applied to the RF modules such as: LNA and VCO to evaluate the performance and applicable of active inductors circuit. Because some of the active inductors have good performance, but they are not applicable in RF modules such as LNA, VCO and filter or other in applications of active inductor circuit.

1.5 Thesis Organization

This dissertation is organized as follows. Chapter 1 discusses the problem statement, objective of research. Chapter 2 begins with an overview of the active inductor circuit structures by presenting fundamental concepts of active inductor circuit and continued with literature review. In this part, we have a quick review of

the active inductor history and advanced active inductors topology. Chapter 3 introduce proposed active inductor circuit. The analysis and the simulation result will be explained in this chapter. In this chapter inductance and Q factor equations will be discussed. In chapter 4, reconfigurable LNA using proposed active inductor circuit will be discussed. LNA circuit will be analyzed and the simulation result will be compared. The tune-ability of frequency range for proposed circuit will be explained. In Chapter 5 the VCO circuit using proposed active inductor circuit will be explained and result will be shown. In chapter 6 the second active inductor circuit will be presented and in Chapter 7 the LNA circuit using the proposed active inductor circuit will be explained. In chapter 8 the third active inductor (differential active inductor) circuit is presented and also it is used in single-to-differential low noise amplifier(S-to-D-LNA) to show the application of this DAI circuit. And finally in chapter 9 the conclusion and some suggestion for future work will be given.

1.6 Contribution of the Thesis

The main aim of this research is focused on a tune-ability of active inductor circuit. Tune ability of active inductors is the main advantage of active inductors that qualified to use it in RF circuit. Because most of the RF circuit such as Filters and VCOs need to use a tunable inductor for frequency band selections. The contributions of this thesis are listed as follows:

i. Propose a first new active inductor circuit topology with wide tuning range (from 1 GHz up to 7 GHz) and high tunable inductance (from a few nH to 100 nH). The best performance of this circuit architecture is high tune-ability and linearity of the inductor for wide frequency range. A feedback resistor is used for tuning the active inductor circuit. Instead of a passive resistor, a PMOS transistor can be used as a resistor to expand the controlling of the active inductor circuit with voltage.

ii. Propose a second and new active inductor circuit topology with high tunable inductance (from a few nH up to 600 nH). The proposed active inductor

circuit uses current mirror circuit to increase inductance in new circuit topology. The extracted results show that the proposed active inductor has wide frequency range (from 1GHz to 4 GHz), high inductance (few nH up to 600 nH) and low power consumption (lower than 5 mW). In this active inductor topology, the power consumption is lower than the first active inductor circuit and also inductance value is higher than the first one.

iii. Propose a third differential active inductor circuit (DAI). It is designed to work in differential mode. The simulation results show the differential inductance is from a few nH to 500 nH and Q factor from 10 to 200 and power dissipation of 2.2 mW. The proposed DAI circuit is used in single-to-differential- LNA (S-to-D-LNA) to show the performance and applicability of DAI circuit.

iv. Design a reconfigurable LNA based on the proposed first active inductor circuit. In this circuit, the proposed active inductor circuit is used as an output load of the amplifier stage and act as a tunable and reconfigurable inductance. Tuning the frequency range of LNA is possible by tuning the active inductor core. In the active inductor core, tuning is done by using variable passive resistor or variable PMOS resistor. The flexibility of frequency band selection is one of the advantages of this circuit. The other advantages are small chip size and fully inductance-less circuit.

v. Design a wide tuning range VCO circuit using the proposed first active inductor circuit.

In this VCO circuit, the active inductor circuit is used instead of a spiral inductor in general VCO circuit architecture and in this VCO topology, the coarse frequency is achieved by tuning the integrated tunable active inductor circuit. In the active inductor circuit, the variable resistor (passive resistor or PMOS resistor) is used to tune the active inductor core.

vi. Design LNA circuit based on the proposed second active inductor circuit. In this circuit, the proposed high tunable active inductor circuit is used instead of the spiral inductor. A common source cascode amplifier with RC feedback is used in

LNA circuit topology as an amplifier stage. This circuit shows the application of the second active inductor circuit in terms of high inductivity.

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