LOW POWER LOW-DROPOUT VOLTAGE REGULATOR (LDO) WITH FAST LOAD TRANSIENT RESPONSE

LIM LAY LENG

UNIVERSITI TEKNOLOGI MALAYSIA

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Specially dedicated to my family, lecturers, fellow friends and those who have guided and inspired me throughout my journey of education

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ABSTRACT

With the recent explosion of devices driving “smart technologies” such as tablets, phones, all the portable and hand-held electronic devices such as cellular phones, PDA, MP3 players, GPS and other multi-media entertainments. The target for the portable battery operated product is towards reducing the number of battery cells, in order to decrease the cost and size. All these battery operated devices need power management circuits to work efficiently and extend the battery life, thus power regulation and power management have become one of the fastest growing sectors in the industry.The goal of this project is to design and implement a low power fully integrated CMOS low-dropout voltage regulator (LDO) based on quick response (QR) circuit to improve the load transient response. A 2.5V, 150mA with proposed high speed response circuit has been implemented in 0.25μm TSMC CMOS technology. The low-voltage operation ability, high current efficiency and low-voltage transient response performance can be achieved. With the small on-chip decoupling capacitor, the LDO with proposed QR circuit can achieve a fast load transient response with less transient overshoot or undershoot when instantaneous load fluctuation. By using the PMOS pass gate in the output stage we achieved a small regulator area and minimum dropout voltage for 100~150mA of output current. The proposed high speed response circuit included Memory circuit, PD_Charge and PD_Discharge circuit, Comparator and Vout_Discharge circuit.

ABSTRAK

Dengan perkembangan peranti-peranti baru yang digelar “teknologi pintar” seperti tablet, telefon, semaua peranti muday alih dan tangan elektronik seperti telefon bimbit, PDA, pemain MP3, GPS dan lain-lain hiburan multi-media. Sasaran untuk produk bateri mudah alih yang dikendalikan adalah tujuan untuk menuju ke arah mengurangkan bilangan sel-sel bateri, kos dan saiz. Semua alat-alat ini dikendalikan bateri perlu mengadakan pengurusan kuasa yang baik untuk memanjangkan hayat bateri. Pengurusan kuasa hayat bateri telah menjadi salah satu sektor yang paling pesat berkembang dalam industri. Objektif utama projek ini adalah untuk merekabentuk dan membina kuasa yang rendah bersepadu CMOS rendah keciciran pengatur voltan (LDO) berdasarkan maklum balas yang cepat (QR) litar untuk meningkatkan sambutan beban fana sepenuhnya. A 2.5V, 150mA dengan cadangan kelajuan tinggi respons litar telah dilaksanakan di 0.25μm TSMC CMOS teknologi. Keupayaan voltan rendah operasi, kecekapan tinggi semasa dan voltan rendah prestasi sambutan fana boleh dicapai.Dengan kapacitor yang kecil dalam kawasan silikon, LDO dengan litar QR yang dicadangkan boleh mencapai sambutan fana beban dengan cepat terlajak serta-merta apabila beban turun naik serta-merta.Dengan menggunakan pintu PMOS pas di peringkat keluaran kami mencapai kawasan pengatur kecil dan voltan keciciran minimum untuk 100 ~ 150mA output semasa.Litar yang digunakan dalam projeck ini termasuk litar Memori, PD_Charge dan litar PD_Discharge, Comparator dan litar Vout_Discharge.

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LIST OF ABBREVIATIONS

BJT		Bipolar Junction Transistor
CMP	-	Comparator
CMOS		Complementary Metal Oxide Semiconductor
HSLDO		High-Speed Low Dropout Voltage Regulator
LDO	-	Low Dropout Voltage Regulator
MOS		Metal Oxide Semiconductor
MOSFET		Metal Oxide Semiconductor Field Effect Transistor
PMOS		P-type metal-oxide-semiconductor
QR	-	Quick Response
SPICE	-	General-Purpose Circuit Simulation Program
TST	-	Test
VO		Output Voltage
VI		Input Voltage

CHAPTER 1

INTRODUCTION

This project is about the low power low-dropout voltage regulator (LDO) with fast load transient response. The low-dropout voltage regulator is implemented on 0.25µm TSMC CMOS technology using Tanner tools S-edit and L-edit v13.00. This chapter gives an overview of the whole project, starts with a brief introduction to the background, followed by the problem statement, project objectives, scope of work and report outline.

1.1 Background

In the new technology era, the technology is developing and growing everyday. Due to their portability and easy of handling, battery operated product become important in the Electronics market including industrial and automotive applications. The increasing demand for the portable battery operated products has driven power supply design towards low voltage and low quiescent current flow, for example all the portable and hand-held electronic devices such as cellular phones, PDA, MP3 players, GPS and other multi-media entertainments is evolving day by day. The target for the portable battery operated product is towards reducing the number of battery cells, in order to decrease the cost and size. All these battery operated devices need power management circuits to work efficiently and extend the battery life, thus power regulation and power management have become one of the fastest growing sectors in the industry.

Due to high fast transient in battery voltage, all battery operated applications demand a stable output voltage with the changing loading. Thus LDO become important in electronic industrial market. Low power regulator can provide more battery life, which makes it even more attractive for the consumer market. The demand for the low-voltage, low drop-out (LDO) regulator is increasing. Meanwhile low-dropout regulator has demonstrated its low noise high-accuracy and fast-response performance, and thereby is widely utilized to power up advanced analogue and radio-frequency integrated circuits. LDO required having a small active area and a small dip at the output voltage in order to reduce the cost development. Low dropout voltage regulators (LDOs) with fast load transient response are a critical power management module in modem portable devices

Now a day, the LDO design has become more and more challenging. This is due to increasing demand of the high-performance LDOs with low-voltage fast-transient. In this project the methods to improve the classical LDO structure have been proposed. However, the structural limitation, which is the main obstacle to simultaneously achieving stability, high output-voltage accuracy and short response time, still cannot be overcome.

For the sake of good understanding theoretical knowledge, gaining hand-on experience for whole processes of analog IC custom design and academic interests, the LDO regulator has been chosen as the final project for the course of Analog and Mixed – Signal IC Design. The design is based on variety of the state-of-the-art published structures, and designed experimental result can achieve proposed specifications.

In this project, I will present the design method of low power LDO with high-speed load transient response. It can catch instantaneous load fluctuation even though from low-power operating condition. Furthermore, on matter how fast the load changes, safe mechanism is proposed to prevent the LDO from falling into unstable state.

1.2 Motivation and Problem Statement

Increasing demand for portable battery operated products has driven power supply design towards low voltage and fast load transient response. The demand for high speed and processing power with efficient power consumption of IC or SOC leads to much more complex design for power supply. Low-dropout (LDO) voltage regulator are one of the most critical power management modules, as its can provide low-noise and precision supply voltages with the load changes instantaneously from un-load to full loaded states.

The heart of this project is to design and implemented a low power fully integrated CMOS low-dropout voltage regulator (LDO) based on quick response (QR) circuit to improve the load transient response.

An almost infinite variety exists of LDO implementations but nearly all of them comprise a power transistor, feedback network and error amplifier where the complexity of the amplifier varies depending on the performance requirements. Those LDO circuits described in the literature are typically optimized for a specific application with either challenging requirements for dropout, efficiency, power supply rejection or transient response time.

However a great need exists also for regulators with high-speed load transient response but smallest possible die area and power consumption. Especially in highly complex system-on chip designs, a large number of those simple regulators are required along the interfaces of the various sub-circuits. In spite of this wide demand, no literature exists on how to implement and optimize such a low cost, low complexity regulator circuit. This project will address this by presenting a low power, low dropout (LDO) voltage regulator with the proposed quick response (QR) circuit to improve the load transient response to achieve low transient overshoot and undershoot when driving a large load current.

1.3 Objectives

The objective of this project is to design Low-Dropout Voltage (LDO) Regulator and its application. This chapter will present the design methodology of the low power LDO with high-speed load transient response. The main objective of this project would be to design and develop a low power fully CMOS LDO based on quick response (QR) circuit to improve the load transient response which can catch instantaneous load fluctuation from low-power operating condition. Furthermore, this proposed circuitry will provide a stable output voltage no matter how fast the load changes. In this work, a 2.5V, 150mA LDO with the proposed quick response circuit has been designed and implemented in a 0.25µm TSMC CMOS technology using Tanner tools S-Edit for schematic capture and Layout the schematic in L-Edit. In the project, several design options and architectures are explored for performance trade-off analysis.

1.4 Scope of Work

The purpose of this project is to achieve a low dropout voltage, small output droop, fast load regulation and small silicon area LDO without utilizing a big capacitor. The proposed circuit consists of voltage reference circuit, Error amplifier circuit, memory circuit, comparator circuit, charge and discharge circuit, and pass element.

In major objective of this project is to study and understand Low-Dropout Voltage (LDO) Regulator and its application. There are few key considerations which would define the scope of work.

a) Conceptual design on systems level (top down design of block diagrams).

b) Breakdown of the system into smaller subsystems.

c) Schematic capture of the subsystem design, using devices realizable in the foundry technology, following a hierarchical approach (bottom up design) .

d) Netlist extraction of the schematic design to generate a SPICE netlist.

e) SPICE simulation of the individual subsystems, applicable interfaces and then the system as a whole.

f) Creation of layout cells (hierarchical)

g) Layout-vs-schematic (LVS) check.

h) Post-layout simulation is then done by extracting device information from the layout file.

i) Assessment of the results, and further refinements if required.

a 2D convolution algorithm is

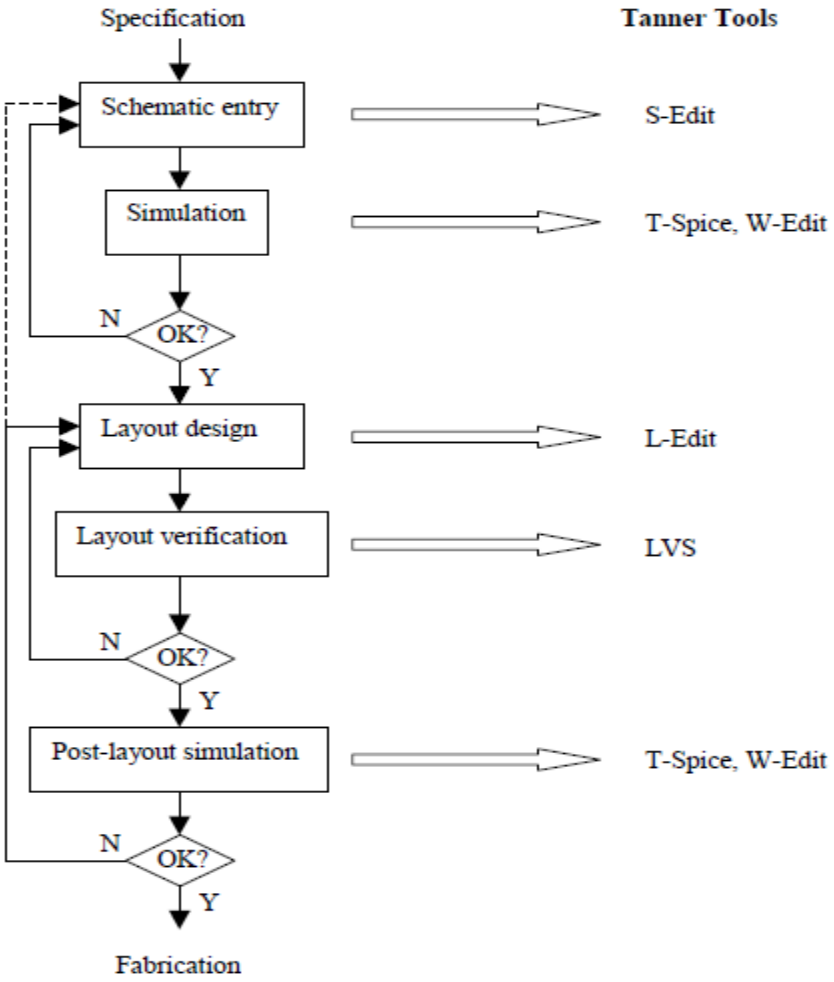

Figure 1.1 : Brief overview the steps of methodology and implementation plan.

- **Tanner Tools S-Edit v13.00**

- Tanner tools S-edit is used for schematic capture and netlist generation.
- Spice uses **model definitions** to obtain information on device parameters.
- The module ***schematic*** designed will result in SPICE netlist which will be used in T-Spice in the design process.

- **T-Spice and W-Edit**

- With a well created netlist, T-Spice serves as a very powerful SPICE engine. It is based on the industry standard Berkeley SPICE, with some added features.
- The netlists created will now be simulated and the results will be viewed using W-Edit.

- **Tanner Tools L-Edit Pro v13.00**

- L-Edit is a powerful layout program used to "paint" or define the devices as physical geometric features that is used to define the IC in terms of the foundry's process layers.
- Running DRC on the drawn transistor to verify that all of the design rules are met.
- Layout-vs-schematic (LVS) is a layout versus schematic program, to compare a schematic netlist to a netlist extracted from a layout file.
- To test and verify the validity of the design, a layout extraction is necessary. This netlist can be used for post-layout simulations.

1.5 Report Outline

The report is organized into 5 chapters namely the introduction, literature review and theory, methodology and design tool, 1D convolution modeling and design, 2D convolution modeling and design, design verification and performance analysis, and lastly the conclusion and future work.

Chapter 1 gives an overview of the project. It starts with a brief introduction to the background, followed by the problem statement, project objectives, scope of work and report outline.

Chapter 2 gives an overview on the prior work and literature review. Next, it introduces the theory of low dropout voltage regulator and the best topologies is chosen that offers low dropout voltage, small output droop, fast load regulation, and small silicon area in this project.

Chapter 3 describes the chosen circuitry and topologies and the project specification and methodology used.

Chapter 4 is the core chapter for this project report which discusses the architecture and design implementation. Simulation waveforms, testbench and design performance analysis are presented in this chapter as well. In this chapter, it will also show how the layout is done and post layout simulation results of the circuit.

Chapter 5 concludes what have the project achieve the fast load transient in terms of low-power design with power supply only 2.5V and lastly of the chapter are proposes the future works for further improvement and enhancement of the project.

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