FPGA IMPLEMENTATION OF A RECONFIGURABLE ADDRESS GENERATION UNIT FOR IMAGE PROCESSING APPLICATIONS

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Specially dedicated to my family, lecturers, fellow friends and those who have guided and inspired me throughout my journey of education

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ABSTRACT

Nowadays, the DSP algorithms are being widely used in the world of digital image processing. Example of the DSP algorithms that used in image processing is 2D correlation, 2D convolution, fast Fourier transforms, FIR filter and etc. The performance of the DSP algorithm is highly depends on its processing speed and memory bandwidth. Those algorithms require intensive data manipulation and calculation happens in parallel. The DSP algorithms also require complex address pattern calculation. The DSP processor needs to handle the data processing and also complex address calculation in the same time. The complex address pattern calculation using RISC processor is not efficient and therefore slower down the overall memory access speed. Hence, a dedicated hardware blocks to perform the address generation is essential. Such hardware known as Address Generation Unit(AGU). The prior arts of AGU have limitations as some of the AGU do not able to handle image edge condition and data reuse. Besides that, the prior art of the AGU have not been verified in the actual SOC environment. In this project, a reconfigurable AGU that targeted for 2D correlation, sum of absolute difference and Finite Impulse Response (FIR) is proposed. The proposed AGU able to take care of the image edge conditions by padding it with edge pixels. The proposed AGU also being integrated into the Altera Avalon fabric and fully verified in Altera DE2-70 FPGA. It also shows 30% to 40% improvements in the performance at certain area.

ABSTRAK

Pada masa kini, algoritma DSP digunakan secara luas dalam dunia pemprosesan imej digital. Algoritma DSP yang digunakan dalam pemprosesan imeg digital termasuk kolerasi 2D, convolution 2D, Fast Fourier Transform, penapis FIR dan lain lain. Prestasi algoritma DSP bergantung kepada kelajuan pemprosesan dan juga jalur lebar memori. Selain daripada itu, algoritma DSP juga memerlukan manipulasi data dan pengiraan alamat memori bercorak kompleks. Pemproses DSP perlu mengendalikan pemprosesan maklumat tersebut secara selari. Pemproses RISC diketahui kurang cekap dalam mengendalikan manipulasi data yang kompleks. Oleh kerana ini, blok perkakasan khusus untuk mengira alamat diperlukan. Perkakasan untuk mengira alamat dikenali sebagai Unit Generasi Alamat (AGU). Generasi AGU terlebih dahulu tidak mampu mengedalikan keadaan tepi imej dan mengguna semula data. Selain itu, generasi AGU terlebh dahulu tidak pernah disahkan dalam persekitaran SOC sebenar. Dalam projek ini, AGU yang boleh dikonfigur semula untik korelasi 2D, SAD dan penapis FIR dicadangkan. AGU tersebut berupaya mengendalikan keadaan tepi imej dan juga mengguna data semula. AGU tersebut akan dimasukkan ke dalam Altera Avalon Fabric dan dilaksanakan dalam papan Altera FPGA bermodel DE2-70. AGU yang dicadangkan juga mempunyai lebih kurang 30% ke 40% lebih laju daripada AGU terlebih dahulu dalam keadaan tertentu.

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AGU	-	Address Generation Unit
ASM	-	Algorithmic State Machine
DSP	-	Digital Signal Processing
FPGA	-	Field-Programmable Gate Array
RTL-CS	-	Register Transfer Level – Control Signal
FIR	-	Finite Impulse Response
SAD	-	Sum of Absolute difference
2D	-	Two Dimension

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CHAPTER 1

INTRODUCTION

1.1 Problem Background

Nowadays, digital signal processing (DSP) hardware required a large amount of processing elements running in parallel. Performance gain in a hardware system are achieved by using techniques such as pipelining, customized functional units, optimized memory hierarchies and running processes in parallel. Therefore large amount of the data access is needed.

Most of the DSP hardware is in cooperate with RISC processor. Manipulation with structure data-types are not efficiently supported by RISC processor. RISC processor is designed to have minimum number of instruction set and a complex compiler is needed. Hence, a considerable amount of codes need to be generated to cater the complex arithmetic manipulation that required by the DSP algorithm. This creates large amount of overhead on the performance of DSP hardware and many clock cycles are needed to fetch the data and instruction, decode, execute and process the data.

DSP algorithm can be used for image processing purposes. Images are stored in the memory, DSP processor are required to read the image from memory, process the image and store it back to the memory. Some of the DSP algorithm required complex address offset calculation and relying on software to calculate the address offset creates more overhead than a dedicated hardware for address calculation.

1.2 Problem Statement

There are several numbers of DSP algorithms which are being widely used for digital image processing. They are 2D convolution, 2D correlation, fast Fourier transforms (FFT), FIR filter and etc. Those algorithms require intensive index manipulations, resulting in complex address pattern. Complex address pattern calculation using RISC processor is in-efficient and it will slow down the overall system performance and resulting larger latency for accessing data.

Therefore, hardware accelerator is needed to speed up the address calculation and reduce the overall latency for accessing data rather than using software to do the address calculation. Such hardware accelerator for address calculation is known as Address Generation Unit (AGU).

Prior arts of reconfigurable AGU [1] only focus on the implementation for 2D correlation. It does not support the address generation for DSP algorithms other than 2D correlation. Furthermore, the prior arts of reconfiguration AGU [1] has only shows the Modelsim simulation results and never been implemented in FGPA.

Enhancement is needed to the design and more address sequences for different DSP algorithm need to be added. The AGU needs to be capable of generating one address per clock in required sequence [6].

1.3 Objective

The main objective of this project is to enhance the prior AGU and implement it to FPGA. The objectives that need to be achieved in this project are listed below:

1. Design a reconfigurable AGU that:
    - Capable to generate an address per clock.
    - Support windows based operation.

- Able to be used for various DSP applications.
- The RTL design needs to be able to configure easily through parameter.
- Support different image size and kernel size.
- Take care of image border and considering the data reuse.

2. Prototype and implement the design into the FPGA.

1.4 Scope of work

The project is targeted for the hardware architecture of Address Generation Unit (AGU) in Altera DE2-70 FPGA. The targeted DSP modules for the AGU in the project include 2D Correlation, Finite Impulse Response (FIR) and Sum of absolute difference (SAD). The DSP modules for targeted application are designed and work together with the AGU. The full design is then integrated to Altera Avalon Bus.

The AGU design is capable to generate an address per clock. Besides that, it also supports windows based operation with different kernel sizes and image dimension. The RTL is being parameterized and easy to be configured. The data reuse and image border consideration is being take care in the design as well.

MATLAB is being used to model the DSP algorithm and Modelsim is used as a simulator in the project. Altera Eclipse IDE is used as the environment to develop the C program to communicate with the design after the full integration of the design. Image pixels are extracted from simulation result in Modelsim and memory in the FPGA to compare with the output result from MATLAB.

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