A 10-BIT 50 MEGA-SAMPLES-PER-SECOND PIPELINED ANALOG-TO-DIGITAL CONVERTER

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ABSTRACT

Most of modern communication devices are implemented on portable systems powered by a battery with limited energy. Due to their dependence on batteries, some efforts have to be made to minimize the power consumption of these devices. One of the approaches is to use low power analog-to-digital converter (ADC). This thesis focuses on the design implementation of low power pipelined ADC for wireless communication system. The pipelined ADC was realized using 1.5-bit per-stage structures with digital error correction. For power reduction, dedicated front-end sample-and-hold circuit used in conventional pipelined ADC architecture is removed. Furthermore, power analysis has been performed using MATLAB® to assist in determining the best stage resolution in pipelined stages. A dynamic comparator is employed to optimize further the power consumption in pipelined stages. This low power pipelined ADC is implemented using Siltera's 0.18µm, 1.8-3.3V complementary metal oxide semiconductor process, with double layer poly-silicon and five metal layers. The designed pipelined ADC exhibits a 10-bit resolution at 50 Mega-Sample per-second and 50.82dB signal to noise and distortion ratio with an effective number of bits of 8.15-bit. The differential non-linearity (DNL) and the integral non-linearity (INL) are ±1 least-significant of bits (LSB). The power consumption is 97mW from a 3V supply and the entire area of the pipelined ADC including input and output pads is 2.4mm^2.

ABSTRAK

Hampir keseluruhan alat komunikasi moden diimplementasi pada sistem mudah alih yang dikuasai oleh tenaga bateri yang terbatas. Disebabkan oleh kebergantungan alat-alat kominukasi ini kepada bateri, sesuatu usaha perlu dilakukan untuk mengurangkan penggunaan kuasa mereka. Salah satu pendekatan ialah dengan menggunakan penukar analog kepada digital (analog-digital) yang berkuasa rendah. Tesis ini memberi tumpuan pada pelaksanaan rekabentuk penukar analog kepada digital jenis talian paip kuasa rendah untuk digunakan di dalam sistem komunikasi tanpa wayar. Penukar analog-digital talian paip ini dihasilkan dengan menggunakan struktur 1.5-bit disetiap peringkat bersama dengan litar pembetulan ralat. Untuk mengurangkan penggunaan kuasa, litar khusus untuk sampel dan pegang yang lazimnya digunakan di bahagian hadapan kebanyakan senibina penukar analog-digital talian paip telah disingkirkan. Tambahan lagi, analisis mengenai penggunaan kuasa di dalam beberapa struktur rekabentuk telah dilakukan dengan bantuan perisian MATLAB® bagi menentukan senibina terbaik untuk resolusi di dalam setiap peringkat talian-talian paip ini. Pembanding dinamik juga turut digunakan untuk mengurangkan lagi penggunaan kuasa di dalam semua peringkat talian-talian paip ini. Penukar analog-digital yang berkuasa rendah ini telah dihasilkan dengan menggunakan teknologi 0.18µm pelengkap logam oksida semiconduktor daripada Siltera dengan dua lapisan polisilikon dan lima lapisan logam. Penukar analog-digital yang telah direkabentuk ini berjaya mencapai resolusi 10-bit pada kelajuan 50 Mega sampel per satu saat dan nisbah isyarat kepada hingar dan herotan adalah 50.82dB. Disamping itu, nombor bit berkesan ialah 8.15-bit. Nilai ketaklurusan kebezaan dan ketaklurusan kamiran masing-masing ialah ±1 bit bererti terkecil. Penggunaan kuasa oleh penukar analog-digital yang direkabentuk ini ialah sebanyak 97mW pada voltan bekalan 3V dan seluruh keluasan bentangan termasuk pad masukan dan keluaran ialah 2.4mm^2.

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LIST OF ABBREVIATIONS

ADC	-	Analog to digital converter
CMFB	-	Common mode feedback
CMOS	-	Complimentary Metal Oxide Semiconductor
DAC	-	Digital to analog converter
DEC	-	Digital error correction
DNL	-	Differential non linearity
DPFM	-	Double poly five metals
ESD	-	Electro static discharge
ENOB	-	Effective number of bit
FFT	-	Fast Fourier Transform
GBW	-	Gain bandwidth
IF	-	Intermediate frequency
INL	-	Integral non linearity
I/O	-	Input-output
LNA	-	Low noise amplifier
LSB	-	Least significant of bit
LO	-	Local Oscillator
MDAC	-	Multiplying digital to analog converter
MSB	-	Most significant of bit
NMOS	-	n-channel metal oxide semiconductor
PMOS	-	p-channel metal oxide semiconductor
SAR	-	Successive approximate register
SC	-	Switch capacitor
SDR	-	Software defined radio

SFDR	-	Spurious free dynamic range
S/H	-	Sample and hold
SNR	-	Signal to noise ratio
SNDR	-	Signal to noise and distortion ratio
SR	-	Slew rate
Sub-ADC	-	Sub-Analog to digital converter
Sub-DAC	-	Sub-Digital to analog converter
THD	-	Total harmonic distortion
VGA	-	Variable gain amplifier

LIST OF APPENDICES

LIST OF PUBLICATIONS

NO.	TITLE
1	Yuzman Yusoff, Rohana Musa, Nazaliza Othman, Mohd Shahiman Sulaiman and Muhammad Nadzir Marsono. A High-Gain and High-Speed OTA for 10-bit 50MS/s Pipelined ADC. *Student Conference on Research and Development (SCORed)*, November 2008. Skudai, Malaysia: IEEE, 58-1 - 58-5.

CHAPTER 1

INTRODUCTION

Over the past few decades, silicon integrated circuit (IC) technology has evolved rapidly. This evolution has been driven mostly by the industry in digital circuits such as microprocessor and memories. As IC fabrication technology has improved, more analog signal processing functions have been replaced by digital circuitries. Despite of this trend, analog-to-digital converters (ADCs) play an important role in most modern electronic systems. The reason is that most of interests signals are analog in nature and must to be converted to digital signals for further signal processing in the digital domain [1].

ADC architectures include flash, pipelined, successive approximation, and sigma-delta; each with its own unique features. Which architecture for which application is typically determined by the speed and resolution requirements. Table 1.1 summarizes some of the ADC applications and their design constraints in terms of resolutions and sampling rates [2].

Table 1.1: ADC applications and their design constraints.

Area	System Applications	Resolutions	Sampling Rate
Wireline Communication	Gigabit Ethernet	6-7 bit	250 MS/s
	Fast Ethernet	7-8 bit	125 MS/s
	xDSL	13-16 bit	35 MS/s
Wireless Communication	Zero-IF Receiver: 802.11 WiMAX	10-14 bit	50-80 MS/s
	IF Sampling Multi-Standard: Software Radio Architectures	10-16 bit	10-100 MS/s
Audio and Video	CD/DVD Quality	24 bit	192 KS/s
	Imaging & Video Processing: Imaging Devices, HDTV	8-12 bit	40 MS/s
Instrumentations	Lab Bench Equipments: Digital Oscilloscope	8 bit	20 GS/s
	Scientific & Medical Equipments, Tester	12 bit	40 MS/s
Storage & Computing Devices	Hard Disk Drive	6-7 bit	0.5-1.5 GS/s
	Data Acquisition Cards	12-18 bit	1-100 MS/s

1.1 Motivation

In wireless telecommunication systems, the goal of the trend toward digitization is to move analog-to-digital converters (ADCs) close to the antennas so that all of the analog functions such as mixing, filtering, and demodulating can be implemented in the digital domain. Thus, one radio system can handle multiple standards by simply changing the programs in the digital signal processing block. This concept is known as

software-defined-radio (SDR) [3]. The system architecture of SDR receiver is shown in Figure 1.1.

Depending on the receiver architecture, analog filtering, and gain control range, the ADCs with a resolution of 10-16 bits and a sample rate between 10 and 100 MS/s are required [4]. Because of growing market on wireless digital communication, ADCs with medium-to-high resolutions and medium-to-high sampling rates are in high demand. However, since these kinds of ADCs are often designed solely for maximum speed, they tend to consume significant amount of power. Consequently, the demand for increased functionality in high-speed ADCs also carries with it the need for low power dissipation. As the above architecture is mostly used on mobile device, the power dissipation is an important design constraint and must be kept low to extend battery life.

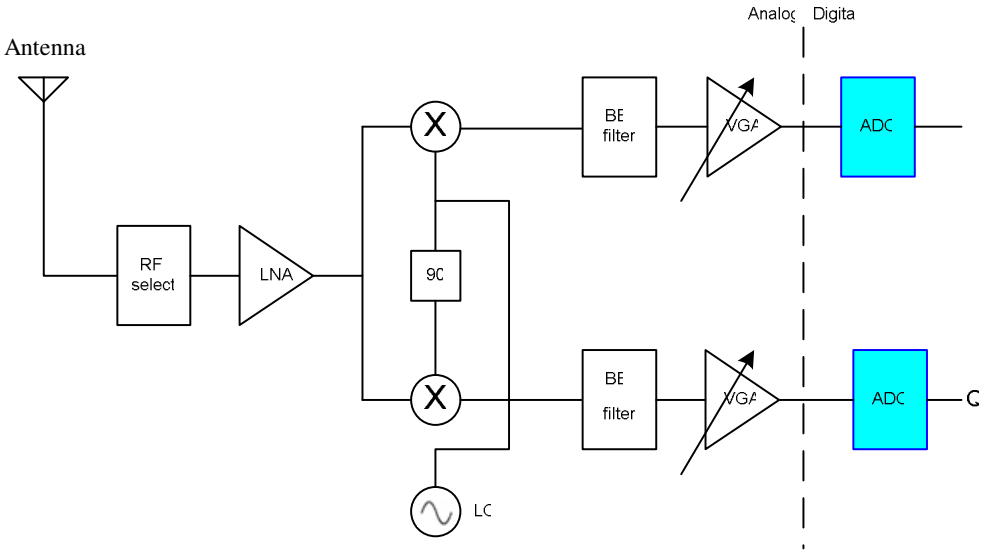

Figure 1.1 The direct conversion receiver architecture for SDR.

Another trend in implementing wireless telecommunication systems is toward higher-level circuit integration for lower cost and smaller feature size. The goal of this trend is to have a single chip solution, in which analog and digital circuits are placed on the same die with advanced CMOS technology. Although advanced fabrication technology benefits digital circuits, it poses great challenges for analog circuits. The

scaling of CMOS devices degrades important analog performance. For instance, lowering output resistance lowers amplifier gain, although cascading transistors or an added gain stage can compensate for this lowered gain. However, the use of cascoding transistors runs into a limitation on the number of transistors that can be stacked, a limitation that is imposed by the low power supply voltage of scaled CMOS technology. Turning to the solution of additional stages has the disadvantages of increased power dissipation and more complicated circuitry.

The low power supply voltage of scaled CMOS technology also limits the performance of analog circuits. Therefore, just as is the case with digital circuits, simply lowering the power supply voltage in analog circuits does not necessarily result in lower power dissipation. In addition, requirements for high gain and high speed make it more difficult to lower their power consumption. This is especially true for already complicated analog systems like ADCs; reducing their power consumption requires careful analysis of system requirements and special strategies.

1.2 Problem Statement

Most modern communication devices are implemented on portable systems powered by a battery with limited energy. Due to their dependence on batteries, some efforts have to be made to minimize the power consumption of these devices. One of the approaches is to use low power ADC. In this application, pipelined topology is the most promising ADC architecture. Its properties are suited to the system requirement that requires ADC with medium-to-high resolution and medium-to-high sampling rate. The pipelined architecture also can be easily calibrated for higher resolution and has potential for low voltage and low power operation. Thus, the objective of this work is to design a low power 10-bit 50MS/s (Mega-Sample per-second) pipelined ADC for wireless communication system applications.

1.3 Research Contribution

This research concentrates on pipelined ADC for wireless communication system. Requirements and optimization of the pipelined ADCs, at the circuit and architectural levels, are addressed to meet the specifications of this target application. Although the proposed ADC is designed according to the specifications of the target systems of wireless communication system, it can be exploited in other applications as well. Based on this research work, some of the analysis and circuit implementations have been partially reported in a related publication [5]. The contributions of this research work are:

(i) *Pipelined ADC MATLAB system model*: MATLAB behavior models are developed for the proposed pipelined ADC characterizations on its static and dynamic linearity.

(ii) *A low power 10-bit pipelined ADC architecture*: Different architectures on pipelined stages are investigated in order to determine the optimum bit per stage structure in term of low power operation.

(iii) *Transistor level pipelined ADC sub-circuits design and analysis*: The ADC sub-blocks such as amplifiers, comparators, non-overlapping clock generator, switches, and digital error correction are designed and simulated at circuit level.

(iv) *Pipelined ADC layouts*: The layout for 10-bit 50MS/s Pipelined ADC is implemented using Siltera's 0.18um CMOS process with double poly-silicon and five metals technology. All techniques such as common-centroid, cross-coupled, interdigitation, and IC decoupling are employed in this layout to reduce parasitic effects.

1.4 Thesis Organization

The rest of the thesis is organized as follows. Chapter 2 presents the literature review of ADCs and it is divided into three small sections. First, Section 2.1 describes the importance of ADC performance parameters. Section 2.2 presents an overview of various ADC architectures. In section 2.3, the pipelined ADC is presented in more details on its basic operation and sub-blocks. Chapter 3 describes system architecture for the proposed pipelined ADC as well as some analysis on its power optimization. Chapter 4 details the design implementation of 10-bit 50MS/s pipelined ADC covering all its sub-components including the amplifier, comparator, and digital error correction circuit. Chapter 5 assesses the performance of the designed 10-bit 50MS/s pipelined ADC. The thesis summary, research contribution, and direction for future works are in Chapter 6.

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