CHARACTERISATION OF BALLISTIC CARBON NANOTUBE FIELD-EFFECT TRANSISTOR

RAHMAT BIN SANUDIN

UNIVERSITI TEKNOLOGI MALAYSIA

CHARACTERISATION OF BALLISTIC CARBON NANOTUBE
FIELD-EFFECT TRANSISTOR

RAHMAT BIN SANUDIN

A project report submitted in partial fulfilment of the
requirements for the award of the degree of
Master of Engineering (Electrical - Electronics & Telecommunications)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

NOVEMBER 2005

To my beloved parents and wife

ACKNOWLEDGEMENT

I would like to thank my supervisor, Associate Professor Dr. Razali Ismail, for giving me the opportunity to work on this project for two semesters; his advice, comments, support, and contacts have been invaluable. These past two semesters have been a struggle for me at times; however, I have learned an enormous amount. Without a strong background, this field was difficult to enter and hard to find a focused project; however the discussions and advice on the topic with my supervisor were very helpful. Also, his comments on my thesis were especially enlightening.

I would like to thank research group at Purdue University, West Lafayette. Their response to my email regarding the device simulation in MATLAB is truly helpful. It was wonderful to have the perspective and knowledge of someone working on research within the nanotube field. I would not have been producing the simulation result as presented in this thesis without the help and support from these people.

And last but not at all least, I would like to thank my family especially my wife who had gotten me through everything, good and bad. I do not know how to thank her enough with her endless amount of thought provoking comments and confidence. Thank you also to all my colleagues, who are very supportive and others who have provided assistance at various occasions.

ABSTRACT

Scaling process of silicon transistor, particularly MOSFET, in the past decades had increased the performance of silicon transistor with reduction of its size. However, the scaling process will eventually reaches its limit and by that time a new group of devices are expected to replace MOSFET in digital applications. This group of devices, known as nanoelectronic devices, is expected to offer better device geometry in nanometre scale with superior performance. Carbon nanotube field-effect transistor (CNFET), one of nanoelectronic devices, is a transistor with its channel is made of carbon nanotube and it is designed to provide the solution for scaling process and the possibility of coexistence with current silicon technology. The purpose of this project is to study the behaviour of CNFET and the main focus is on the simulation of its current-voltage (I-V) characteristic. The simulation study is carried out using MATLAB program and the result obtained is used to compare the device performance with MOSFET. Further analysis is also made to see the effect of oxide thickness and carbon nanotube diameter on the device performance, in particular the drain current. From the simulation study, it is concluded that the performance of CNFET has no significant advantage over MOSFET and its performance is also affected by both nanotube diameter and oxide thickness.

ABSTRAK

Proses penskalaan terhadap transistor silikon, terutamanya MOSFET, selama beberapa dekad yang lalu telah berjaya memperbaiki pencapaian peranti ini serta mampu mengurangkan saiz peranti ini. Namun, proses ini akan tiba di had keupayaannya dan pada masa itu beberapa peranti baru akan menggantikan MOSFET dalam aplikasi digital. Kumpulan peranti ini, yang dikenali sebagai peranti elektronik-nano, dijangka akan memberikan bentuk peranti yang lebih baik dalam skala nanometer dan juga pencapaian yang mengkagumkan. Transistor tiub-nano karbon (CNFET), salah satu daripada peranti elektronik-nano, merupakan transistor yang mempunyai saluran yang diperbuat daripada tiub-nano karbon dan ianya direkabentuk untuk memberikan penyelesaian terhadap masalah penskalaan dan berkemungkinan untuk diintegrasikan bersama teknologi silikon. Tujuan projek ini adalah untuk mengkaji sifat peranti ini dan fokus utama diberikan kepada simulasi terhadap sifat arus-voltan (I-V) peranti ini. Kajian simulasi ini dibuat menggunakan program MATLAB dan hasil keputusan yang dicapai akan digunakan untuk membandingkan pencapaian peranti ini dengan MOSFET. Analisis selanjutnya dilakukan untuk melihat kesan diameter tiub-nano karbon dan ketebalan oksida terhadap pencapaian peranti ini, atau lebih tepat lagi terhadap arus drain. Hasil keputusan yang dicapai daripada kajian simulasi mendapati bahawa pencapaian peranti ini tidak mempunyai kelebihan yang nyata berbanding MOSFET dan pencapaian peranti ini juga dipengaruhi oleh diameter tiub-nano karbon serta ketebalan oksida.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

α_D	-	Coefficient of drain capacitance
α_G	-	Coefficient of gate capacitance
α_S	-	Coefficient of source capacitance
C_D	-	Drain terminal capacitance
C_G	-	Gate terminal capacitance
C_S	-	Source terminal capacitance
C_Σ	-	Total capacitance
$D(E)$	-	Carbon nanotube density of states at top of the barrier
E_{F1}	-	Source Fermi level (eV)
E_{F2}	-	Drain Fermi level (eV)
$f(E)$	-	Probability that a state with energy E is occupied
h	-	Planck's constant (eV-s)
I_0	-	Extrapolated current per width at threshold voltage
I_D	-	Drain current (I)
I_{ON}	-	On-current
I_{OFF}	-	Leakage current
k_B	-	Boltzmann's constant (eV/K)
m	-	Gate voltage swing required per unit of electron potential
N_0	-	Equilibrium electron density at top of the barrier
N_1	-	Positive velocity states filled by source
N_2	-	Negative velocity states filled by drain
q	-	Electronic charge (C)
T	-	Operating temperature (K)
U_L	-	Laplace potential
U_P	-	Potential due to mobile charge
U_{scf}	-	Self-consistent potential at top of the barrier
V_D	-	Drain voltage (V)

V_G	-	Gate voltage (V)
V_S	-	Source voltage (V)
V_t	-	Threshold voltage (V)

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

As an introduction, this chapter presents the objectives and scopes of this project and background of this project. This chapter also gives outline of this thesis as well as summary of content for each chapter.

1.1 Project Objectives

The main interest of this project is to study the characteristic one nanoelectronic device. Ballistic carbon nanotube field-effect transistor (CNFET) is chosen as one of nanoelectronic devices that have great potential to be the switching device for future. The main objectives of this project are as follows:

a) Understand the device characteristic, fundamental equation and mathematical model of CNFET.
b) To attain and investigate the I-V characteristics of CNFET.

The means through which the main objectives could be achieved are:

a) To study the behaviour of carbon nanotube, the most important material that is used to build CNFET.
b) Identify the most suitable structure of CNFET that can promote ballistic transport.

1.2 Scope of Project

The scope of this project is to carry out simulation study of carbon nanotube field-effect transistor using MATLAB program based on the mathematical model. The structure of MOSFET-like CNFET is used in this project because this structure has better performance than Schottky-barrier CNFET (SB-CNFET). The simulation result is then compared with MOSFET in order to measure the level of CNFET performance.

1.3 Layout of Thesis

This thesis consists of six chapters beginning with this chapter. Chapter 1 gives the objectives and scope of the project as well as the layout of thesis.

Chapter 2 presents an overview of nanoelectronic devices such as single electron transistors, resonant tunnelling diode and carbon nanotube field-effect transistor. This chapter also discussed the limiting factors that prevent improvement in MOSFET performance as its size is kept on shrinking.

Chapter 3 is dedicated to carbon nanotube, the material used as transistor channel in CNFET. This chapter discussed the background of carbon nanotube, its basic structure as well as its properties that make it very special material. Growth technique of this material is presented briefly to give an overview of how this material is produced.

Chapter 4 deals with CNFET, the basis of research in this project. It starts with its structure, followed by simple explanation on its operation and finally the applications associated with this device.

Chapter 5 presents the simulation result of this project. This result is then analysed through comparison with MOSFET and also factors that affects the performance of CNFET.

Finally, Chapter 6 gives conclusion for the whole project. This chapter also presents several recommendations for future work.

REFERENCES

1. Goldhaber-Gordon, D. et. al. Overview of Nanoelectronic Devices. 1997. *Proceedings of The IEEE*. 85(4): 521-540.
2. Neamen, D. A. *Semiconductor Physics and Devices*, Third Edition. Avenue of Americas, NY: McGraw-Hill. 2003.
3. Bohr, M. T. Nanotechnology Goals and Challenges for Electronic Applications. 2002. *IEEE Transactions on Nanotechnology*. 1(1): 56-62.
4. Compano, R. ed. *Technology Roadmap for Nanoelectronics*. Microelectronics Advanced Research Initiative. 2000.
5. Keshavarzi, A., Roy, K. and Hawkins, C. F. Intrinsic Leakage in Deep Submicron CMOS ICs - Measurement-Based Test Solutions. 2000. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 8(6): 717-723.
6. Chen, Z. et. al. I_{DDQ} Testing for Deep-Submicron ICs: Challenges and Solutions. 2002. *IEEE Design and Test of Computers*. 24-33.
7. Chang, L. *Ballistic Transport in Silicon MOSFET's*. 2000. unpublished.
8. Taur, Y. CMOS design near the limit of scaling. 2002. *IBM J. Ref. & Dev*, 46(2): 213-220.
9. Korotkov, A. N. *Coulomb Blockade and Digital Single Electron Devices*. 1996. *Molecular Electronics*. 157-189
10. Hadley, P., Lientschnig, G., and Lai, M. J. *Single-Electron Transistors*. 2003. Institute Of Physics Conference Series. 174: 125-132.
11. Goodnick S. M. and Bird, J. Quantum Effect and Single Electron Devices. 2003. *IEEE Transaction on Nanotechnology*. 2(4): 368-383.
12. Likharev, K. K. Single-Electron Devices and Their Applications. 1999. *Proceedings of The IEEE*, 87(4):606-632.
13. Lageweg, C., Cotofanˇa, S. and Vassiliadis, S. Single Electron Encoded Latches and Flip Flops. 2004. *IEEE Transactions on Nanotechnology*, 3(2): 37-248.

14. Takahashi, Y. et. al. *Silicon Single-Electron Devices and Their Applications*. 2000. *Proceedings of 30th IEEE International Symposium on Multiple-Valued Logic*. 411-420.

15. Mathews, R. H. A New RTD-FET Logic Family. 1999. *Proceedings of The IEEE*, 87(4): 596-605.

16. Avouris, P. et. al. Carbon Nanotube Electronics. 2003. *Proceedings of The IEEE*. 91(11): 1772-1784.

17. Guo, J. and Lundstrom, M. S. A Computational Study of Thin-Body, Double-Gate Schottky Barrier MOSFETs. 2002. *IEEE Transactions on Electron Devices*. 49(11): 1897-1902.

18. Huang, C. K., Zhang, Z. E. and Yang, C. H. Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10nm. 1998. *IEEE Transactions on Electron Devices*. 45(4): 842-847.

19. Ren, Z. et. al. The Ballistic Nanotransistors: A Simulation Study. 2000. *Proceedings of IEDM*.

20. Naveh, Y., Likharev, K. K., Modeling of 10-nm-Scale Ballistic MOSFET's. 2000. *IEEE Electron Device Letters*, 21(5): 242-244.

21. Rahman, A. et. al. Theory of Ballistic Nanotransistors. 2003. *IEEE Transactions on Electron Devices*, 50(9): 1853-1864.

22. Dresselhaus, M. S. and Avouris, P. Introduction to Carbon Materials Research. In: Dresselhaus, M. S., Dresselhaus, G. and Avouris, P. eds. *Carbon Nanotubes: Synthesis, Structures, Properties and Applications.* Berlin, Germany: Springer-Verlag Berlin Heidelberg. 1-9; 2001.

23. Saito, R., Dresselhaus, G. and Dresselhaus, M. S. *Physical Properties of Carbon Nanotubes*. Imperial College London: Imperial College Press. 1998.

24. Forro, L. and Schoenberger, C. Physical Properties of Multi-wall Nanotubes. In: Dresselhaus, M. S., Dresselhaus, G. and Avouris, P. eds. *Carbon Nanotubes: Synthesis, Structures, Properties and Applications.* Berlin, Germany: Springer-Verlag Berlin Heidelberg. 329-390; 2001.

25. Hoenlein, W. et. al. Carbon Nanotube Applications in Microelectronics. 2004. *IEEE Transactions on Components and Packaging Technologies*. 27(4): 629-634.

26. McEuen, P. L., Fuhrer M. S. and Park, H. Single-Walled Carbon Nanotube Electronics. 2002. *IEEE Transactions on Nanotechnology*. 1(1): 78-85.

27. Avouris, P. Molecular Electronics with Carbon Nanotube. 2002. *Accounts of Chemical Research*. 35(12): 1026-1034.

28. Tans, S. J. et. al. Individual single-wall carbon nanotubes as quantum wires. 1997. *Nature*. 386(3): 474-477.

29. Yao, Z., Dekker, C. and Avouris, P. Electrical Transport Through Single-Wall Carbon Nanotube. In: Dresselhaus, M. S., Dresselhaus, G. and Avouris, P. eds. *Carbon Nanotubes: Synthesis, Structures, Properties and Applications*. Berlin, Germany: Springer-Verlag Berlin Heidelberg. 147-171; 2001.

30. Dai, H. Nanotube Growth and Characterization. In: Dresselhaus, M. S., Dresselhaus, G. and Avouris, P. eds. *Carbon Nanotubes: Synthesis, Structures, Properties and Applications*. Berlin, Germany: Springer-Verlag Berlin Heidelberg. 55-80; 2001.

31. Scott, C. D. Growth mechanisms for single-walled carbon nanotubes in a laser ablation process. 2001. *Applied Physics A*. 72: 573-580.

32. Nikolaev, P. et. al. Gas-phase catalytic growth of single-walled carbon nanotubes from carbon monoxide. 1999. *Chemical Physics Letters*. 313: 91-97.

33. Martel, R. et. al. Carbon Nanotube Field-Effect Transistors and Logic Circuits. 2002. *Proceedings of the 39th Conference on Design Automation***.** 94-98.

34. Choi, W. B. et. al. Aligned carbon nanotubes for nanoelectronics. 2004. *Institute of Physics Publishing*. 15: 512-516.

35. Heinze, S., Tersoff, J. and Avouris, P. *Carbon Nanotube Electronics and Optoelectronics*. Institute of Applied Physics, University of Hamburg. unpublished.

36. Derycke, V. et. al. Carbon Nanotube Inter- and Intramolecular Logic Gates. 2001. *Nano Letters*. 1(9): 453-456.

37. Bachtold, A. et. al. Logic circuits based on carbon nanotubes. *Physica E*. 2003. 16: 42-46.

38. Guo, J. et. al. *Predicted Performance Advantages of Carbon Nanotube Transistors with Doped Nanotubes as Source/Drain*. School of ECE, Purdue University, West Lafayette. unpublished.

39. Guo, J., Datta, S., Lundstrom, M. Assessment of Silicon MOS and Carbon Nanotube FET Performance Limits Using General Theory of Ballistic Transistors. 2002. *International Electron Devices Meeting (IEDM)*. 711-715.