QUANTUM MECHANICAL EFFECTS ON THE PERFORMANCE OF STRAINED SILICON METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR

KANG ENG SIEW

UNIVERSITI TEKNOLOGI MALAYSIA

QUANTUM MECHANICAL EFFECTS ON THE PERFORMANCE OF STRAINED SILICON METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR

KANG ENG SIEW

A thesis submitted in fulfilment of the
requirements for the award of the degree of
Doctor of Philosophy (Electrical Engineering)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

FEBRUARY 2013

To my beloved family

ACKNOWLEDGEMENT

There are many people who I would like to thanks for their helps and encouragements that they have given me over the past four years. First and foremost, I would like to express my greatest gratitude and deep appreciation to my project supervisor, Prof. Dr. Razali Ismail, for all his guidance and support throughout the course of my degree. His enormous moral support and guidance are worthy of my gratitude from the bottom of my heart. His advices, feedbacks and patience are invaluable, especially when the confusion struck and disorientation caught me in the middle of the road.

Nonetheless, I would like to acknowledge the support I received from Prof. Sohail Anwar (Pennsylvania State University, USA), who provided me with much valuable guidance and advices. He is also a great advisor in the writing for publication papers, which greatly influence the development of my professional writing skills. My appreciation also goes to Dr. Amit Chaudhry (Panjab University, India) for sharing his knowledge with me and being the source of support in variety ways.

In addition, special thanks to my colleague in the Computational Nanoelectronics (CoNe) research group for all the helps that they have given me, namely Yau Wei Heong, Jatmiko Endro Susendo, Munawar Agus Riyadi, Zaharah Johari, Noraliah Aziziah, Fatimah Abdul Hamid, Siti Norazlin Bahador and Muhammand Afid Nuruddin. Furthermore, a note of appreciation goes to

Nanoelectronics Laboratory staff, particularly Mohd Helmi Bin Dollah and Hj. Anuar Bin Yusof, for their favors.

I also hereby gratefully honored the financial support from the National Science Foundation (NSF) grant of the Ministry of higher Education (MOHE). Also thanks to the Research Management Centre (RMC) of Universiti Teknologi Malaysia (UTM) for providing an excellent research environment in which to complete this work.

On a personal note, I would like to thanks my family in Kelantan for all the supports and encouragements, without which I would never even have considered doing this research. Their firm supports and understanding have been a part of my spirit and soul. Special thanks to my friend, Chow Wai Leong who offered me ear, shoulder and moments that help me to release the stress along doing this research.

Finally, I would like to dedicate this dissertation to the memory of my younger brother, Kang Yun Thern.

ABSTRACT

In recent development of nanoelectronic devices, strained silicon Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has been identified as a promising structure for the future nanoscale device. Strained silicon is an attractive option due to the enhanced carrier mobility, high field velocity and carrier velocity overshoot. However, the aggressive geometry scaling has approached a limit where the classical mechanism is insufficient to clarify the characteristics of nanoscale MOSFET accurately. Beyond the classical limit, quantum-mechanical model becomes necessary to provide thorough assessment of the device performance. This research describes the modeling of nanoscale strained silicon MOSFET taking into account the critical quantum mechanical effects in terms of energy quantization and carrier charge distribution. Technology-Computer-Aided-Design (TCAD) simulations that apply the classical mechanisms are conducted to allow comparison with the developed models. It is shown that quantum mechanical effects become more dominant at channel length below 60nm. Significant discrepancy of threshold voltage as high as 90mV is found particularly in short channel regimes. The analytical model was also extended to the advanced structure of dual channel that provides higher electron and hole mobility compared to strained silicon MOSFET. The models were subsequently compared to the TCAD simulation results using a similar set of parameters as well as to the existing data from other literatures. Excellent agreements validate the models based on the physics of the quantum mechanical effects. In addition, the current-voltage model incorporating the quantum mechanical correction was also developed. The role of quantum capacitance over current drive in the channel was discussed. The developed models successfully replicate experimental data with proper physical explanation.

ABSTRAK

Pada era pembangunan peranti elektronik masa kini, penegang silikon semikonducktor oksida logam transistor kesan medan (MOSFET) telah dikenal pasti sebagai struktur semikonductor berukuran nano masa hadapan. Penegang silicon merupakan satu opsyen yang menarik disebabkan peningkatan dalam kebolehgerakan pengangkut, kelajuan medan tinggi dan kelajuan terlanjak. Tetapi, skala geometri yang agresif telah mencapai satu tahap dimana mekanisme klasikal tidak mencukupi untuk menerangkan tingkah laku MOSFET nano. Pada had melebihi fizik klasikal ini, model kuantum mekanik diperlukan bagi menyediakan satu penilaian penuh ke atas prestasi peranti. Kajian ini menerangkan model penegang silicon MOSFET nano yang menggabungkan kesan kritikal kuantum mekanik dari segi pengkuantuman tenaga dan taburan cas pengangkut. Teknologi-Reka Bentuk-Berpandukan-Komputer (TCAD) yang menggunakan mekanisme klasik dilakukan untuk membenarkan perbandingan dengan model-model yang dibangunkan. Ia menunjukkan bahawa kesan kuantum mekanik menjadi lebih dominan pada lebar saluran di bawah 60nm. Perbezaan ketara dalam voltan ambang setinggi 90mV ditemui terutamanya pada bahagian saluran pendek. Model analisis ini juga diperkembangkan untuk struktur dua saluran yang menyediakan kebolehgerakan yang lebih tinggi untuk elektron dan lubang berbanding dengan penegang silicon MOSFET. Model ini kemudiannya dibandingkan dengan TCAD dengan menggunakan satu set parameter yang serupa serta data yang sedia ada dari sumber literasi. Persamaan baik yang diperolehi mengesahkan teori fizik yang mengambil kira kesan kuantum mekanik. Tambahan pula, persamaan arus-voltan yang mengambil kira kesan kuantum mekanik turut diperolehi. Peranan kemuatan kuantum ke atas arus saluran turut dibincangkan. Model-model yang dibangunkan berjaya menepati data eksperimen dengan penerangan fizikal yang tepat.

TABLE OF CONTENTS

CHAPTER	TITLE		PAGE
	DECLARATION		ii
	DEDICATION		iii
	ACKNOWLEDGEMENTS		iv
	ABSTRACT		vi
	ABSTRAK		vii
	TABLE OF CONTENTS		viii
	LIST OF TABLES		xii
	LIST OF FIGURES		xiii
	LIST OF ABBREVIATIONS		xvii
	LIST OF SYMBOLS		xix
	LIST OF APPENDICES		xxii
1	**INTRODUCTION**		**1**
	1.1	Background	1
	1.2	Problem Statement	3
	1.3	Research Objectives	5
	1.4	Research Scopes	5
	1.5	Thesis Organization	7
2	**LITERATURE REVIEW**		**9**
	2.1	Introduction	9
	2.2	Geometry Scaling of MOSFETs	10
	2.3	International Technological Roadmap	12

	Semiconductor	
	2.4 Silicon Material Properties	16
	2.5 Strained Silicon Technology	17
	2.5.1 Formation of Biaxial Strained Si	20
	2.5.2 Physics of Biaxial Strained Si	22
	2.5.2.1 Biaxial Tensile Strain	22
	2.5.2.2 Biaxial Compressive Strain	25
	2.6 Dual Channel Heterostructure	27
	2.7 Quantum Mechanical Effects	30
	2.8 Threshold Voltage Model	33
	2.8.1 Long Channel Strained Si	34
	2.8.2 Short Channel Strained Si	35
	2.8.3 Review of Published Models	37
	2.9 Carrier Statistic and Velocity Saturation	39
	2.10 Current-Voltage Characteristic	44
	2.11 Summary	46
3	**RESEARCH METHODOLOGY**	**48**
	3.1 Introduction	48
	3.2 Research Flowchart	49
	3.3 Device Simulation and Characterization Approach	51
	3.4 Analytical Modeling Approaches	53
	3.4.1 MATHEMATICA	54
	3.4.2 MATLAB	55
	3.5 Summary	55
4	**QUANTUM MECHANICAL EFFECTS ON THE THRESHOLD VOLTAGE NANOSCALE STRAINED SI MOSFET**	**56**
	4.1 Introduction	56
	4.2 Device Structure and Simulation Procedure	57
	4.2.1 Strained Silicon NMOSFET	57

		4.2.2 Dual Channel Heterostructure	61
	4.3	Threshold Voltage Modeling of Strained Si NMOSFET	62
		4.3.1 Strain Effects on Energy Band Diagram	62
		4.3.2 Quantum Mechanical Effects (QMEs)	64
		4.3.3 Surface Potential Formulation	66
		4.3.4 Threshold Voltage Formulation	71
		4.3.5 Results and Discussions	74
	4.4	Threshold Voltage Modeling of Dual Channel Heterostructure	78
		4.4.1 Strain Effects on Energy Band Diagram	79
		4.4.2 Surface Potential Formulation	80
		4.4.3 Threshold Voltage Formulation	86
	4.5	Threshold Voltage Modeling of Dual Channel Heterostructure using Three Potentials Terms	88
		4.4.1 Results and Discussions	91
	4.6	Summary	95
5	**QUANTUM MECHANICAL EFFECTS ON THE CURRENT-VOLTAGE CHARACTERISTIC OF NANOSCALE STRAINED SI MOSFET**		**97**
	5.1	Introduction	97
	5.2	Two-dimensional Energy Spectrum	98
	5.3	Modeling of Intrinsic Velocity	102
		5.3.1 Non-Degenerate Regime	105
		5.3.2 Degenerate Regime	107
	5.4	Low Field Mobility	109
	5.5	Current-Voltage Characteristic	110
	5.6	Summary	115
6	**CONCLUSION AND RECOMMENDATION**		**116**
	6.1	Conclusions	116
	6.2	Main Contributions of Research	118

6.3 Recommendations for Future Works 119

REFERENCES 121

Appendices A -G 136 - 162

LIST OF TABLES

TABLE NO.	TITLE	PAGE
2.1	2011 ITRS roadmap for High Performance (HP) logic technology requirement	13
2.2	The properties of Si and Ge	17
2.3	Review of the published QMEs models.	32
2.4	Threshold voltage models developed by various authors.	37
3.1	Model parameters available in Silvaco’s ATLAS	52

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
2.1	Accelerated scaling of physical channel gate length of nanometer-scale CMOS transistor. (ITRS, 2011)	12
2.2	The potential solutions addressed by ITRS 2011	15
2.3	Direction of force experienced by (a) biaxial strain silicon and (b) uniaxial strain silicon in crystal lattice form	18
2.4	Schematic feature of uniaxial strained technology: (a) embedded SiGe in the source and drain for compressive strain PMOS and (b) SiN capping for tensile strain NMOS (Acosta and Sood, 2006)	19
2.5	The approach to induce biaxial strained on $Si_{1-x}Ge_x$ virtual substrate	20
2.6	Schematic illustration of (a) lattice constant of Si to be grown on top of SiGe (b) lattice distortion when Si thin film being tensile strained (c) lattice constant of SiGe film to be grown on top of Si film and (d) lattice distortion when SiGe film being compressively strained (Paul, 2004)	21
2.7	Schematic illustration of conduction band splitting due to the tensile strained Si	22
2.8	Schematic illustration of valence band splitting for (a) conventional bulk Si and (b) tensile strained Si on relaxed $Si_{1-x}Ge_x$	23
2.9	Effective electron mobility in tensile strained Si inversion layer compared to the universal mobility (Maiti et al, 2007)	24

2.10	Hole mobility enhancement in tensile strained Si_1 inversion layer (Maiti et al, 2007)	24
2.11	Schematic of conduction band splitting due to the compressive strained $Si_{1-y}Ge_y$	25
2.12	Schematic of valence band energy versus k (a) conventional bulk Si and (b) Compressive $Si_{1-y}Ge_y$ on Relaxed Si	26
2.13	Schematic diagram of electron and hole mobility in tensile strained Si channel and compressive strained $Si_{1-y}Ge_y$ channel respectively (Yeo et al, 2000)	27
2.14	Dual channel layer structure incorporated a compressively strained $Si_{1-y}Ge_y$ layer between strained Si and relaxed $Si_{1-x}Ge_x$ virtual substrate	28
2.15	Schematic energy band alignment of dual channel heterostructure under inversion for n- and p-channel devices (Olsen et al, 2004)	28
2.16	PMOS mobility in strained Si channel and dual channel heterostructure (Åberg et al, 2006)	29
2.17	Discrete energy spectrums due to energy quantization	31
2.18	Schematic diagram illustrates the peak carrier distribution is shifted away from the Si/SiO_2 interface by a constant of Δz	31
2.19	Long channel strained Si MOSFET	34
2.20	Short channel strained Si MOSFET	36
2.21	Low dimensional system for (a) 3D (b) 2D and (c) 1D	40
2.22	Comparison of *I-V* characteristic where short channel device displays an extended saturation region due to velocity saturation	45
3.1	Research methodology flowchart that describes the overall research sequences	50
4.1	Fabrication steps for strained Si NMOSFET	59
4.2	The flowchart for the fabrication process	60
4.3	The cross section of dual channel heterostructure using TCAD tools	61
4.4	Strained Si n-channel MOSFET which show the quantum	65

correlation constant in the channel

4.5 Variation of effective oxide thickness with Δz 66

4.6 The schematic cross section of a tensile strained Si/relaxed $Si_{1-x}Ge_x$ architecture 66

4.7 Distribution of surface potential variations along 30nm channel length for strained Si with 20% germanium content 71

4.8 Threshold voltage comparison between analytical model and TCAD simulation for sub 120 nm channel lengths 75

4.9 Threshold voltage variations with decreasing Ge content for short channel length (30 nm) and long channel length (100 nm) 75

4.10 Threshold voltage performance versus strained silicon thickness for L=30 nm, 50 nm and 100 nm for 30% Ge content in $Si_{1-x}Ge_x$ substrate 77

4.11 Comparison of DIBL in different channel length for T_{si} = 5 nm and T_{si} = 10 nm 78

4.12 The schematic cross section of strained Si/Strained $Si_{1-y}Ge_y$/relaxed $Si_{1-x}Ge_x$ dual channel architecture 79

4.13 Variation of the flatband voltage difference, V_{fb} versus the substrate doping for oxide thickness T_{ox} =0.5 nm and 2 nm 90

4.14 Variation on threshold voltage against the Ge fraction in strained $Si_{1-y}Ge_y$ for different channel length for strained Si/strained $Si_{1-y}Ge_y$/relaxed $Si_{0.85}Ge_{0.15}$ 92

4.15 The threshold voltage variation against oxide thickness for three difference channel length as 45 nm,120 nm and 200 nm 93

4.16 The shift of threshold voltage V_{th} against several oxide thickness with L=45 nm,120 nm and 200 nm 94

4.17 Threshold voltage variation with respect to the Ge fraction in strained $Si_{1-y}Ge_y$ with L=100 nm 95

5.1 Cross sectional view of 2D strained Si MOSFET 98

5.2 Effective oxide thickness due to energy quantization of inversion charges versus gate voltage with T_{ox}=2 nm bulk MOSFET 101

5.3	The effective gate capacitance versus gate voltage, comparing the classical and quantum capacitance	101
5.4	The energy band diagram showing the non-degenerate regime and degenerate regime	102
5.5	Fermi-Dirac integral of the general, non-degenerate approximation and degenerate approximation	104
5.6	Velocity as a function of temperature for three different carrier concentrations	105
5.7	The variation of intrinsic velocity against temperature for three different Ge content, Ge=10%, Ge=30% and Ge=50%	106
5.8	Velocity versus carrier concentration for ambient temperature 4.2K, 77K and 300K	108
5.9	The variation of the intrinsic velocity against carrier concentration in the degenerate regime for a wide range of Ge content	108
5.10	Cross section of n-type strained Si MOSFET that shows the distance *x* along the channel together with the transverse and longitudinal electric field	111
5.11	The variation of current-voltage characteristic for three different gate voltage, V_{GS} = 1.2V, V_{GS} = 1.0V and V_{GS} = 0.8	114
5.12	The quantum mechanical effects on the current-voltage characteristic of strained Si MOSFET which introduce significant decreases of the drive current	115

LIST OF ABBREVIATIONS

1D	-	One-dimensional
2D	-	Two-dimensional
3D	-	Three-dimensional
CNT	-	Carbon Nanotube
CMOS	-	Complementary Metal Oxide Semiconductor
DIBL	-	Drain Induced Barrier Lowering
DOS	-	Density of State
DRAM	-	Dynamic Random Access Memory
FD	-	Fully Depleted
FET	-	Field Effect Transistor
GNR	-	Graphene NanoRibbon
HH	-	Heavy Hole
IC	-	Integrated Circuit
I-V	-	Current-Voltage
ITRS	-	International Technology Roadmap for Semiconductors
LH	-	Light Hole
NMOS	-	n-channel MOSFET
MATLAB	-	Mathematical Laboratory
MOS	-	Metal-Oxide-Semiconductor
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect Transistor
PMOS	-	p-channel MOSFET
QME	-	Quantum Mechanical Effect
S/D	-	MOSFET Source/Drain
SCE	-	Short Channel Effect
SGOI	-	Relaxed Silicon Germanium on Insulator

SO	-	Spilt Off
SOI	-	Silicon On Insulator
TCAD	-	Technology Computer Aided Design
VLSI	-	Very Large Scale Integration

LIST OF SYMBOLS

Symbol		Description
v_{o}	-	dielectric constant of vacuum
v_{ox}	-	dielectric constant of oxide
v_{Si}	-	dielectric constant of silicon
v_{SiGe}	-	dielectric constant of silicon germanium
W_{F}	-	Fermi potential (V)
W_{s}	-	surface potential (V)
W_{smin}	-	minimum surface potential (V)
$\hbar$	-	Plank constant
l_0	-	mean free path
Γ	-	gamma function
$\sim_{eff}$	-	effective mobility
$\sim_{0}$	-	low field mobility
t	-	electron affinity in silicon
t^{SiGe}	-	electron affinity in silicon germanium
y_{F}	-	reduced Fermi energy
$\Im_i$	-	Fermi-Dirac integral of order *i*
$\}$	-	natural length
C_{ox}	-	oxide capacitance
C_G^{QM}	-	quantum gate oxide capacitance
$\mathrm{E_g}$	-	silicon bandgap
$\mathrm{E_{g,SiGe}}$	-	silicon germanium bandgap
E_y	-	electric field
E_L	-	longitudinal electric field
v_{c}	-	critical electric field

$f(E)$	-	Fermi-Dirac distribution
Ge	-	germanium
I_D	-	drain current (A)
I_{Dsat}	-	saturation drain current (A)
I_{on}	-	off current (A)
I_{off}	-	on current (A)
k_B	-	Boltzmann constant
L	-	channel length (nm)
m_0	-	electron mass
m^*	-	effective mass
n_i	-	intrinsic carrier density of silicon
N_A	-	channel doping density (cm^{-3})
N_D	-	source/drain doping density (cm^{-3})
N_{cd}	-	effective density of state in conduction band
q	-	charge (C)
r_j	-	junction depth (nm)
S	-	subthreshold slope (mV/dec)
Si	-	silicon
$SiGe$	-	Silicon Germanium
SiO_2	-	silicon dioxide
T	-	temperature (K)
T_{ox}	-	oxide thickness (nm)
T_{Si}	-	silicon thickness (nm)
T_{SiGe}	-	silicon germanium thickness (nm)
T_{buff}	-	buffer thickness (nm)
V_{bi}	-	silicon build-in voltage (V)
$V_{bi,SiGe}$	-	silicon germanium build-in voltage (V)
V_c	-	critical voltage (V)
V_D	-	drain voltage (V)
V_{DS}	-	drain-to-source voltage
V_{Dsat}	-	saturation voltage
V_{fb}	-	flatband voltage (V)
V_{fb}^{QM}	-	quantum flatband voltage (V)

V_G	-	gate voltage (V)
V_{GS}	-	gate-to-source voltage (V)
V_{th}	-	threshold voltage (V)
V_{th}^{QM}	-	quantum threshold voltage (V)
V_{sub}	-	substrate voltage (V)
v_d	-	drift velocity
v_i	-	intrinsic velocity
v_{sat}		saturation velocity
v_{th}	-	thermal velocity
W	-	channel width (µm)
z_{QM}	-	quantum correction

LIST OF APPENDICES

APPENDIX	TITLE	PAGE
A	List of Publications	136
B	Derivation of Threshold Voltage For Strained Silicon	139
C	Derivation of Threshold Voltage For Dual Channel Heterostructure	145
D	Model Parameters in Silvaco's ATLAS	155
E	Effective Charge Under The Gate	157
F	Two Dimensional Modeling	159
G	Derivation of Current-Voltage	162

CHAPTER 1

INTRODUCTION

This chapter begins with little description of the background of the field-effect transistors from it first invention to the latest development in today's semiconductor industries. Next, the arising problems regarding to the research topic are addressed in the problem statement section, following with the research objectives and scopes. The overall organization of this thesis is presented in the last section of this chapter.

1.1 Background

The invention of the first field-effect transistor (FET) can be traced back in 1925, when the first patent filed by Austrian-Hungarian physicist Lilienfeld (Arns, 1998). However, Lilienfeld did not publish any research articles on his research nor his patents cited any specific examples of a working prototype. The practical Metal-Oxide-Semiconductor (MOS) was only developed much later in 1947 when the Bell Telephone Laboratories performed the fundamental works on FETs. Following in the year 1959, Moll fabricated the first MOS capacitor (Sah, 2005). This was followed

by the first Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) build by Kahng and Atalla (Arns, 1998). Nowadays, numerous advances have been done to the MOS transistors and it is now, the most abundant man-made object in the world. World's largest microelectronics manufacturer, Intel currently announces a historic innovation for the world's first 3-D transistors in mass production with 22 nm feature size (Intel, 2012).

The rapid advancement and growth in the semiconductor industry is fuelled by the increasing need for faster, smaller and cheaper microprocessors and microelectronic devices. For over the past few decades, the miniaturization in silicon (Si) integrated circuits (IC's) has been well characterized and envisioned by Moore's Law, which predicted that the number of transistors on chip doubled every 18 to 24 months, compared to its predecessor (Thompson and Parthesarathy, 2006; Mack, 2011). Many improved lithography and semiconductor fabrication equipments are designed to be on track with the curve and one ahead of the technology. So far, Moore's Law has been a valuable way of describing the progress of ICs and number of transistors fitted into each generation of processors.

For many years now, the size shrinking of MOSFET has been predominantly directed by the scaling of it physical properties (Ernst et al, 2000; Frank et al, 2001). Researches on the scaling limitations were initially concerned with the predicted minimum feature size of MOSFET. The ultimate physical limit of the scaling is believed to be the atom atomic distance in the silicon crystal which is around 0.3 nm, which in turn, limit the channel length to be 25 nm for planar Si MOSFET (Iwai et al, 2006). The scaling strategy is getting complicated as the effective channel length approaches sub 100 nm and supply voltage reaches 1V (Zeitzoff, 2006). These challenges include several physical limitations on gate oxide thickness, doping concentration, depletion and junction depth as well as the presence of short channel effects (SCEs).

Physical and performance limitations are encountered along with the continuous shrinking the size of the transistors into nanometer regime, where the scalability of the conventional Si MOSFET devices seem to be constrained. Novel materials and novel architectures are to be investigated to continue to increase the speed and scalability of MOSFET devices, leading to the future electronic systems in new paradigm. In conjunction, International Roadmap of Semiconductor (ITRS) pointed that one of the primary challenge that the industry has identified is how to decrease the size of semiconductor while increasing performance standard to meet consumer demands (ITRS, 2011), with the hope of maintaining the Moore's exponential growth. The extended CMOS platform via heterogeneous integration of new technologies that are being explored include: new device designs namely dual gate, FinFet, silicon-on-insulator (SOI) and new materials such as strained silicon, carbon nanotube, graphene and nanowire.

Current nanometer-scaled MOSFETs are true short channel devices, where the device dimensions are scaled down into nanometer regime and several serious doubts are being raised regarding the ability to shrink the gate length of conventional bulk MOSFET below 30 nm. In addition, classical physics are insufficient to fully understand the behavior of MOSFET at small dimension. Significant deviations from the classical calculation are observed, which must be explained by the quantum theory in order to model the next generation of more precise short channel MOSFETs.

1.2 Problem Statement

The sustained scaling of conventional bulk devices into sub-nanometer regime shows a tremendous growth by the introduction of novel devices with enhanced performance. The re-evaluation of the device physics in nanoscale regime

through simulation and modeling are necessary to generate a new paradigm of understanding the physical characterizations and give a truthful interpretation on the device operations. Simulation tools dramatically reduce the development costs and time that allow the users to examine various scenarios of physical aspects (Silvaco, 2012). This is important as it allows for performance enhancement without the need for monetary investment to obtain new specialized equipments. Accordingly, the modeling provides a new insight into the operation of modern semiconductor devices and explores new phenomena of the device physics.

Leading from many technological and fundamental physical challenges posed in scaling the conventional MOSFET, strained silicon/silicon germanium (strained Si/SiGe) arises as one innovation to continue the performance enhancements without significant changes to the current Si processing steps. Strained Si was reported to increase the electron and hole mobility by 110% and 45%, respectively. However, as the device dimension is shrinking into nanometer regime, the classical models are found to be insufficient (Jayadeva amd DasGupta, 2009) that resulted in erroneous on critical device structures and inadequate predictions of the electrical behavior parameters. Consequently, fundamental physical and practical consideration of such a small device is vitally needed to be re-visited.

One of the concerns is the influence of quantum effects on the threshold voltage and current-voltage variations. These electrical characteristics that incorporate the quantum mechanical effects significantly deviate from the classical models. At extremely small dimension where the oxide thickness is typically thin and the channel is highly doped, the presence of high electric field in the channel causes energy quantization and charge carrier re-distribution (Ma et al, 2000). Moreover, the Maxwellian distribution which is generally applied for lowly doped semiconductor is no longer sufficient to describe the current-voltage characteristic for these devices. Hence, the electrical behaviors of degenerately doped short channel MOSFET are necessary to re-considered associated with the quantum theory.

1.3 Research Objectives

The aim of this research is to investigate the impact of quantum mechanics on the threshold voltage of both strained Si MOSFET and dual channel heterostructure using two-dimensional Poisson equation and to model the current-voltage characteristic of two-dimensional strained Si MOSFET. The followings are the objectives of this research:

1. To design and simulate strained Si MOSFET and dual channel heterostructure with enhanced performance for channel length down to 30 nm.

2. To investigate and model the quantum mechanical effects on the threshold voltage of nanoscale strained Si MOSFET and dual channel heterostructure.

3 To formulate analytical current-voltage characteristic with the incorporation of quantum theory of two-dimensional short channel strained Si MOSFET.

1.4 Research Scopes

In this research, the quantum mechanical effects on the electrical performance of strained Si MOSFET and dual channel heterostructure are investigated. The research scopes of this work are divided into five main categories as follow:

a) *TCAD Simulation*

Simulation of strained Si MOSFET and dual channel heterostructure are conducted using Silvaco's TCAD software. Both fabrication processes and characterization are reported using TCAD tools: ANTHENA and ATLAS for sub-100 nm scalable channel length.

b) *Analytical Modeling of Threshold Voltage*

The quantum-mechanical threshold voltage models of both strained Si and dual channel heterostructure are developed using MATHEMATICA and MATLAB software. A theory of quantum of nanoscale transistors is adopted and reported.

c) *Analytical Modeling of Current-Voltage Characteristic*

The analytical modeling of current-voltage characteristic of two-dimensional strained Si MOSFET that comprises of quantum capacitance, carrier statistic, intrinsic velocity and carrier mobility is carried out for both non-degenerate and degenerate doped devices using MATHEMATICA and MATLAB software.

d) *Results Analysis*

The characteristics and performances of the models are studied particularly in understanding the underlying physics and mechanisms.

d) *Validation*

Comparisons between the analytical results and TCAD simulation results as well as the experimental data or others published models are performed in order to evaluate the validity of the developed models and adopted theories

1.5 Thesis Organization

This thesis work has been divided into six chapters. Chapter 1 introduces the background of this research by providing the problem statements, research objectives, research scopes and thesis organization.

Following this chapter, a thorough historical review of different MOSFET development is presented in chapter 2. It briefly discusses the fundamentals of strained Si technology, the physics behind the mobility improvement of strained Si devices and the advantages of dual channel heterostructure. A detail description on the quantum mechanical effects is also presented. Reviews of the previous threshold voltage models are also provided. The model characteristics and related researches are summarized at the end of this chapter.

Chapter 3 deals with the workflow for this research. It also introduces the modeling and simulation approaches used in accomplishing the respective research objectives. The research methodology flowchart that summarizes the overall research sequences is also presented in this chapter.

In chapter 4, the analytical threshold voltage that takes into account the quantum mechanical effects for strained Si MOSFET and dual channel heterostructure are presented. Intensive analysis is carried out on the analytical results and the findings are discussed. The comparison between analytical models and simulation results using TCAD tool are presented in the chapter with detailed physical explanation.

Chapter 5 describes the current-voltage (*I-V)* characteristic of two-dimensional strained Si MOSFET in the degenerate regime. A small portion of this

chapter discusses the definition of non-degenerately and degenerately doped semiconductor. The *I-V* characteristic has been validated using the available experimental data and the degradation of drain current attributed to the quantum mechanical effects is discussed and explained.

Finally, chapter 6 summarizes and concludes the findings of this research together with the main contributions and recommendations of possible areas for future research and development.

REFERENCES

Åberg I, Chléirigh C. N and Hoyt J. L. (2006). Ultra Thin Body Strained Si and SiGe Heterostructure on Insulator MOSFETs. *IEEE Trans. on Electron Devices*, vol. 53, no. 5, pp.1021-1029.

Åberg I, Chléirigh C. N, Olubuyide O. O and Hoyt J. L. (2004). High Electron and Hole Mobility Enhancement in Thin-Body Strained Si/Strained SiGe/Strained Si Heterostructure on Insulator. *IEDM Technical Digest. IEEE International*, pp. 173-176.

Acosta T and Sood S. (2006). Engineering Strained Silicon-Looking Back and Into the Future. *IEEE Potentials*, vol. 25, issue. 4, pp. 31-34.

Agnello P. D. (2002). Process Requirements for Continued Scaling of CMOS-The Need and Prospects for Atomic-Level Manipulation. *IBM J. Res. & Dev*., vol. 46, pp. 317-338.

Ahmadi M. T, Lau H. H, Ismail R, and Arora V.K. (2009). Current-Voltage Characteristics of a Silicon Nanowire Transistors. *Microelectronics Journal*, vol. 40, pp. 547-549.

Ahmed S. S. and Vasileska D. (2003). Threshold Voltage Shift in Narrow SOI Due to Quantum Mechanical Size-Quantization Effects. *Physica E*, vol. 19, pp. 48-52.

Akers L. A. and Sanchez J. J. (1982). Threshold Voltage Models of Short, Narrow and Small Geometry MOSFETs: A Review. *Solid State Electronics*, vol. 25, no. 7, pp. 621-641.

Appenzeller J. (2008). Carbon Nanotubes for High-Performance Electronic Progress and Prospect. *Proceeding of the IEEE*, vol. 96, pp. 201-211.

Arns R. G. (1998). The Other Transistor: Early History of the Metal-Oxide-Semiconductor-Field-Effect-Transistor. *Engineering Science and Education Journal*, pp. 233-240.

Arora N. (2007). *MOSFET Modeling For VLSI Simulation: Theory and Practic*e. Singapore: World Scientific Publishing.

Arora V. K. (2008). Ballistic Quantum Transport in Nono Devices and Circuits, *IEEE International Nanoelectronics Conference* , pp.573-578.

Arora V. K and Das M. B.(1990). Effect of Electric-Field-Induced Mobility Degradation on the Velocity Distribution in a sub-μm Channel Length of InGaAs/AlGaAs Heterojunction MODFET. *Semicond. Sci. Techno*l. vol, 5, pp. 967.

Badcock S. G, O'Neill A. G, and Chester E.G. (2002). Device and Circuit Performance of SiGe/Si MOSFETs. *Solid State Electron*, vol. 46, pp.1925-1932.

Bangsaruntip S, Cohen G. M, Majumdar A. and Sleight, J.W. (2010). Universality of Short Channel Effects in Undoped-Body Silicon Nanowire MOSFETs. *IEEE Electron Device Letters*, vol. 31, no. 9 pp. 903-905.

Bensidhoum T, Lime F. and Ghibaudo G. (2008). Mobility Extraction in Unixially and Biaxially Strained N-MOSFETs. *African Physical Review 2 Special Issue (Microelectronics)*: 0007, pp. 15-17.

Bindu B, DasGupta N. and DasGupta A. (2006). Analytical Model of Drain Current of Strained Si/Strained $Si_{1-y}Ge_y$/Relaxed $Si_{1-x}Ge_x$ NMOSFETs and PMOSFETs for Circuit Simulation. *Solid State electronics*, vol. 50, pp. 448-455.

Blakemore J. S. (1982). Approximation for Fermi-Dirac Integrals Especially the Function $\Im_{1/2}(y_F)$ used to Describe Electron Density in a Semiconductor. *Solid State Electronics,* vol.25, pp.1067.

Briggs P. J., Walker A. B. and Herbert D. C. (1998). Modelling the Influence of High Current on the Cutoff Frequency in Si/SiGe/Si Heterojunction Transistors. *Semicond. Sci. Technol*. vol. 13, pp. 468-479.

Bringuier, E. (2002). On High-Field Departures From Ohm's Local Law. *Europe Journal of Physics*, vol. 23, pp. 367-370.

Celler G. K and Cristoloveanu S. (2003). Frontiers of Silicon-on-Insulator. *Journal of Applied Physics*, vol. 93, pp. 4955.

Chandrasekaram K, Zhou X, and Chiah S. B. (2004). Physic-Based Scalable Threshold Voltage Model for Strained-Silicon MOSFETs. *Proc. NSTI Nanatech*, vol. 2, pp.179-182.

Cham K. M, Oh S. Y, Chin D, Moll J. L and Lee K. et al (1988). *Computer-Aided Design and VLSI Device Development*, 2nd Ed, Boston: Kluwer Academic Publisher.

Chattopadhyay S, Driscoll L. D, Kwa K.S.K, Olsen S. H, and O'Neill A. G (2004). Strained Si MOSFETs on Relaxed SiGe Platforms: Performance and Challenges. *Solid State Electron*, vol. 48, pp. 1407-1416.

Chaudhry A. and Kumar M. J. (2004). Controlling Short-Channel-Effects in Deep Submicron SOI MOSFETs for Improved Reliability: A Review. *IEEE Trans. on Device and Materials Reliability*, vol. 4, no. 1, pp. 99-109.

Chaudhry A. and Kumar M. J. (2004). Investigation of the Novel Attributes of a Fully Depleted Dual Material Gate SOI MOSFE*Ts*. *IEEE Trans. on Electron Devices,* vol. 51, no. 9, pp.1463-1467.

Chaudhry A, Roy J. N. and Joshi G. (2010). Nanoscale Strained Si MOSFETs Physics and Modeling Approaches: A Review. *Journal of Semiconductor*, vol. 31, no. 10.

Chaudhry A, Sangwan S. and Roy J. N. (2011). Analytical Threshold Voltage for a Biaxial Strained-Si MOSFET. *Contemporary Engineering Sciences*, vol. 4, no. 6, pp. 249-258.

Chek D. C. Y. Ahmadi M. T, Tan M .L. P, Ismail R and Arora V. K (2008). Band Structure Effects on the Carbon Nanotube Carrier Statistics. *MASS Regional Conference on Solid State Science and Technology*, Port Dickson.

Chidambaram P. R, Bowen C, Chakravarthi S, Machala C and Wise R. (2006). Fundamentals of Silicon Material Properties for Successful Exploitation of Strain Engineering in Modern CMOS Manufacturing. *IEEE Trans. on Electrons Devices,* vol. 53, no. 5, pp. 944-964.

Clere R, Spinelli A, Ghibaudo G and Pananakakis G. (2002). Theory of Direct Tunneling Current in Metal Oxide Semiconductor Structures. *Journal of Applied Physics,* vol. 91, no. 2, pp. 1400-1409.

Cressler J. D. (2008). *SiGe and Si Strained Layer Epitaxy for Silicon Heterostructure Devices*, United States of America: CRC Press.

Cui Y, Zhong Z, Wang D, Wang W. U, and Lieber C. M. (2003). High Performance Silicon Nanowire Field Effect Transistors, *Nano Letters*, vol. 3, no.2, pp. 149–152.

D'Agostino F. and Quercia D. (2000). *Short Channel Effects in MOSFETs*. Research Project.

Datta S, Brask J, Dewey G, Doezy M and Doyle B. et al (2004). Advanced Si and SiGe Strained NMOS and PMOS Transistors with High-K/Metal-Gate Stack, *IEEE BCTM*, pp.194-197.

Dhar S, Karlowats G, Ungersboeck E. and Kosina H. (2005). Numerical and Analytical Modeling of the High Field Electron Mobility in Strained Silicon, *Proc SISPADM*, pp. 223-226.

Driussi F, Esseni D, Selmi L, Hellström P.E and Malm G. et al (2008). On the Electron Mobility Enhancement in Biaxially Strained Si MOSFETs. *Solid-State Electronics* , vol. 52, pp. 498-505.

Dollfus P, Musalem F. X, Galdin S, and Hesto P. (1996). Operation of SiGe Channel Heterojunction p-MOSFETs. *Applied Surface Science*, vol. 102, pp. 259-262.

Engstrom O and Landsberg P. T. (2005). Charge Carrier Statistics at InAs/GaAs Quantum Dots. *Physical review B,* vol. 72, pp. 075360.

Ernst T, Tinella C, Raynaud C, and CristoloveanuS. (2000). Fringing Fields in sub-0.1 µm FD SOI MOSFETs: Optimization of the Device Architecture, *Proc.ULIS 2000 Workshop* , pp. 47–50.

Fairis A. T. M and Arora V.K. (2000). Quantum Engineering of Nanoelectronic Devices: The Role of Quantum Confinement on Mobility Degradation, *Microelectronics Journal*, vol. 32, pp. 679-689.

Frank D. J, Laux S. E, and Fischetti M. V. (1992). Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go. *IEEE International Electron Devices Meeting*, pp. 553-556.

Frank D. J, Dennard R. H, Norwak E, Solomon P. M, Taur Y. and Wong H. S. P. (2001). Device Scaling Limits of Si MOSFETs and Their Application Dependencies, *Proc. IEEE*, vol. 89, no. 3, pp. 259–288.

Gannavaram S, Pesovic N and Öztürk M. C. (2000). Low Temperature ($800 \circ C$) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70 nm CMOS. *IEDM Tech. Dig*. pp. 437-440.

Gargini P. (2000). The International Technological Roadmap Semiconductor (ITRS): Past, Present and Future, *GaAs IC Symposium, 22nd Annual.*

Geim A. K and Novoselov K. S. (2007). The Rise of Graphene. *Nature Materials,* vol. 6 pp. 183-191.

Ghani T, Armstrong M, Auth C, Giles M. D, and Mistry K. et al (2004). Uniaxial Strained Silicon CMOS Devices for High Performance Logic Nanotechnology. *Electrochemical Society Fall Meeting*, Honolulu, Hawaii.

Ghyselen B. (2005). Strain Engineering in SOI-Type Materials for Future Technologies. *Materials Science and Engineering B*, vol. 124-25, pg16-23.

Godoy A, Lopez-Villanueva J. A, Jimenez-Tejada J. A, Palma A, and Gamiz F. (2001). A Simple Subthreshold Swing Model for Short Channel MOSFETs. *Solid State Electronics,* vol 45, pp. 391-397.

Goyal P, Moon J. E, and Kurinex S. K (2007). Design and Simulation of Strained Si /SiGe Dual Channel MOSFETs. *Semiconductor Device Research Symposium*, pp. 1-2.

Hamid H. A. E, Guitart J. R, and I íguez B. (2007). Two-Dimensional Analytical Threshold Voltage and Subthreshold Swing Models of Undoped Symmetric Double-Gate MOSFETs. *IEEE Trans. On Electron Devices*, vol. 54, no. 6, pp. 1402-1408.

Hareland S. A, Jallepalli S, Chindalore G, Shih W. K. and Tasch A. F. et al. (1997). A Simple Model for Quantum Mechanical Effects in Hole Inversion Layers in Silicon PMOS Devices, *IEEE Trans. on Electron Devices*, vol. 44, no. 7, pp. 1172-1173.

Hashemi P and Hoyt J. L. (2012). High Hole Mobility Strained-Ge/SiGe P-MOSFETs With High-K/Metal Gate: Role of Strained Si Cap Thickness. *IEEE Electron Device Letters,* vol. 33, no. 2, pp. 173-175.

He J, Chan M, Zhang X and Wang Y. (2006). An Analytical Model to Account for Quantum Mechanical Effects on MOSFETs Using a Parabolic Potential Well Approximation, *IEEE Trans. on Electron Devices*, vol. 53, no. 9, pp. 2082-2090.

Hoyt J. L, Nayfeh. M, Eguchi S, Aberg I and Xia G. et al (2002). Strained Silicon MOSFET Technology. *IEDM Tech. Dig*. , pp. 23–26.

Huang X , Lee W. C, Kuo C, Hisamota D, Chang L and Kedzierski J. et al (2001). Sub 50 nm P-Channel FinFet. *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp.880-886.

Huang L, Chu J. O, Goma S. A, D'Emic C. P and Koester S. J. et al (2002). Electron and Hole Mobility Enhancement in Strained SOI by Wafer Bonding. *IEEE Trans. on Electron Devices*, vol. 49, no. 9, pp.1566-1572.

Illinois (2006). *A Magazine for Young People*, www.illinois-history.gov/IH306. pdf

Iniewski K, Voinigescu S, Atcha J and Salama C. A.T. (1993). Analytical Modeling of Threshold Voltage in P-Channel Si/SiGe/Si MOS Structure. *Solid State Electron*, vol. 36, no.2, pp. 179-182.

Intel (2012). *Intel 22 nm Technology*, http://www.intel.com

ITRS (2011). *The International Technology Roadmap for Semiconductor.* http://www.itrs.net/report.html

Iwai H, Kakushima K. and Wong H. (2006). Challenges for Future Semiconductor Manufacturing. *International Journal of High Speed Electronics and Systems*, vol. 16, pp. 43-82.

Jayadeva G.S. and DasGupta A. (2009). Compact Model of Short-Channel MOSFETs Considering Quantum Mechanical Effects, *Solid-State-Electronics,*vol.53,pp.649-657.

Jayanarayanan S, Prins F, Chen X. D, and Banerjee S. (2002). Enhanced Mobility in 100 nm Strained SiGe Vertical p-MOSFETs Fabricated by UHVCVD. *Mat. Res. Soc. Symp. Proc*. vol. 686.

Jiang X. W, Deng H. X, Li S. S, Luo J. W. and Wang L. W. (2009). Quantum Mechanical Simulation of Nanosized Metal-Oxide-Semiconductor-Field-Effect Transistor Using Empirical Pseudopotentials: A Comparison for Charge Density Occupation Methods, *Journal of Applied Physics*, vol. 106, pp. 084510.

Jung J, Lee M. L, Yu S. Fitzgerald E. A and Antoniadis D. A. (2003). Implementation of Both High Hole and Electron Mobility in Strained Si/Strained $Si_{1-y}Ge_y$ on Relaxed $Si_{1-x}Ge_x$ ($x<y$) Virtual Substrate. *IEEE Electron Device Letters,* vol. 24, no. 7, pp. 460-462\

Kang E. S, Yau W. H, Anwar S. and Ismail R.. (2012) Two-Dimensional Analytical Threshold Voltage Model of Nanoscale Strained Si/Si_{1-x} Ge_x MOSFETs including Quantum Mechanical Effects. *Journal of Computational and Theoretical Nanoscience*, vol. 9. no. 3, pp. 441-447.

Kang E. S, Anwar S. and Ismail R. (2012). Quantum Mechanical Effect on the Threshold Voltage of Nanoscale Dual Channel Strained Si/Strained Si_{1-}

$_{y}Ge_{y}$/relaxed $Si_{1-x}Ge_{x}$ PMOSFETs. *Journal of Computational and Theoretical Nanoscience,* (accepted).

Kang H, Han J. W. and Choi Y. K. (2008). Analytical Threshold Voltage Model for Double Gate MOSFETs with Localized Charges. *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 927-930.

Karamdel K, Ahmadi M. T, Damghanian M, Majlis B. Y and Dee C. F et al (2009). Analysis and Simulation of Carrier Statistic for Semiconducting Single Wall Carbon Nanotube. *Materials Reseach Innovations*, vol. 13, no. 21, pp. 211-213.

Karim M. A. and Haque A. (2010). A Physically Based Accurate Model for Quantum Mechanical Correction to the Surface Potential of Nanoscale MOSFETs, *IEEE Trans. on Electron Devices*, vol. 57, no. 2, pp. 496-502.

Kaur R, Chaujar R, Saxena M. and Gupta R. S. (2007). Unified Subthreshold Model for Channel-Engineered Sub 100 nm Advanced MOSFET Structures. *IEEE Trans. on Electron Devices,* vol. 54, no. 9, pp. 2475-2486.

Kim J. S and Won T. Y. (2006). Two-Dimensional Quantum Mechanical Modeling For Multiple Channel FET. *Solid State Electronics,* vol. 50, pp. 1150-1155

Kloes A and Weidemann M. (2007). Self-Consistent 2D Modeling of Nanoscale Bulk MOSFET. Solid-State Electronics, vol. 51, pp. 739-748

Krishnamohan T, Jungemann C, Kim D, Selberherr S and Meinerzhagen B. et al (2007). High Performance Uniaxially-Strained, Silicon and Germanium, Double-Gate P-MOSFETs. *Microelectronic Engineering* , vol. 84, pp. 2063-2066.

Kumar M. J, Venkataram V. and Nawal . (2007). Impact of Strain or Ge Content on the Threshold Voltage of Nanoscale Strained Si/SiGe Bulk MOSFETs. *IEEE Trans. on Device and Materials Reliability*, vol. 27, no. 1, pp.181-187.

Kumar S. P, Agralwal A, Chaujar R, Gupta R. S and Gupta M. (2011). Device Linearity and Intermodulation Distortion Comparison of Dual Material Gate and Conventional AlGaN/GaN High Electron Mobility Transistor. *Microelectronic Reliability*, vol. 51, no. 3, pp. 587-596.

Lang D.V, People R, Bean J. C, and Sergent A. M. (1985). Measurement of the Bandgap of $Si_{1-x}Ge_{x}$/Si Strained Layer Heterostructures. *Apply. Phys. Lett.* vol 47, no.12, pp.1333-1335.

Lee M. L and Fitzgerald E. A (2003). Optimized Strained Si/ Strained Ge Dual Channel Heterostructures for High Mobility P- and N-MOSFETs. *IEEE International Electron Device Meeting (IEDM*), pp. 429-432.

Lee M. L and Fitzgerald E. A (2005). Strained Si, SiGe, and Ge Channels for High Mobility Metal Oxide Semiconductor Field Effect Transistors. *Journal of Applied Physics,vol.* 97, pp.011101.

Leitz C. W, Currie M. T, Lee M. L, Cheng Z. Y and Antoniadis D. A. et al (2001). Hole Mobility Enhancemnet in Strained $Si/Si_{1-y}Ge_y$ p-type Metal-Oxide-Semiconductor Field Effect Transistors Grown on Relaxed $Si_{1-x}Ge_x$ ($x<y$) virtual Substrates, *Appl. Phys. Lett*. vol. **79,** pp. 4246-4248.

Li C, Luo G. L, Liu Z. N, Chen P. Y and Tsien P. H. (2002). Novel Strained Si/Relaxed SiGe Channel PMOSFETs. *Thin Solid Films* vol., 409, pp. 112-115.

Li J, Liu H, Li B, Cao L and Yuan B. (2010). Two-Dimensional Threshold Voltage Model for DMG Strained-Si-On-Insulator MOSFETs. Journal of Semiconductor, vol. 31, no. 8, 084008.

Lin P. S and Wu C. Y. (1987). A New Approach to Analytically Solving the Two-Dimensional Poisson's Equation and Its Application in Short Channel MOSFET Modeling. IEEE Transaction on Electron Devices, vol. ED 34, no. 9, pp. 1947-1956

Lim J S, Thompson S. E. and Fossum J. G. (2004). Comparison of Threshold Voltage Shifts for Uniaxial and Biaxial Tensile-Stresses N-MOSFETs. *IEEE Electron Device Letters, vol*. 25, no. 11, pp713-733.

Lime F, Andrieu F, Derix J, Ghibaudo G, Boeuf F, Skotnicki T. (2006). Low Tempereture Characterization of Effective Mobility in Uniaxially and Biaxially Strained NMOSFETs. *Solid State Electronics,*vol. 50*,* pp. 644-649.

Liu X. Y, Kang J. F and Han R. Q. (2003). Direct Tunneling Current Model for MOS Devices with Ultra-Thin Gate Oxide Including Quantization Effect and Polysilicon Depletion Effect. *Solid State Communications*, vol. 125, no. 3-4, pp. 219-223.

Lochtefeld A, Djomehri I. J., Samudra G. and Antoniadis D. A. (2002). New Insights into Carrier Transport in n-MOSFETs. *IBM J. Res. & Dev*., vol. 46, pp. 347-358.

Lu W. Y and Taur Y. (2006). On the Scaling Limit of Ultra thin SOI MOSFETs. *IEEE Trans. on Electron Devices*, vol. 53, no. 5, pp. 1137-1141.

Lundstrom M and Guo J. (2006). *Nanoscale Transistor: Device Physics, Modeling and Simulation*, New York : Springer

Luo Z, Steegen A, Eller M, Mann M and Baiocco C et al (2004). High Performance and Low Power Transistors Integrated in 65 nm Bulk CMOS Technology. I*ED Tech. Dig*., pp. 661-664.

Ma Y. T, Li Z. J, Liu L. T, Tian L. L and Yu Z. P. (2000).Effective Density of State Approache to QM Corrections in MOS Structure, *Solid State Electronics*, vol. 44, pp. 401-407.

Mack C. A. (2011). Fifty Years of Moore's Law. *IEEE Transaction on Semiconductor Manufacturing*, vol. 24, pp. 202-207.

Mahato S. S, Maiti T. K, Arora R, Saha A. R, Sarker S. K and Maiti C. K (2006). Strained Engineering for Future CMOS Technologies. 3rd *International Conference on Computers and Devices for Communication (COED-06)*, Calcuta.

Maiti C. K, Chattopadhyay S and Bera L. K. (2007). S*trained Si Heterostructure Field Effect Devices*, United States of America: Taylor & Francis Group.

MathWorks (2012). *Accelerating the Pace of Engineering and Science* http://www.mathworks.com/products/matlab/

Moers J. (2007). Turning The World Vertical: MOSFET with Current Flow Perpendicular to the Wafer Surface. *Applied Physics A: Materials Science & Processing,* vol. 87, pp. 531-537.

Montoro C. G and Schneider M. C. (2007). *MOSFET Modeling for Circuit Analysis and Design*, Singapore: World Scientific Publishing.

Mousavi S. M, Ahmadi M. T, Sadeghi H, Nilghaz A and Amin A. et al (2011). Bilayer Graphene Nanoribbon Carrier Statistic in Degenerate and Non Degenerate Limit. *Journal of Computational and Theoretical Nanoscience*, vol. 8, no.10, pp. 2029-2032.

Mukhopadhyay B, Biswas A, Basu P. K, Eneman G, Verheyen P. et al (2008). Modeling of Threshold Voltage and Subthreshold Slope of Strained Si MOSFETs Including Quantum Effects. *Semiconductor Science and Technology*, vol. 23, 095017

Natori K. (2008). Ballistic/Quasi Ballistic Transport in Nanoscale Transistor. *Applied Surface Scienc*e, vol. 254, pp.6194-6198.

Nayfeh H. M, Leitz C. W, Pitera A. J, Fitzgerald E. A and Hoyt J. L et al (2003). Influence of High Channel Doping on the Inversion Layer Electron Mobility in Strained Silicon n-MOSFETs. *IEEE Trans. Device Letters*, vol. 24, no.4, pp. 248-250.

Nayfeh H. M., Hoyt J. L and Antoniadis D. A. (2004). A Physically Based Analytical Model for the Threshold Voltage of Strained Si NMOSFETs. *IEEE Trans. on Electron Devices*, vol. 51, no. 12, pp. 2069-2072.

Numata T, Mizuno T, Tezuka T, Koga J and Takagi S. (2005). Control of Threshold Voltage and Short Channel Effects in Ultra-Thin Strained SOI CMOS, *IEEE Trans. Of Electron Devices*, vol. 52, no. 5, pp. 1780-1786.

Oda S and Ferry D. (2006). *Silicon Nanoelectronics*. Boca Raton, RL: CRC Press.

Ohkura Y (1990). Quantum Effects in Si nMOS Inversion Layer at High Substrate Concentration. *Solid-State Electronics*, vol. 33, pp. 1581-1585.

Olsen S. H, Kwa K. S. K , Driscoll L, S,Chattopadhyay and O'Neill A. G. (2004). Design, Fabrication and Characterisation of Strained Si/SiGe MOS Transistors. *IEEE Proc. Circuits Devices Syst*. vol. 151, no. 5, pp. 431-437.

Olsen S. H, O'Neill A. G, Chattopadhyay S, Driscoll L. S and Kwa K. S. K. et al (2004). Study of Single and Dual Channel Designs for High Performance Strained-Si-SiGe n-MOSFETs. *IEEE Trans. on Electron Devices*, vol. 51, no. 7, pp.1245-1253.

O'Neill A. G, Olsen S. H, Escobedo-Cousin E, Varzgar J. B. and Agaiby R. et al (2006). Strained Silicon Technology. *International Conference on Solid-State and Integrated Circuit Technology Proceeding*, pp. 104-107.

Paul D. J. (2004). Si/SiGe Heterostructure: From Material and Physics to Devices and Circuits. *Semicond. Sci. Technol*. vol.19, pp. R 75-R108.

Pennington G and Goldsman N. (2005). Low Field Semiclassical Carrier Transport in Semiconducting Carbon Nanotubes. Physical Review B, vol. 71, no. 20.

People R. and Bean J. C. (1986). Band Alignment of Coherently Strained $Si_{1-x}Ge_x$ /Si Heterostructures on <001> $Si_{1-y}Ge_y$ Substrates. *Appl. Phys. Lett*. vol. 48, no.8, pp. 530-540.

Pierret R. F. (1987). *Advanced Semiconductor Fundamentals*, Massachusetts: Addison-Wesley.

Pirovano A, Lacaita A. L. and Spinelli A. S. (2002). Two-dimensional Quantum Effects in Nanoscale MOSFETs, *IEEE Trans. on Electron Devices*, vol. 49, no. 1, pp. 25-31.

Prégaldiny F, Lallement C and Mathiot D. (2003). Accounting for Quantum Mechanical Effects From Accumulation to Inversion, in a Fully Analytical Surface-Potential –Based MOSFET Model, *Solid-State Electronics*, vol. 48, pp. 781-787.

Rabaey J. M, Chandrakasan A. and Nikolic B. (2003). *Digital Integrated Circuits: A Design Perspective*. 2nd edition, New Jersey: Prentice Hall.

Ramesh R, Madheswaran M and Kannan K. (2008). Three-Dimensional Quantum Effects in NanoMOSFETs. *Int. Conference on Recent Advances in Microwave Theory and Application*, pp. 761-763.

Rechem D. and Latreche S, (2008). The Effects of Short Channel on Nanoscale SOI MOSFET. *African Physical Review 2 Special Issue (Microelectronics):*0038, pp.80-81.

Rim K, Chu J, Chen H, Jenkins K. A, Kanarsky T. et al (2002). Characteristics and Device Design of Sub-100 nm Strained Si N- and P-MOSFETs. *Symposium on VLSI Technology Digest of Technical Paper*s, pp. 98-99.

Riyadi M. A, Ahmadi M. T and Saad I. (2009). Analytical Study of Carrier Statistics in 2-Dimensional NanoscalE PMOS. *AIP Conference Proceedings*, vol. 1136, pp. 89-92.

Saad I, Tan L. P. and Hii I. H. (2009). Ballistic Mobility and Saturation Velocity in Low Dimensional Nanostructures. *Microelectronics Journal*, vol. 40, pp. 540-542.

Saad I, Riyadi M. A, Taghi M, Atfyiz. F. M. N. andV. K. Arora (2010). Analytical Analysis of Ballistic Drift Velocity in Low-Dimensional Nano-Devices. *Proc. Asia Modelling Symposium,* pp. 601-605.

Sah C. T. (2005). A History of MOS Transistor Compact Modeling. *NSTI, Nanotech*, pp 347-190.

Sanuki T , Oishi A, Morimasa Y, Aoya S and Khinoshita T. et al (2003). Scalability of Strained Silicon CMOSFET and High Drive Current Enhancement in the 40 nm Gate Length Technology. *IEDM Tech, Dig.* , pp.65-68.

Seetharamappa J, Yellappa S, and D'SouzaF. (2006). Carbon Nanotube: Next Generation of Electronic Materials. *The Electrochemical Society Interface*, pp. 23-26.

Sharan N. and Rana A. K. (2011). Impact of Strain and Channel Thickness on Performance of Biaxial Strained Silicon MOSFETs. *International Journal of VLSI Design & Communication Systems*, vol. 2, no. 1, pp. 61-71.

Sharma R. K, Gupta M and Gupta R.S. (2009). Two-Dimensional Analytical Subthreshold Model of Graded Channel DG FD SOI n-MOSFET with Gate Misalignment Effects, *Superlattices and Microstructures*, vol. 45, pp. 91-104.

Silvaco. (2009) *ATLAS and ANTHENA User Manual: Device and Process Simulation Software*: Silvaco International.

Silvaco (2012), *TCAD Services*, www.silvaco.com

Stern F. (1972). Self Consistent Results for n-Type Si Inversion Layers. *Phys. Rev. B. Condens. Matter*, vol. 5, no. 12, pp. 4891-4899.

Sugii N, Hisamato D, Washio K, Yokoyama N and Kimura S. (2002). Performance Enhancement of Strained Si MOSFETs Fabricated on a Chemical-Mechanical-Polished SiGe Substrate. *IEEE Trans. On Electron Devices*, vol. 49, no. 12, pp. 2237-2243.

Takagi S, Maeda T, Numata T, Usuda K and Tanabe A et al (2004). Device Characterization and Physical Models of Strained Si Channel CMOS. *Proc. IEEE Int. Conference on Microeletronic Test Structure*, vol. 17, pp. 133-138.

Tan M. L. P, Arora V. K, Saad I, Ahmadi M. T. and Ismail R. (2009). The Drain Velocity Overshoot in an 80 nm Metal Oxide Semiconductor Field Effect Transistor, *Journal of Applied Physics*, vol. 105, pp. 074503.

Tan M. L. P. and Ismail R. (2007). Modeling of Nanoscale MOSFET Performance in the Velocity Saturation Region. *Jurnal Elektika*, vol. 9, no. 1, pp. 37-41.

Taur Y and Ning T. H. (2009). *Fundamental of Modern Devices.* Cambridge University Press.

Tenuka T, Nakaharai S, Moriyama Y, Hirashita N and Toyodo E. et al (2007). Strained SOI/SGOI Dual Channel CMOS Technology Based on the Ge Condensation Technique. *Semiconductor Science and Technology*, vol. 22, no. 1, pp. 93-98.

Thoma K. H. Th. (1999). Physical Device Models: A Potential Tool in Investigation Conductivity in Ionix and Moxed Conductors. *Ionics*, vol. 5, pp. 76-79.

Thompson S. E, Sun G, Choi Y. S. and Nishida T. (2006). Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap. *IEEE Trans. on Electrons Devices*, vol. 53, no. 5, pp.1010-1020.

Thompson S. E. and Parthesarathy S. (2006). Moore's Law: The Future of Si Microelectronics. *Materials Today*, vol. 9, pp. 20-25.

Tinoco J. C, Garcia R, Iniguez, Cerdeira A, and Estrada M. (2008). Threshold Voltage Model for Bulk Strained Silicon NMOSFETs. *Semicond. Sci. Technol*, vol. 23, pp. 035017.

Tripathi S and Jit S. (2011). Journal of Semiconductor Technology and Science, vol. 11, no. 1, pp.40-50.

Tsang Y. L, Charropadhyay S, Uppal. S, Escobedo-Cousin E and Ramakrishnan H. K. et al (2007). Modeling of the Threshold Voltage in Strained Si/Si1-xGex/Si1-yGey (x>y) CMOS Architectures, *IEEE Trans. on Electron Devices*, vol. 54, no.11, pp. 3040-3048.

Tsividis Y. (1999). Operation and Modeling of the MOS Transistor. 2nd ed. New York USA, McGraw-Hill, Inc.

Van de Walle C. G and Martin R. M. (1986). Theoretical Calculations of Heterojunction Discontinuities in the Si/Ge System, *Physical Review B (Condensed Matter)*, vol. 34, pp. 5621-5634.

Venkataraman V, Nawal S. and Kumar M. J. (2007). Compact Analytical Threshold Voltage Model of Nanoscale Fully Depleted Strained-Si on Silicon-Germanium-on-Insulator (SGOI) MOSFETs. *IEEE Trans. On Electron Devices*, vol. 54, no. 3, pp. 554-561.

Verhulst A. S, Soree B, Leonelli D. Vandenberghe W.G, and Groeseneken G. (2010). Modeling the Single Gate, Double Gate, and Gate-All-Around Tunnel Field Effect Transistor, *Journal of Applied Physics*, vol. 017, pp. 024518-8

Wang L. H. (2006). *Quantum Mechanical Effects on MOSFET Scaling Limit.* Georgio Institute of Technology, PhD Thesis.

Wolf H. F. (1971). *Semiconductors*, New York: Wiley-Interscience.

Wuyun Q, Kim D. M. and Hi-Deok L. (2002). Quantum C-V Modeling in Depletion and Inversion: Accurate Extraction of Electrical Thickness of Gate Oxide in Deep

Submicron MOSFETs, *IEEE Trans. on Electron Devices*, vol. 49, no. 5, pp. 889-894.

Yang F. L, Chen H. Y, Chen F. C, Chan Y. L and Yang K. N. et al (2002). 35 nm CMOS FinFETs. *Digest of Technical Papers, Symposium on VLSI Technology*, pp. 104-105.

Yau L. D. (1974). A Simple Theory to Predict the Threshold Voltage of Short Channel IGFETs. *Solid State Electronics*, vol. 17, pp.1059-1063.

Yeo Y. C, Qiang L, King T. J, Hu C. M and Kawashima T. et al (2000). Enhance Performance in Sub 100 nm CMOSFETs using Strained Epitaxial Silicon-Germanium. *International Electron Devices Meeting, Technical Diges*t, pp. 753-756.

Young K. K. (1989). Short Channel Effect in Fully Depleted SOI MOSFETs. *IEEE Trans. Electron Devices*, vol. 36, no. 2, pp. 399-402.

Yousif M. Y. A, Nur O, Chretien O, Fu Y. and Willander M. (1998). Threshold Voltage and Charge Control Consideration in Double Quantum Well Si/SiGe p-Type MOSFETs. *Solid State Electronics*, vol. 42, pp. 951-956.

Yu B, Chang L, Ahmed S, Wang H and Bell S. et al (2001). FinFet Scaling to 10 nm Gate Length. *IEEE Int. Electron Device Meeting,* pp. 251-254.

Yu B, Wang H, Riccobene C, Xiang Q. and Lin M. R. (2000). Limit of Gate oxide Scaling in Nano-Transistors. *2000 Symposium on VLSI Technology Digest of Technical Papers*, pp. 90-91.

Yu S. F, Jung J. W, Hoyt J. L. and Antoniadis D. A. (2004). Strained Si/Strained SiGe Dual Channel Layer Structure as CMOS Substrate for Single Work Function Metal Gate Technology. *IEEE Electron Device Letters*, vol. 25, no. 6, pp. 402-404.

Yuan T, Buchanan D. A, Wei C, Frank D. J and Ismail K. E et al (1997). CMOS Scaling into the Nanometer Regime. *Proceedings of the IEEE,* vol. 85, no. 4, pp. 486-504.

Zainuddin A. N. M and Haque A. (2005). Threshold Voltage Reduction in Strained Si/SiGe MOS Devices Due to a Difference in the Dielectric Constants of Si and Ge. *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2812-2814.

Zednik, R, Lu C. H, Jagannathan, H, McVittie, and J, McIntyre P.C. et al (2004). Experimental Study of Biaxial and Uniaxial Strain Effects on Carrier Mobility in

Bulk and Ultrathin-Body SOI MOSFETs. *IEDM Technical Digest. IEEE International* pp. 229 – 232.

Zeitoff P. M and Chung J. E. (2005). A Perspective From the 2003 ITRS-MOSFET Scaling Trends, Challenges and Potential Solutions. *IEEE Circuit and Devices Magazines*, pp. 4-15.

Zeitzoff P. M. (2006). Trends and Challenges in MOSFETs Scaling. *Solid State Technology*, vol. 49, pp. 42-44.

Zhang W. and Fossum J. G. (2005). On the Threshold Voltage of Strained-Si-$Si_{1-x}Ge_x$ MOSFETs. *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 263–268.

APPENDIX A

LIST OF PUBLICATIONS

A. Journal Papers

1. Eng Siew Kang, Sohail Anwar and Razali Ismail. (2013). Energy Quantization on the Current-Voltage Characteristic of Nanoscale Strained Si / $Si_{1-x}Ge_x$ MOSFETs. International Journal of Modern Physic B. (accepted), IF=0.32
2. Eng Siew Kang, Wei Hong Yau, Sohail Anwar and Razali Ismail. (2012) Two-Dimensional Analytical Threshold Voltage Model of Nanoscale Strained Si/$Si_{1-x}Ge_x$ MOSFETs including Quantum Mechanical Effects. *Journal of Computational and Theoretical Nanoscience*, vol. 9. no. 3, pp. 441-447, IF=0.9
3. Eng Siew Kang, Sohail Anwar and Razali Ismail. (2012). Quantum Mechanical Effect on the Threshold Voltage of Nanoscale Dual Channel Strained Si/Strained $Si_{1-y}Ge_y$/relaxed $Si_{1-x}Ge_x$ PMOSFETs. *Journal of Computational and Theoretical Nanoscience,* (accepted), IF=0.9
4. Eng Siew Kang, Sohail Anwar and Razali Ismail. (2012). Threshold Voltage Variation of Nanoscale Strained Si / $Si_{1-x}Ge_x$ MOSFETs in the Presence of Punch Through Effect. *Journal of Computational and Theoretical Nanoscience,* (accepted), IF=0.9
5. Eng Siew Kang, Sohail Anwar and Razali Ismail. (2012). Quantum Confinement on the Current-Voltage Characteristics of Nanoscale Two-Dimensional MOSFETs. *Jurnal Teknologi*. (accepted), Listed SCOPUS

6. Eng Siew Kang, Fatimah A. Hamid and Razali Ismail. (2012). Einstein Relation of Two-Dimensional Strained Si/$Si_{1-x}Ge_x$ PMOSFETs in Nondegenerate Regime and Degenerate Regime. *International Journal of Nano Devices, Sensors and Systems*, Vol. 1, No. 1, 2012.
7. Eng Siew Kang, Sohail Anwar Mohammad Taghi Ahmadi and Razali Ismail. (2012). Impact of Germanium in Strained Si/Relaxed $Si_{1-x}Ge_x$ on the Carrier Performance in Nondegenerate and Degenerate Regime. *Journal of Semiconductor* (accepted).

B. Book Chapter

1. Eng Siew Kang and Razali Ismail (2012). *Advanced Nanoelectronics: Quantum Mechanical Effects in Nanometer Scale Strained Si/$Si_{1-x}Ge_x$ MOSFETs*, December 2012: CRC Press / Taylor and Francis Group. ISBN 9781439856802

C. Conference Papers

1. Eng Siew Kang, Mohammad T.Ahmadi, Munawar A Riyadi and Razali Ismail. (2009). Numerical Study of Diffusion Current Characteristic for Non-Degenerate N-type Strained Silicon MOSFETs. *Proceedings of International Conference on Basic and Applied Science and Regional Annual Fundamental Science Seminar*, Johor Bahru, 2-4 June, (ICORAFSS 2009)
2. Eng Siew Kang, Mohammad T. Ahmadi, Wei Hong Yau and Razali Ismail. (2009). Current Characteristic for High Performance Strained Silicon NMOSFETs. *Proceeding of 2009 Regional Symposium on Microelectronics,* Kota Bharu, Kelantan, 10-12, pp. 209-212 (RSM 2009)
3. Eng Siew Kang, Kiani M. J, Hedayat S. N. Ahmadi M. T, Hamzah M. A and Razali Ismail.(2012). Analytical Study of the Intrinsic Velosity of Nanoscale

Strained Silicon MOSFETs, Including the Effects of Germanium. *Isfahan's Electrical Engineering National Conference*.

4. Munawar. A Riyadi, Mohammad T. Ahmadi and Jatmiko E. Suseno, Eng Siew Kang, Ismail Saad, Razali Ismail and V. K. Arora. (2009). Physics-Based Simulation of Carrier Velocity in 2-Dimensional P-type MOSFET. *Proceedings of 2009 3rd Asia International Conference on Modelling and Simulation, AMS*, pp. 735 -738.
5. Yu Chan Thien, Eng Siew Kang and Razali Ismail. (2012). Simulation of Nanoscale Dual-channel Strained Si/$Si_{1-x}Ge_x$ Silicon PMOSFET. *10th IEEE International Conference on Semiconductor Electronics*.