THE RTL DESIGN OF 32-BIT RISC PROCESSOR USING VERILOG HDL

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To my beloved family, friends and lecturers who have guided and inspired me along this journey.

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ABSTRACT

The objective of this research is to design a Reduced Instruction Set Computer (RISC) processor core based on ARM instruction set architecture for System-on-Chip (SoC) development design. The RISC computer architecture is selected because as it is accepted as the processor for mobile computing and in SoC based design computing system. Moreover, it reduces processor complexity by reducing its instruction set from highly complex microprogrammed instruction set into a limited number of instruction that can completely executes one instruction in one cycle. As System on Chip (SoC) becomes an amazing solution in various applications such as hardware accelerator for video and image processing system in an embedded system, importance of microprocessor design in SoC increases for developing an optimal embedded system which are fast, small memory size, and low power consumption.

ABSTRAK

Objektif kajian ini adalah untuk mereka bentuk Set Arahan Mengurangkan Komputer (RISC)pemproses teras yang berdasarkan seni bina ARM set arahan untuk pembangunan reka bentuk Sistem-atas-cip (SoC).Seni bina RISC komputer dipilih kerana kerana ia diterima sebagai pemproses untuk pengkomputeran mudah alih dan dalam sistem komputerberasaskan SoC. Selain itu, ia mengurangkan kerumitan pemproses dengan mengurangkan set arahan daripada set arahan yang sangat kompleks microprogrammedkepada beberapa arahan yang terhad yang boleh benar-benar melaksanakan satu arahan dalam satu kitaran. Sebagai Sistem atas Cip (SoC) menjadi satu penyelesaian yangmenakjubkan dalam pelbagai aplikasi seperti pemecut perkakasan bagi sistem pemprosesan video dan imej dalam sistem terbenam, kepentingan reka bentuk mikropemproses di SoC meningkAt bagi membangunkan sistem optimum yang tertanamyang cepat, memori saiz yang kecil, dan penggunaan kuasa yang rendah.

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LIST OF ABBREVIATIONS

RISC	-	Reduced Instruction Set Computer
CISC	-	Complex Instruction Set Computer
SoC	-	System-on-Chip
ISA	-	Instruction Set Architecture
PC	-	Program Counter
OPCODE	-	Operation Code

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CHAPTER 1

INTRODUCTION

This project report is about 32-bit 5-stage pipeline RISC processor design based on ARM instruction set architecture and format. This chapter discusses the introduction to this project which covers the background research, research motivation, scope of work and the report organization. The problem statement and the objective that lead to implementation of this project are also discussed.

1.1 Research Background

Microprocessor is one of the greatest inventions in 20^{th} century to fulfill the people needs such as in daily works and communications where nowadays, people are communicating anytime and from anywhere [1]. As a result, people need a communication device such smartphone or tablet computer for them to communicate with various high end applications running on that device which need a high end computing system. RISC is one of the simple and yet popular processor architectures in computing industry [1]. To develop a high performance computing, yet lower powered and small area usage, a microprocessor system which meet that specification must be design.

In this project, a processor is designed which is based on RISC processor design. The design philosophy of RISC processor is to reduce the complexity of the ISA by limiting the instruction set in to a smaller number of more frequently used instruction that yields better efficiency in modern computing [2].

Besides, the RISC processor throughput is improved by implementation of the pipeline mechanism that brings the processor to achieve a high performance in speed because all the operations are done by the registers. RISC architecture was first introduced by IBM in 1975 [16]. However, RISC designs such as Berkeley's RISC processor and Stanford's MIPS processor which were introduced by respective university research teams were gaining higher popularity in term of public RISC design [16].

1.2 Project Background

The RISC processor design proposed is based on ARM processor core architecture is designed using Verilog HDL design entry and the design methodology is based on hierarchical modularity of RTL design methodology so that the functional unit of the processor can be modeled using behavioral programming style and the all functional blocks will be integrated into a system using structural modeling technique for both processor core datapath and control unit design.

Hardwired control approach will be applied to design the control unit as against microprogrammed control approach in conventional Complex Instruction Set Computer (CISC) processor [11]. CISC processor has gained the major marketplace in world of computing over the decades [5]. They support various addressing modes and data types. The instruction is complex and the length is varies from one instruction to another instruction [6]. The CISC processor is also frequently accessing data in external memory for the processor to execute its instruction and this is very slow [5].

Compared to RISC processor, it operates on very few data types, simple and yet limited addressing modes, and does only the simple instructions [5]. It supports very few addressing modes and is mostly register based. Most of the instructions operate on data present in the register files, so called register-to-register operation, and this is faster than CISC's memory-to-memory operation [6]. Only load and store data from and into memory are working on memory accessing. Furthermore, the RISC instruction length is fixed and hence the decoding technique is easier compared to CISC microprogrammed decoding technique to generate the control signals [6].

Parallel execution of instructions through the pipelined mechanism of processor will improves the overall throughput [4]. The ARM architecture is used as guidance to design the RISC processor because of successful design of its architecture in many embedded systems as well as mobile computing. The SoC design could be used to develop various fast, small die area size usages and yet low powered embedded system as well mobile computing [4].

1.3 Problem Statement

Nowadays, System-on-Chip (SoC) becomes a realistic solution in various application domains such as cryptography, image processing system and digital signal processing in various embedded system such as mobile smart phones, portable gaming gadget as well as mobile computing. SoC is bringing down their complex algorithm that demanding a heavy computation into hardware, implemented as an Application Specific Instruction Set Processor (ASISP) as co-processor or more specific as a hardware accelerator for a processor core which is faster instead of implementation on software on the same platform. The idea of this project is to bring down the heavily computation and complex algorithm from the software realm to the hardware realm [6] to perform a specific instruction which is can be performed faster in hardware so that the application is mainly depends on hardware instead of software by designing a processor core that is open to work with any ASIC design and becomes a system that is called System-on-Chip (SoC) [6].

1.4 Objective

The objective of this project is to study, design, and validate a 32-bit 5-stage pipeline RISC processor based on ARM instruction set architecture and format. It covers the study of ARM core architecture datapath design and investigation on how the processor executes it's instruction.

1.5 Scope of Work

The scope of works in this project covers the design of a 32-bit RISC processor with implementation of 5-stage pipeline that can execute three main types of ARM instruction set architecture which are data processing, single data transfer, as well as branching. The project covers the design entry using Verilog HDL and synthesizing using Altera Quartus II Tool.

1.6 Project Schedule

The project is scheduled for two semesters, which is span for eight months. The hardware specification and requirement were derived in the first semester while the Verilog HDL coding, synthesis, compilation, simulation, and validation for the design processor were done in the second semester.

1.7 Report Outline

Report outline discusses the content in each chapter of this project report.

Chapter 1 A brief introduction to the research and project background, the project's objectives and scopes covers in this project, and the organization of this project report.

Chapter 2 Introduction to the instruction set architectures, pipelining mechanism, basic processor's functional units needed to design a RISC processor, and the previous works done.

Chapter 3 Research and design methodology that applied to design the processor and the tools used.

Chapter 4 Discussion of the processor design and the performance analysis.

Chapter 5 Conclusion and suggestion for future works.

1.8 Summary of Chapter 1

Research and project background, objective of the project, scope of work, and significance of this research has been discussed. The project report organization is also discussed.

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