RECONFIGURABLE ADDRESS GENERATION UNIT FOR 2D CORRELATION IN FPGA

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To my beloved father and mother

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ABSTRACT

2D correlation has been commonly used in image processing. In general, performance of the 2D correlation function depends on its processing speed, memory speed as well as address calculation speed. As the processing and memory speed increase, the address calculation speed becomes bottleneck for overall performance. It is thus necessary to accelerate the address calculation or generation by implementing it in hardware like FPGA rather than depending on software to calculate the addresses; such hardware is known as address generation unit (AGU). Prior arts of reconfigurable AGU can be reconfigured to generate address for different digital signal processing (DSP) functions including 2D correlation; however, they don't support address generation for different designs of 2D correlation circuits. None of the prior arts of AGU able to handle image edge condition while considering data reuse in 2D correlation circuit. Furthermore, prior arts of AGU have never been implemented in FPGA. In this paper, a reconfigurable AGU for different designs of 2D correlation in FPGA, which takes care of image edge condition while considering data reuse, is presented. The proposed reconfigurable AGU is targeted for two different architectures of 2D correlation circuit. The two architectures of 2D correlation circuit, which work together with the reconfigurable AGU, are also designed. The proposed reconfigurable AGU reduces the circuit area by sharing or reusing the common components such as adder, comparator, register and etc. In general, the reconfigurable AGU reduces circuit area by 30% as compared to integrating two dedicated AGUs for two different architectures of 2D correlation circuit. The maximum speed of the reconfigurable AGU is 125MHz for Cyclone III device targeting FPGA.

ABSTRAK

Korelasi 2D telah biasa digunakan dalam pemprosesan imej. Secara amnya, prestasi fungsi korelasi 2D bergantung kepada kelajuan pemprosesan, kelajuan memori serta kelajuan untuk alamat pengiraan. Selaras dengan peningkatan kelajuan pemprosesan dan memori, kelajuan alamat pengiraan menjadi kejejalan untuk prestasi keseluruhan. Oleh itu, adalah perlu untuk mempercepatkan pengiraan alamat dengan meggunakan perkakasan seperti FPGA dan bukannya bergantung kepada perisian untuk mengira alamat; perkakasan itu dikenali sebagai "unit pengenerasi alamat" (AGU). Generasi AGU yang lama boleh diatur semula untuk menjana alamat untuk fungsi pemprosesan isyarat digital (DSP) yang berbeza termasuk korelasi 2D; bagaimanapun, mereka tidak menyokong pengiraan alamat untuk litar korelasi 2D dengan reka bentuk yang berbeza. Tambahan pula, generasi AGU terlebih dahulu tidak pernah dilaksanakan di FPGA. Dalam kertas ini, AGU yang boleh dikonfigur semula untuk korelasi 2D dengan reka bentuk yang berbeza di FPGA, yang mengambil peduli keadaan tepi imej sambil mempertimbangkan penggunaan semula data, dibentangkan. AGU yang dicadangkan mensasarkan untuk dua litar korelasi 2D dengan reka bentuk yang berbeza. Kedua-dua litar korelasi 2D, yang bekerja bersama-sama dengan AGU, juga direka. AGU cadangan mengurangkan kawasan litar dengan berkongsi atau menggunakan semula komponen yang sama seperti penambah, komparator, "register" dan sebagainya. Secara amnya, AGU yang boleh dikonfigur semula mengurangkan kawasan litar sebanyak 30% berbanding dengan mengintegrasikan dua AGU yang berlainan untuk dua litar korelasi 2D yang berbeza. Kelajuan maksimum untuk AGU yang boleh dikonfigur adalah 125MHz untuk "Cyclone III" yang mensasarkan FPGA.

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LIST OF ABBREVIATIONS

AGU	-	Address Generation Unit
ASM	-	Algorithmic State Machine
DSP	-	Digital Signal Processing
FPGA	-	Field-Programmable Gate Array
RTL-CS	-	Register Transfer Level – Control Signal
2D	-	Two Dimension

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CHAPTER 1

INTRODUCTION

1.1 Problem Background

Nowadays, image processing has been used in a wide range of applications such as photography, medical imaging, forensics, transportation, military applications and etc. There are a number of digital signal processing (DSP) algorithms or functions available to be used in image processing, they are 2D convolution, 2D correlation, fast Fourier transform (FFT), filtering and etc. 2D correlation is one of the commonly used DSP functions in image processing. Depending on the types of kernel, 2D correlation can be used to serve different purposes in image processing such as smoothing, noise elimination and edge detection.

As image is normally stored in memory, it is necessary to read image from memory for 2D correlation processing and store the result into memory after processing as shown in Figure 1.1. For 2D correlation processing, it is required to feed the data path with the input data in certain order depending on the design of data path. Since image to be processed is stored in memory, it is necessary for data to be accessed in such order or sequence as well. In other words, addresses in such sequence are needed to supply to memory. Thus, it is necessary to calculate or generate address sequence for reading image data as well as for storing result. Some applications rely on software to calculate the address sequence which is inefficient and time consuming.

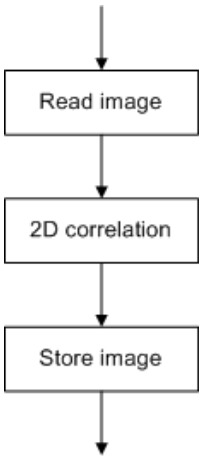

Figure 1.1: Image read and store for 2D correlation.

1.2 Problem Statement

For real time and faster application, 2D correlation is often implemented in hardware to accelerate the computation. Performance of the 2D correlation processing is not only depends on the speed of 2D correlation circuit itself, but also memory speed as well as address calculation speed. As the processing and memory speed increase, the address calculation speed becomes bottleneck for overall performance.

It is thus necessary to speed up the address calculation or generation by implementing it in hardware like FPGA rather than depending on software to calculate the addresses; such hardware is known as address generation unit (AGU). To ensure that the AGU can accelerate, the AGU should have its own datapath instead of sharing with 2D correlation for address calculation.

Prior arts of reconfigurable AGU can be reconfigured to generate address for different digital signal processing (DSP) functions including 2D correlation; however, they don’t support address generation for different types of designs of 2D correlation circuit. None of the prior arts of AGU able to handle image edge condition while considering data reuse in 2D correlation circuit. Prior arts of reconfigurable AGU normally have a number of processing units each for generating address dedicatedly

for different addressing sequence resulting in inefficient design and larger circuit area. Furthermore, prior arts of AGU have never been implemented in FPGA.

Therefore, it is necessary to design and implement a reconfigurable AGU for different designs of 2D correlation in FPGA with minimal circuit area, which takes care of image edge condition while considering data reuse.

Some challenges were encountered along the design and implementation phase of the project. One of the challenges is that there is not much implementation details can be obtained from the prior arts of AGU. Address calculation for Arch2 (refer to section 4.4), which is column by column basis, is quite challenging when image border is taken into account of consideration as none of the prior arts has done it before. Another challenge is the timing consideration of internal signals in AGU. In addition, interface and timing issue between AGU and 2D correlation circuits are the most time consuming part during the design phase. The circular buffer is designed in Arch2 (refer to section 4.3) for data reuse; in order to make Arch2 reconfigurable for different kernel sizes, parameterized coding is involved. The parameterized coding is quite tedious and time consuming.

1.3 Objectives

The objective of this project is to design a reconfigurable AGU for 2D correlation in FPGA. The 4 main objectives accomplished in this project are shown below.

1. The reconfigurable AGU can generate address sequence for reading out image data needed for 2D correlation processing from a memory; and can also generate address sequence for storing the result or output image into memory.
2. The AGU can be configured to generate address sequence for different designs of 2D correlation.

3. The AGU can also be configured to generate address sequence for different image dimensions and kernel sizes.
4. The reconfigurable AGU can take care of image border while considering data reuse in 2D correlation circuit.

The configuration data, consists of the type of design of 2D correlation circuit, image dimension and kernel size, is specified by the user.

1.4 Scope of Study

The project is targeted for implementation in FPGA. The project is implemented in Verilog code using Quartus II targeting FPGA. The device involved is Cyclone III targeting FPGA. Due to time constraint, the Verilog code is not loaded into FPGA board. Thus, it is limited to simulation based model. In other words, the project is targeted to deliver the simulation model or work of reconfigurable AGU and 2D correlation. The design is simulated on Altera Modelsim. Matlab simulated result is used as a reference to verify the outcome from Modelsim.

A reconfigurable AGU which is targeted to work for two different architectures of 2D correlation is designed. The AGU is also targeted to work for different image dimensions and kernel sizes. The two different architectures of 2D correlation circuit will be designed and implemented as well. Each design of 2D correlation is reconfigurable for different image dimensions and kernel sizes.

As the reconfigurable AGU is the focus of the project, we only aim to design the skeleton of 2D correlation which can work together with the reconfigurable AGU. Thus, the 2D correlation designs are limited to averaging filter and their performances are also limited in term of speed and accuracy. The reconfigurable AGU design is verified with Arch1 and Arch2, as well as sample images and kernels with different sizes.

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