PERFORMANCE COMPARISON OF NxN MATRIX MULTIPLICATION BETWEEN FIELD PROGRAMMABLE GATE ARRAY AND GENERAL PURPOSE PROCESSOR

CHAY CHIN FATT

UNIVERSITI TEKNOLOGI MALAYSIA

PERFORMANCE COMPARISON OF NxN MATRIX MULTIPLICATION BETWEEN FIELD PROGRAMMABLE GATE ARRAY AND GENERAL PURPOSE PROCESSOR

CHAY CHIN FATT

This project report is submitted in partial fulfillment of the requirement for the award of the degree of Master of Engineering (Electrical – Computer & Microelectronic System)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

JUNE 2012

Special dedicated to

My dearest family

ACKNOWLEDGEMENT

I would like to take this opportunity to express my deepest gratitude to Dr Izzeldin Ibrahim Mohamed who had provide valuable feedback and input to me in completing this research. His guidance and advice is a big encouragement to me on successfully completing this research work. Furthermore, I would like to thank my wife (Tang Inn Inn) and my child (Chay Ze Huan) for supporting my academic choice.

ABSTRACT

Era of “on the move with anyone, anytime and anywhere” has become a reality as high performance portable product such as smart phone, and up to more powerful and sophisticated devices such as laptop has become essential electronic equipment for most of people in their daily life. The level of portability of such device directly influences and normally it is a key differentiator factor in a user’s purchase decision. Level of portability is measured in terms of the weight of devices and the interval of recharging. Thus, lowering down the power consumption of devices or circuit and better power management techniques without seriously impacting the overall system performance has become a number one priority. The most apparent reason for low power design is to prolong the battery life of portable electronic devices. And, of course it leads to a smaller battery pack which indirectly reduces the device weight. An excellent design with less power dissipation avoid adding cost for active cooling solution such as fan or even passive cooling solution such as heat sink. In this project report, a hardware oriented n x n matrix multiplication module was designed and implemented on Altera FPGA and it was compared and analyzed to general purpose processor form Intel (both Core i5 Clarkdale and Atom Pineview-D) in term of power and energy consumption.

ABSTRAK

Era "bergerak dengan sesiapa sahaja, pada bila-bila masa dan di mana-mana" telah menjadi benar. Produk berprestasi tinggi mudah alih seperti telefon pintar, dan alat-alat yang lebih berkuasa dan canggih seperti komputer riba telah menjadi peralatan elektronik yang penting dalam kehidupan harian kebanyakan orang. Tahap kemudahalihan peralatan elektronik secara langsung mempengaruhi dan biasanya ia merupakan faktor utama mempengaruhi keputusan pembelian pengguna. Tahap kemudahalihan diukur dari segi berat peralatan dan tempoh penggunaan bateri peralatan. Oleh itu, mengurangkan penggunaan kuasa peralatan elektronik dan teknik-teknik pengurusan kuasa yang lebih baik tanpa memberi kesan kepada prestasi keseluruhan sistem telah menjadi keutamaan. Sebab yang paling ketara untuk mereka peralatan yang menggunakan kuasa yang rendah adalah untuk memanjangkan hayat bateri alat-alat elektronik mudah alih. Lebih lebih lagi ia tentu membawa kepada bateri yang lebih kecil yang secara tidak langsung mengurangkan berat peralatan elektronik. Sesuatu reka bentuk yang baik dengan pelesapan kuasa yang kurang dapat mengelakkan penggunaan kipas angin yang mana akan menambah kos peralatan elektronik. Dalam projek ini, perkakasan berorientasikan pendaraban matriks nxn direka bentuk dan dilaksanakan pada Altera FPGA dan ia akan dibandingkan dengan Intel CPU dari segi kuasa dan penggunaan tenaga.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

CPU	-	Centre Processing Unit
DSP	-	Digital Signal Processing
FPGA	-	Field Programmable Gate Array
LDO	-	Linear Dropout Regulator
MAC	-	Multiplier- Accumulator
PLL	-	Phase-Locked Loop
RAM	-	Random Access Memory
VHDL	-	Very High Speed Integrated Circuit Hardware Description Language
VLSI	-	Very Large Scale Integration

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

This project report evaluates the performance in term of power dissipation, energy efficiency as well as latency of FPGAs and general purpose processor from Intel which are Core i5 Clarkdale and Atom Pineview-D in multiplying two nxn 32 bit matrices and result in one 64 bits matrix. The reason matrix multiplication was chosen is because matrix multiplication is a very basic manipulation of matrix used in wide range of applications like audio, video and image encoder and decoder as well as communication [10]. This chapter covers the background, problem statement and research objective.

1.1 Background

With flexibility and cost effective provided by general purpose processor, one might think that combination of software and general purpose processor is the best solution for most of applications. However, this is totally not true for application which is computationally demanding and application which need real time data processing. The nature of general purpose processor might not yield the highest performance for particular application and on the other hand some application might not fully utilize the entire resources causing more power consumption and lead to energy efficiency issue.

With drastic improvement and mature of Field Programmable Gate Array (FPGA) technology nowadays, FPGAs become one of the choices for designer other than traditionally solution such as general purpose processor and digital signal processor (DSP). Its nature of reconfigurable and can be programmed to implement any digital circuit make it a best candidate for most of data computation extensive application compare to general purpose processor. This is including area such as signal processing and encryption engine which involves large amount of real time data processing. FPGAs provide better throughput and latency since it is able to be customized to optimize the execution of particular process or algorithm.

Traditionally, research of FPGAs and improvement of FPGAs are mainly focusing on reducing the area overhead and increasing the speed [7]. With emerging of portable and mobile devices which are now become a need of most of people today, performance metrics of any of devices are not mainly focus on latency and throughput but energy efficiency is key factor as well. Apparently, shifting of focus to energy efficiency design on FPGAs is mainly influenced by heavily usage and popularity of mobile devices. On other words, this shift is due to the demanding of low power design on mobile and portable devices and increasing of energy cost. Furthermore, more competitive environment on business electronic devices is driving for lower design cost and cheaper cooling solution which makes low power design an essential requirement on non-mobile electronic devices as well.

As summary, performances of electronic devices are not mainly focusing on just speed but energy efficiency should be listed as a major design consideration.

1.2 Problem Statement

As stated in previous section, performance metric of most signal processing application are mainly focusing on throughput and latency before proliferation of hand held devices recently. But, energy efficiency has become another importance performance metrics to be considered. Battery life of portable devices such as mobile phone or laptop is key differentiator that influences the buying decision of consumer. Better energy efficiency design means longer battery life and lead to smaller battery pack for same amount of operating time.

Any of signal processing application or data computation extensive application can be implemented in both hardware and software. For software, it can be easily coded in any high level programming language such as C++ and execute it on a general purpose process or DSP. However, this type of implementation does not yield the higher performance in term of throughput and energy efficiency although it is fairly easy method. In most of signal processing application such as video compression and decompression, data encryption and image processing require real time data processing and it normally involve large amount of data. This brings to the needs of low latency and high throughput. Software approach is typically too slow and not power efficient for such application.

Designers are focusing on producing high throughput solution while maintaining the power consumption low. A lot of study and experiment had been done comparing the energy efficiency between FPGAs, DSPs, embedded processor and general purpose processor. However, particularly on general purpose processor, most of experiment are not comparing to the greatest and latest commercial processor in market which claimed by manufacturer that several low power design techniques had been adopted. With the advance of semiconductor process

technology nowadays which lead to lower leakage current, and flexibility of software implementation for power saving, performance of general purpose processor in term of power dissipation and energy consumption had greatly improved. The key question here is how well current modern general purpose processor in market performs in term of energy efficiency compares to FPGAs particularly on signal processing centric application. This project report is going to evaluate and discuss in detail this key question by executing nxn matrix multiplication on Altera FPGA and Intel processor and comparing the performance of both devices in term of power dissipation and energy efficiency.

1.3 Objective

Major objectives had been identified for this project report as following:

i. Design a nxn matrix multiplication module which multiply two 32bit nxn matrices and result in 64 bit matrix. The matrix multiplication module is based on systolic array architecture and Verilog is the hardware description language used. The designed module has to be implemented in Altera FPGA DE2 evaluation board.

ii. From the matrix multiplication module design in (i), power and energy measurement need to be taken on different matrix sizes. The same matrix multiplication process needs to be coded in Mathlab and execute on Intel Core i5 and Atom Pineview-D. Power and energy consume by processor will be measured on different matrix sizes.

iii. Data obtain from (ii) are analyze and compare. Base on the overall data collected, between FPGA and general purpose processor, conclusion and proposal should be made on which solution is more energy efficient.

1.4 Scope of Work

The following outlines the scope of work of this project report. Basically, it is consist of 5 major scopes.

i. Design a hardware oriented matrix multiplication module which multiply two 32 bit nxn matrixes and result in 64bit output and implement in Altera FPGA. Figure 1.1 below shows the high level block diagram of the matrix multiplier. Two 32 bit matrices to be multiplied are stored in Matrix A1 and Matrix A2 RAMs respectively. These two matrices are given to multiplication processor design base on systolic array architecture.

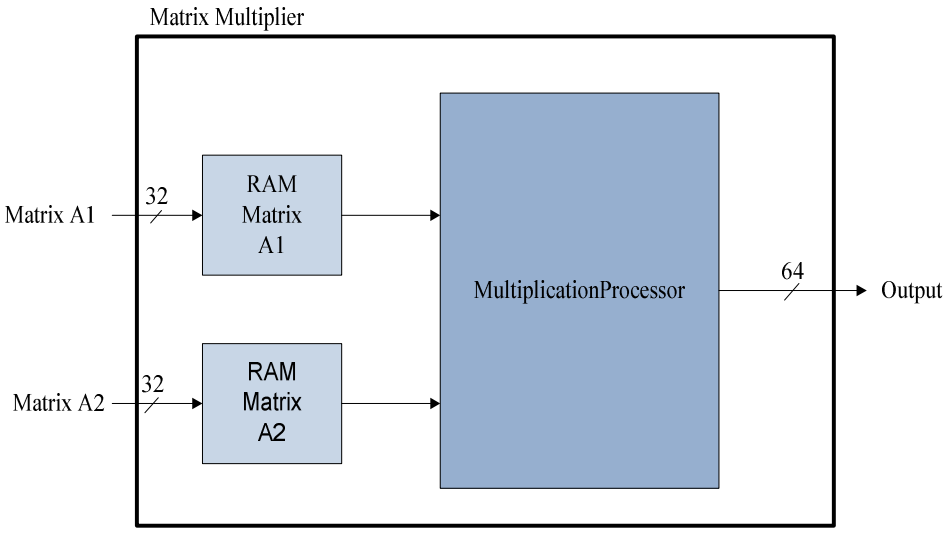

Figure 1.1 High Level Block Diagram of Matrix Multiplier

ii. The same matrix multiplication process will be coded in Mathlab and runs on Intel Core i5 and Atom Pineview-D general purpose processor.

iii. The design matrix multiplier which is implemented in Altera FPGA will be compared and analyzed to general purpose processor in term of performance which includes power, energy consumption as well as latency on different value of n.

iv. Energy consume by general purpose processor will be determined by measuring the actual current consume on each power rail to the running computer system and this was done by using current probe together with a digital oscilloscope. Total execution time needed for energy calculation will be determined by using tic-toc function in Mathlab.

REFERENCES

1. R. Scrofano, S. Choi, and V. K. Prasanna, “Energy Efficiency of FPGAs and Programmable Processors for Matrix Multiplication,” in Proc. of IEEE Intl. Conf. on Field Programmable Technology, pp. 422-425, 2002.e
2. S. Choi, V. K. Prasanna, and J. Jang, “Minimizing energy dissipation of matrix multiplication kernel on Virtex-II,” in Proc. of SPIE, Vol. 4867, pp. 98-106, 2002.
3. J. Jang, S. Choi, and V. K. Prasanna, “Energy efficient matrix multiplication on FPGAs,” in Proc. of 12th Intl. Conf.on Field Programmable Logic and Applications, pp. 534-544, 2002.
4. J. Jang, S. Choi, and V. K. Prasanna, “Area and Time Efficient Implementations of Matrix Multiplication on FPGAs,” in Proc. of IEEE Intl. Conf. on Field Programmable Technology, pp. 93-100, 2002.
5. H. T. Kung and C. E. Leiserson, “Systolic arrays for (VLSI),” *Introduction to VLSI Systems*, 1980
6. V. K. P. Kumar and Y. Tsai, “On synthesizing optimal family of linear systolic arrays for matrix multiplication,” *IEEE Trans Comput.*, vol. 40, no. 6, pp. 770–774, 1991.
7. Lamoureux J and Luk, W,“An overview of Low-Power Techniques for Field-Programmable Gate Arrays.”, in Adaptive Hardware and System, 2008. AHS’08. NASA/ESA
8. Sutter, G., Boemo, E. "Experiments in low power FPGA design", Lat. Am. Appl. Res., vol.37, no.1, pp.99-104, 2007.
9. Dave. N, Fleming. K, Myron King, Pellauer. M, Vijayaraghavan, M. “Hardware Acceleration of Matrix Multiplication on a Xilinx FPGA”, in Formal Methods and Models for Codesign, 2007. MEMOCODE 2007. 5th IEEE/ACM International Conference, May 30 2007-June 2 2007.

10. Aslan. S, Desmouliers. C., Oruklu. E and Saniie. J. “An Efficient Hardware Design Tool for Scalable Matrix Multiplication”, in Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium, pp1262-1265, 2010
11. H.T. Kung. “Why Systolic Architecture”, in IEEE computer, 1982, pp37-46.
12. Ju-Wook Jang, Seonil B. Choi and Viktor K. Prasanna. “ Energy and Time Efficient Matrix Multiplication on FPGAs”, in IEEE transactions on very large scale integration (VLSI) system vol 13, NO 11, November 2005.
13. Qasim, S.M, Abbasi S.A, Almashary B. “ A proposed FPGA-based parallel architecture for matrix multiplication”, in circuits and systems, 2008, APCCAS 2008, IEEE Asia Pacific Conference, pp1763-1766, 2008.
14. Syed M, Qasim, Ahmed A.Telba, Abdulhameed Y. AlMazroo. “FPGA Design and Implementation of Matrix Multiplier Architectures for Image and Signal Processing Applications”, in IJCSNS International Journal of Computer Science and Network Security, VOL 10. NO2, Feb 2010.
15. AHM Shapri and N.A.Z Rahman. “Performance Analysis of Two-Dimensional Systolic Array Matrix Multiplication with Orthogonal Interconnections”, in International Journal on New Computer Architectures and Their Applications (IJNCAA) 1(3): 1090-1100, 2001
16. Jonathan Break. “Systolic Array and their Application”, in http://www.cs.ucf.edu/courses/cot4810/fall04/.../Systolic_Arrays.ppt
17. Altera Inc, Cyclone II Device Handbook, Volume 1, available at www.altera.com
18. Altera Inc, DE2 Development and Education Board Use Manual available at www.altera.com
19. Altera Inc DE2 Development and Education Board Schematic, available at www.altera.com