DESIGN OF AN OFDM TRANSMITTER AND RECEIVER USING FPGA

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ABSTRACT

Orthogonal Frequency Division Multiplexing (OFDM) is a multi carrier modulation technique. OFDM provides high bandwidth efficiency because the carriers are orthogonal to each others and multiple carriers share the data among themselves. The main advantage of this transmission technique is their robustness to channel fading in wireless communication environment. The main objective of this project is to design and implement a base band OFDM transmitter and receiver using FPGA. This project focuses on the core processing block of an OFDM system, which are the Fast Fourier Transform (FFT) block and the Inverse Fast Fourier Transform (IFFT). The 8 points IFFT / FFT decimation-in-frequency (DIF) with radix-2 algorithm is analyzed in detail to produce a solution that is suitable for FPGA implementation. The FPGA implementation of the project is performed using Very High Speed Integrated Circuit (VHSIC) Hardware Descriptive Language (VHDL). This performance of the coding is analyzed from the result of timing simulation using Altera Max Plus II.

ABSTRAK

Orthogonal Frequency Division Multiplexing (OFDM) atau Pemultipleksan Pembahagian Frekuensi Orthogonal adalah sejenis pemodulation pelbagai pembawa. OFDM menyediakan kecekapan lebar jalur yang lebih tinggi kerana pemodulatan pelbagai pembawa mempunyai ciri-ciri dimana setiap pembawa aalah ortoganal sesama sendiri dan data di kongsi bersama setiap pembawa. Kebaikan utama jenis pemodulatan pelbagai pembawa ini adalah ia tidak terjejas kepada *channel fading* dalam komunikasi tanpa wayar. Tujuan utama projek ini adalah merekebentuk dan melaksanakan satu penghantar (transmitter) and penerima (receiver) OFDM. menggunakan FPGA. Projek ini tertumpu kepada struktur pemprosesan utama dalam satu OFDM system, iaitu, blok Jelmaan Fourier Pantas atau *Fast Fourier Transform (FFT)* dan block Songsangan Jelmaan Fourier Pantas atau *Inverse Fast Fourier Transform (IFFT).* 8 sampel blok Jelmaan Fourier Pantas dan Blok Songsangan Jelmaan Fourier Pantas (IFFT) menggunakan pembahagian dalam frekuensi (DIF) dengan pembahagian 2 atau *radix-2* dikaji dengan teliti untuk menghasilkan satu kaedah yang sesuai untuk pelaksanaan rekebentuk menggunakan FPGA. Komputer program ditulis menggunakan *Very-High-Speed-Integrated-Circuit (VHSIC) Hardware Descriptive Language (VHDL).* Kod ini diuji dan dianalisis dengan menggunakan keputusan daripada simulasi masa yang dilaksanakan dengan menggunakan Altera Max Plus II.

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CHAPTER 1

INTRODUCTION

1.1 Digital Communication System Structure

A digital communication system involves the transmission of information in digital form from one point to another point as shown in Figure 1.1

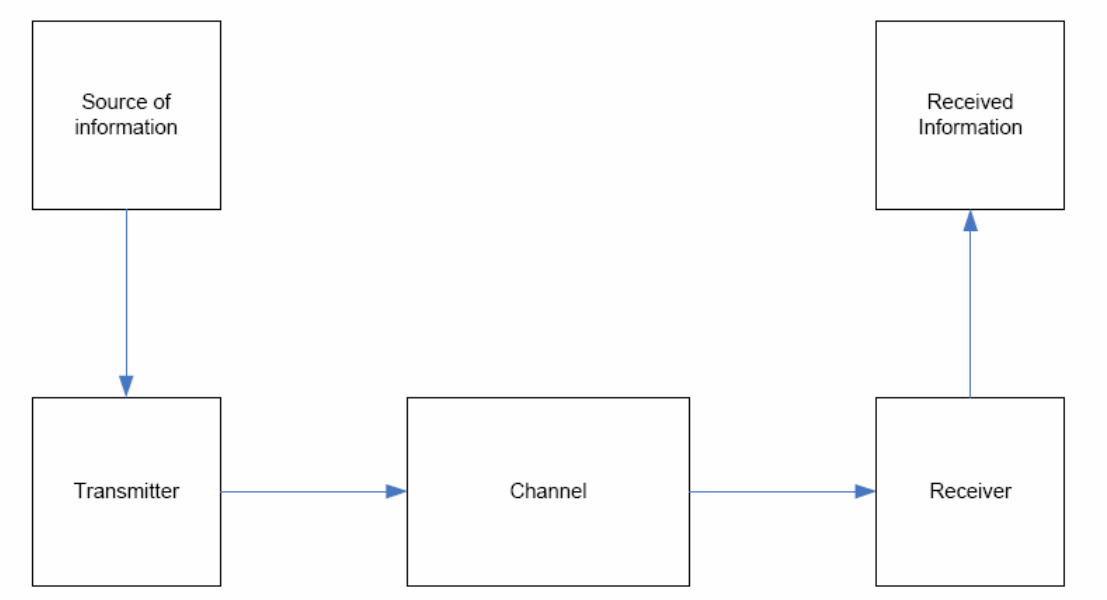

Figure 1.1 Digital Communication Systems

Regardless of the form of communication method, the three basic elements in a communication system consist of transmitter, channel and receiver.

The source of information is the messages that are to be transmitted to the other end in the receiver. A transmitter can consist of source encoder, channel encoder and modulation. Source encoder employed an efficient representation of the information such that resources can be conserved. A channel encoder may include error detection and correction code. The aim is to increase the redundancy in the data to improve the reliability of transmission. A modulation process convert the base band signal into band pass signal before transmission.

During transmission, the signal experiences impairment which attenuates the signals amplitude and distort signals phase. Also, the signals transmitting through a channel also impaired by noise, which is assumed to be Gaussian distributed component.

In the receiver end, the reversed order of the steps in the transmitter is performed. Ideally, the same information must be decoded in the receiving end.

1.2 Project Background

Figure 1.2 and 1.3 show a detailed OFDM transmitter and receiver communications system. In this project, the main focus is in the FFT and IFFT part of the OFDM system.

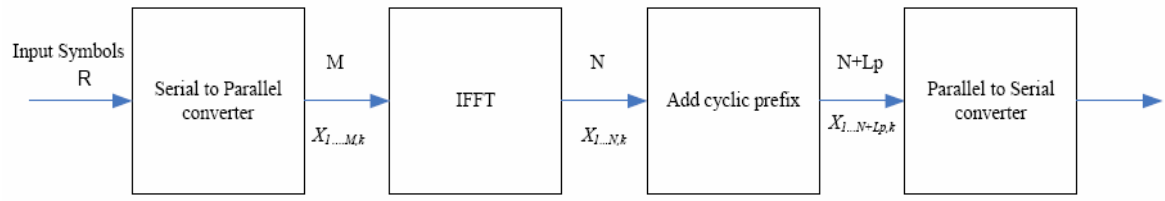

Figure 1.2 OFDM Transmitter

The input symbols are input into the transmitter in series at R symbols/second. These symbols pass through a serial to parallel converter and output data on M lines in parallel. The data rate on every M line is R/M symbols/second.

A symbol in this parallel stream of data is denoted as $X_{i,k}$. The index *i* refer to which sub channel the symbol belongs to, and *i* ranges from 1 to M. The *k* denotes the *k*-th collection of M symbols. The sub symbol collection from $X_{1,k}$ to $X_{M,k}$ makes up an OFDM symbol.

The M symbols are sent to an Inverse Fast Fourier Transform (IFFT) block that performs N-point IFFT operation. The IFFT transform a spectrum (amplitude and phase of each component) into a time domain signal. An IFFT converts a number of complex data points, of length that is power of 2, into the same number of points in time domain. Each data point in frequency spectrum used for an FFT or IFFT operation is called a bin. The output is N time-domain samples.

In order to preserve the sub-carrier orthogonality and the independence of subsequent OFDM symbols, a cyclic guard interval is introduced. Time and frequency synchronization can be established by means of cyclic extension in the prefix and the postfix period.

In this case, assumed a cyclic prefix of length L_p samples is pre-pended to the N samples to form a cyclically extended OFDM symbol. The cyclic prefix is simply the last L_p samples of the N inverse Fast Fourier Transform output samples.

For example, assumed N=4 and L_p=2. If the outputs of a 4 point inverse Fourier transform is [1 2 3 4]. The cyclic prefix will be [3 4]. The cyclically extended symbol would be [3 4 1 2 3 4]. Therefore, the length of the transmitted OFDM symbol is N+ L_p.

Pre-pending the cyclic prefix aids in removing the effects of the channel at the receiver. ISI can occur when multi path channel cause delayed version of previous OFDM symbol to corrupt the current received symbol. If the value of L_p is greater than or equal to the size of the transmission channel, the ISI will only affect the cyclic prefix. The actual OFDM symbol will arrive unchanged.

The cyclic prefix makes the OFDM symbol appear periodic over the band of interest. The cyclically extended symbols are passed through a parallel-to-serial converter. They are transmitted in series across the channel response of the OFDM symbol with the frequency response of the channel.

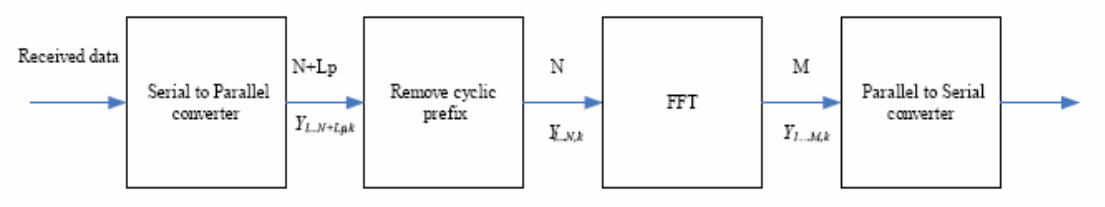

Figure 1.3 OFDM Receiver

The received symbol is in time domain and it is distorted due to the effect of the channel. The received signal goes through a serial to parallel converter and cyclic prefix removal.

After the cyclic prefix removal, the signals are passed through an *N*-point fast Fourier transform to convert the signal to frequency domain. The output of the FFT is formed from the first *M* samples of the output.

1.3 Project Objective

The project aim is to design an OFDM transmitter and receiver using FPGA. The OFDM signal is generated by implementing the Inverse Fast Fourier Transform (IFFT) function at the transmitter. At the receiver end, the Fast Fourier Transform (FFT) is implemented.

The objective of this project is to use High-Speed-Integrated-Circuit (VHSIC) Hardware Description Language (VHDL) to produce VHDL code that carry out FFT and IFFT function.

The synthesis tool utilized is Altera Max Plus II to map the design to targeted device. Validation of the result and timing simulation are also using Altera Max Plus II.

The main challenge in this project is to derive the algorithm that is to be used in this project, for example, the algorithm for Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT). There are many algorithms available that can implement FFT / IFFT.

Second, the author finds it is very challenging on how software algorithm may be mapped to hardware logic. After the simulation result is verified, the process of converting the software statement into VHDL code is a major task. A variable may correspond to a wire or a register depending on its application and sometimes an operator can be mapped to hardware like adder, latches, multiplexers etc.

1.4 Project Scope

The scope of the project is focuses on the design and implementation of OFDM base band transmitter and receiver. This project focuses on the core processing block of the transmitter and receiver, which is the IFFT and FFT block. This design computes 8-points IFFT and implements 8 inputs of real binary bits. The design will discuss on optimization of computational time by using the direct mathematical derivation method.

The implementation of the IFFT and FFT block is using VHDL code. The computation is done in separate sub modules for each output. Each sub module computes a single output path. The combination of eight sub modules produces the complete design of 8 points IFFT and FFT.

1.5 Project Outline

The project is organized into five chapters, namely introduction, literature review, implementation of an OFDM transmitter and receiver based on 8- points inverse Fast Fourier Transform and Fast Fourier Transform, result of VHDL simulation and Conclusion.

Chapter 1 discusses the general idea of the project which cover the overview, project objective, project background and scope of the project.

Chapter 2 shows the literature review of the OFDM system. The history and principle of the OFDM system, Fast Fourier Transform introduction and VHDL programming basic introduction is elaborate in this chapter.

Chapter 3 derives the Fast Fourier Transform and Inverse Fourier Transform algorithm using direct mathematical method. The equations are optimized for digital implementation.

Chapter 4 shows the VHDL simulation output. The results are presented in their sub-modules and then all the modules are combined to give the final output. Then, the VHDL output are compared with Matlab simulation output.

Chapter 5 consists of conclusion, problems encountered in completing this project and suggestion to further improve this project.

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