2-D DWT SYSTEM ARCHITECTURE FOR IMAGE COMPRESSION

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To my dearest family, friends, colleagues and fellow coursemates.

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ABSTRACT

Since the introduction of wavelet transform in early 1980s, it has contributed significantly in multiple areas, such as image processing and compression, radar signal analysis, numerical analysis, biomedical signal processing, medical imaging and digital signal processing. The key advantage of wavelet analysis is the extra time and frequency information compared to other transforms. However, the discrete wavelet transform (DWT) requires very large memory requirement and is computationally intensive, especially for 2-D transform. Typically, it has quadratic computational complexity. In this project, we propose a fully dedicated processor which specialized in 2-D DWT. This architecture aims to achieve improvements on throughput, scalability and flexibility compared to other prior architectures. This architecture requires significantly less computational resources and internal memory. The proposed architecture can achieve threoritical throughput of 138fps for a 2048x1566 video processing. The DWT system has been designed for scalability by supporting up to 8 parallel DWT engines and each DWT engine can work independently. The DWT system architecture is very flexible and the performance can be scaled by increasing or reducing the DWT engines, according to different application needs. Furthermore, this architecture has been designed with the consideration of integration into existing Advanced Microcontroller Bus Architecture (AMBA) systems in future.

ABSTRAK

Sejak pengenalan jelmaan wavelet pada awal 1980-an, ia telah memberi sumbangan yang ketara dalam pelbagai bidang seperti pemprosesan imej dan mampatan, analisis isyarat radar, analisis berangka, pemprosesan isyarat bioperubatan, imej perubation, dan pemprosesan isyarat digital. Satu kelebihan utama analisis wavelet adalah maklumat tambahan masa dan kekerapan berbanding dengan jelmaan yang lain. Walau bagaimanapun, jelmaan wavelet diskret (DWT) memerlukan keperluan memori yang sangat besar dan pengiraannya sangat intensif, terutamanya bagi jelmaan 2-D. Biasanya, ia mempunyai kerumitan pengiraan kuadratik. Dalam projek ini, kami mencadangkan pemproses berdedikasi penuh yang khusus dalam 2-D DWT. Senibina ini bertujuan untuk mencapai peningkatan dari aspek pengeluaran, skalabiliti dan fleksibiliti berbanding dengan senibina yang lain terlebih dahulu. Senibina ini memerlukan sumber pengiraan dan memori dalaman yang amat kurang. Senibina yang dicadangkan boleh mencapai pengeluaran secara teori sebanyak 138fps untuk pemprosesan video 2048x1566. Sistem DWT telah direka untuk skalabiliti supaya menyokong sehingga 8 DWT enjin secara serentak dan setiap enjin DWT boleh beroperari secara bebas. Senibina sistem DWT adalah sangat fleksibel dan prestasi boleh dipertingkatkan dengan menambah atau mengurangkan enjin DWT, mengikut keperluan permohonan yang berbeza. Tambahan pula, senibina ini memerlukan sumber pengiraan dan memori dalaman yang sangat kurang. Senibina ini telah direka dengan pertimbangan integrasi ke dalam sistem AMBA yang sedia ada pada masa akan datang.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AMBA	-	Advanced Microcontroller Bus Architecture
ASIC	-	Application Specific Integrated Circuit
AXI	-	Advanced eXtensible Interface
DCT	-	Discrete Cosine Transform
DFG	-	Data Flow Graph
DFT	-	Discrete Fourier Transform
DSP	-	Digital Signal Processor
DWT	-	Discrete Wavelet Transform
FIFO	-	First In, First Out
FL-DWT	-	Fast Lifting Discrete Wavelet Transform
FOPS	-	Filtering Operation Per Second
FPGA	-	Field Programmable Gate Array
FSM	-	Finite State Machine
FT	-	Fourier Transform
HD	-	High Definition
HDL	-	Hardware Description Language
IO	-	Input/Output
JPEG	-	Joint Photographic Experts Group
LC	-	Logic Cell
MAC	-	Multiply And Accumulate
MSE	-	Mean Square Error
POC	-	Proof of Concept
PSNR	-	Peak Signal-to-Noise Ratio
SFG	-	Signal Flow Graph
STFT	-	Short Time Fourier Transform
SVGA	-	Super Video Graphics Array
VGA	-	Video Graphics Array
VLSI	-	Very Large Scale Integration

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

The project proposes a system architecture for 2-D Discrete Wavelet Transform. The main objective is to design a fully dedicated processor optimized for 2-D Discrete Wavelet Transform. This research project is divided into two parts. The first part is an introduction to wavelet theory and review of existing DWT architectures. The second part is the design of a DWT processor with multiple wavelet engines for parallel processing, followed by simulation data and performance analysis of the design.

1.1 Wavelet History

Wavelet transform is a relatively new methodology to analyze and represent a signal. It is proven to be very useful in digital signal processing. Since the introduction of wavelet transform in early 80's, wavelet theories and analysis have contributed significantly in multiple areas, such as image processing and compression, radar signal analysis, numerical analysis, biomedical signal processing, medical imaging and digital signal processing [1].

In general, wavelet transform offers very unique features as compared to Fourier Transform or Cosine Transform [2]. For example:

- Adaptive time-frequency windows
- Less computational complexity
- Lower aliasing distortion for signal processing
- Inherent scalability
- Efficient VLSI implementation

Wavelet transform is a multi-level decomposition of a signal in time-scale domain. The multi-level property allows faster and more accurate calculation. The accuracy is higher because more coefficients or high frequency components are used to represent signal details. The calculation is faster because the low frequency components (slow-changing part) can be represented by lesser coefficients. The resolution can be varied depending on the application or medium of transmission. For a low bandwidth medium, image data can be sent with only low frequency components, by sacrificing some level of details. One major breakthrough as compared with Discrete Cosine Transform (DCT) is wavelet transform does not suffer from the blocky effect. Due to this significant advantage, wavelet transform has been proposed in JPEG 2000 specification. Similar to Fourier Transform, Wavelet Transform also can be categorized into continuous Wavelet Transform and Discrete Wavelet Transform. The DWT concept, first introduced by Mallat in 1989 [3], has found to be very useful in various applications due to ease of implementation. Therefore, DWT design and implementation have become very important.

1.2 Related Works in Wavelet Implementation

There are several DWT implementations using VLSI, with the simplest DWT implementation is one-dimensional DWT filter bank [4]. The filter bank is typically implemented using systolic architecture or parallel architecture. These architectures essentially feed the input data through a chain of filters that perform wavelet transform. Another DWT implementation is the two-dimensional DWT. The 2-D DWT can be implemented by cascading systolic 1-D filters in a parallel array.

The 1-D and 2-D DWT implemented in hardware filters are direct form of DWT, i.e. convolution based wavelet transform. The convolution based wavelet transform involves multiple additions and multiplications, thus the implementations require a lot of adders and multipliers. Another way to reduce DWT computation complexity is Fast Lifting Discrete Wavelet Transform (FL-DWT) [5]. The FL-DWT factors the original DWT into smaller and simpler filtering steps. The number of multiplications has been reduced significantly. Additionally, the coefficients used in FL-DWT can be integers instead of floating points, without experiencing precision loss.

1.3 Problem Statement

The systolic array architecture proposed by Vishwanath, Owens and Irwin in 1995 [4] and parallel architecture proposed by Chakrabarti and Vishwanath in 1995 [6] are based on convolution based DWT. These architectures require large amount of multipliers and adders, resulting in large chip area.

More recent architectures, such as those by Martina, Masera, Piccinini, and Zamboni in 2000 [7], Jamkhandi, A. Mukherjee, K. Mukherjee and Franceschini in 2000 [8], and Petrovsky, Laopoulos, Golovko, Sadykhov, Sachenko in 2001 [9], are based on systems comprising of FPGAs and DSPs. These systems are very flexible, configurable and programmable. However, the system board area is larger because the use of multiple components.

A newer architecture proposed by A. Mansouri and A. Ahaitouf and F. Abdi in 2009 [5] is a lined based Fast Lifting DWT. This is far more superior architecture as it uses significant lesser multipliers, adders and internal memory storage. We believe that the system performance and throughput can be further improved if parallel processing technique incorporated into the architecture presented by Mansouri.

1.4 Objective

Based on the survey of the existing DWT architectures, this project aims to achieve the following improvements:

1. Throughput – to be able to transform a 1024x768 grayscale image at 30 fps frame rate, without using large on-chip memory and tiling technique
2. Scalability – parallel processing that able to be expanded to support higher requirements and reduced to support lower requirements.
3. Flexibility - modular DWT architecture that can be re-used for any application in future

Furthermore, the project will also look into the design implementation and performance issues related the above objectives.

1.5 Scope of Work

This project is aim to develop a new DWT system architecture based on objectives stated above. New algorithm development and entire image compression system development are out of the scope of this project. The simulation output will be compared against software modeling. Evaluation will be carried out in terms of resource utilization, latency, throughput and power efficiency. The design is intended for ASIC implementation, but this project is limited to architectural Proof of Concept (PoC) using Altera Quartus II software and targeting Stratix III FPGA family. The HDL design entry, logic synthesis, verification, timing analysis and power analysis will be done using tool suite provided by Altera Quartus II software.

1.6 Methodology

Data Flow Graph (DFG), Signal Flow Graph (SFG) and other high level design techniques are used for architectural development. Subsequently, Verilog HDL is used for design entry. The RTL design is simulated using Altera Quartus II software. The design is then synthesized into gate level netlist using the Altera Quartus II. After synthesis step, the netlist is fit into Stratix III device by converting the design to use the FPGA's logic element. Once the gate level design is ready, simulation is then performed using the actual gates and interconnects delays from a detailed timing model of the targeting device. The routed design is used for critical path delay analysis through the aid of Quartus II timing analysis tool.

1.7 Structure of Report

The report is organized into five chapters. The rest of the chapters are as follow.

Chapter 2 presents the fundamental of the wavelet theories. The wavelet transform concept is first introduced, followed by different computation approaches of DWT. Existing VLSI architectures for DWT will be reviewed in detail as well.

Chapter 3 presents a software model of the DWT implemented in fast lifting form in C++. It also discusses the architecture specification of the proposed

architecture, high level architecture overview and implementation details of DWT engine.

Chapter 4 presents the validation methodology and discussion of the performance analysis of the proposed architecture.

Finally, conclusion and future work are presented in Chapter 5.

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