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GATE LEAKAGE LOGIC DETECTION FOR ANALOG CMOS CIRCUIT

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3.1 INTRODUCTION

In micron technology node, Igate is not a big issue to circuit designer due to its negligible value. But in deep submicron technology node, Igate is one of the major and dominant leakage components. Igate is also reacts to process variation. As this issue arise, circuit designer need to aware the impact of Igate towards their design. In addition the ability to observe the Igate level is more desirable.

The variation in Igate is most sensitive to oxide thickness, TOX, due to their exponential relationship (Mukhopadhyay and Roy, 2003). It will rise by the factor of 4,000 from 90 nm to 50 nm node (Helms, Schmidt and Nebel, 2004). TOX tends to vary from one process corner to another, resulted in the variation in Igate. In digital circuit, Igate will contribute to increase off state power consumption. In contrast, for analog circuit, simple current mirror with large ratio will suffer on unexpected output current due to the leakage path from gate to ground.

Apart from the study on the impact of Igate toward circuit performance, there is insufficient discussion about the method to

detect Igate level in IC from testing perspective. Recent work shows that Igate for SRAM cell has been successfully monitored using specific hardware (Kanj et al., 2007). However it can only be used to that particular cell only. Another work use simple current mirror topology to detect Igate level in individual transistor (Chen and Huang, 2006). This method is difficult to implement in real circuit which contain more than one transistor.

In this work, a new detection method for Igate variation is presented which used I_{DDQ} test approach. Igate is detected at supply current node as Igtotal which represent the summation of all transistors' Igate in the circuit. From the simulation, it is shown that the detection method is capable of detecting Igtotal variation when it varies from the selected threshold.

3.2 CIRCUIT UNDER TEST IGATE STUDY

In order to investigate Igate current in the circuit under test (CUT), compact Igate model need to be included in the simulation. For that reason, BSIM4 model is used to model the transistors in the circuit. This work used 90 nm Predictive Technology Model (PTM) which had been modeled using BSIM4 format. As for circuit simulator, TSPICE is used throughout this work.

This work used I_{DDQ} test to sense the leakage level variation. Self biasing Vt reference bias current circuit has been chosen as a CUT and it is shown in Figure 3.1 (Allen and Holberg, 2002). The CUT is only conducting a DC current. The analysis on Igate variation in DC current is much easier compared to dynamic current. At first, the simple relationship of Igate and the CUT's I_{DDQ} is defined in Equation 3.1.

$$I_{DDQ} = I_{DDQ}' + Igtotal \tag{3.1}$$

I_{DDQ}' stands for the supply current without gate leakage and Igtotal

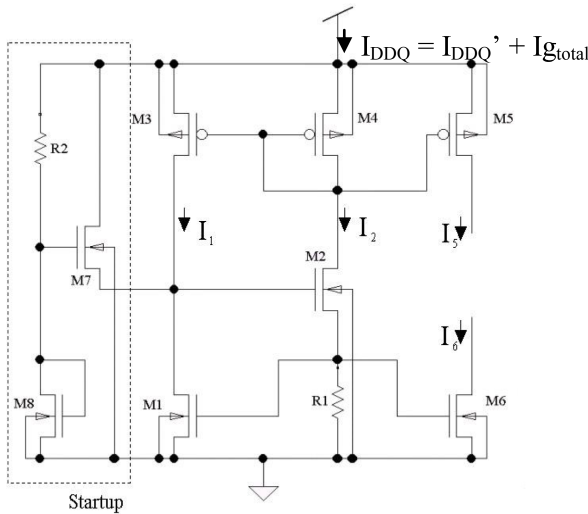


Figure 3.1 CUT.

is the total gate leakage from the transistors in the circuit. From circuit point of view it is more practical treating the gate leakage for this circuit as the summation of individual Igate in each transistor.

It is possible to observe Igtotal using PTM in TSPICE. The model for gate leakage can be switch on and off using two parameters in the PTM. The parameters are *IGCMOD* and *IGBMOD* that represent gate-to-channel and gate-to-bulk current respectively. When both parameters are set to 1, the gate leakage model is turned on meaning that the simulation will include gate leakage effect in it. In contrast, if these two parameters are set to 0, the simulation will neglect gate leakage impact on the simulation result. Therefore by controlling these two parameters, Equation 3.1 is used to observe Igtotal.

Since this work is interested on DC test only, DC operation point analysis is conducted in TSPICE. First, the simulation is done with the gate leakage model is set to on. Second, the same simulation is

repeated with the gate leakage model is set to off. In the first simulation, I_{DDQ} is observed at the V_{DD} node of the CUT. Similarly, I_{DDQ}' is observed at the similar node for the second simulation. The result of these two simulations is noted and the difference between these two results denotes Igtotal value. These two simulations are repeated at different temperature and process corners. The result of Igtotal variation is shown in Figure 3.2.

Figure 3.2 denotes that the variation of Igtotal across process corners is small. The graph is overlapping on each other which indicates that the value of Igtotal at specific temperature is similar. This is clearly shown at 27 °C to 60 °C. At other temperatures, the variation is small about 1nA to 2 nA from the typical Igtotal. So it is safe to assume that Igtotal is insensitive to process corner. However this assumption is valid to the PTM process only. Different processes may require different technique to model their transistor.

The reason that Igtotal is insensitive to process corner relies on the corner model itself. Igate is a function of transistor size, oxide thickness, TOX, gate-to-source, VGS, gate-to-drain, VDS and supply current (Dongwoo et al., 2003). However TOX is the most influential parameter that affects Igate variation. The variation of TOX in PTM corner model is neglected. This is why at all the

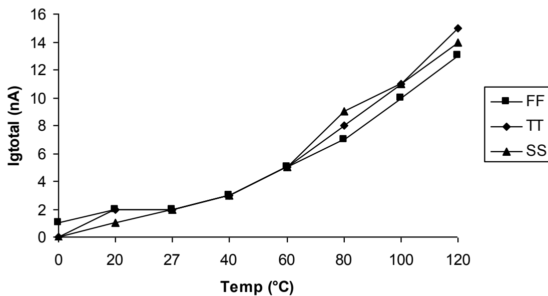


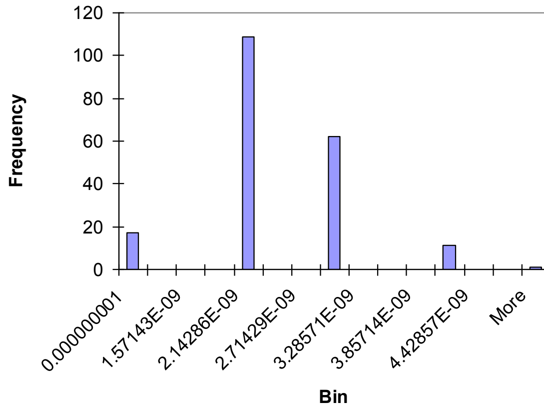
Figure 3.2 Igtotal variation.

process corners, the value of Igtotal is almost similar.

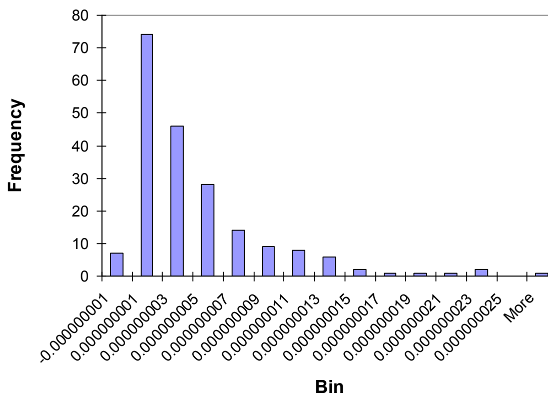
It is essential to investigate Igtotal variation due to TOX variation because the huge impact that it bring toward Igate. Typical PTM model is modified to include TOX variation in it. The TOX is modeled using normal distribution. At first the 3σ value for this distribution is set to 4% followed by 20%. The 4% variation corresponds to the maximum allowable variation in TOX for 90 nm technology node as stated in the ITRS, 2004. However in reality, to obtain at most 4% variation in TOX is difficult. So the 20% variation in TOX is also considered because it reflects a realistic variation in processes (Mukhopadhyay and Roy, 2003).

At every 3σ value considered above, DC operation point Monte Carlo analysis with 200 iterations is conducted. The simulation temperature is set to 27 °C. The Igtotal distribution for 4% and 20% variation in TOX is shown in Figure 3.3a and 3b respectively.

Figure 3.3, shows the distribution of Igtotal. For Figure 3.3a, the mean for Igtotal is 2.35 nA with 0.735 nA standard deviation. In contrast, for Figure 3.3b, the mean is 3.77nA while the standard deviation is 4.66n. The largest Igtotal obtained in this simulation was 4 nA and 24 nA for 4% and 20% variation of TOX respectively. It is shown that the distribution of Igtotal forms a normal distribution. However the left side of the graph is not even as the right side. This normal distribution graph is known as skewed right normal distribution. The skewed graph indicates that the actual Igtotal data obtained from this simulation might not form a perfect normal distribution but it has been assumed normal distributed by data analysis program. As for a comparison, the Igtotal distribution obtained in this work has similar shape with the work by Kanj et al. (2007). This similar relationship can be investigated further for future Igtotal analysis.



(a)



(b)

Figure 3.3 Igtotal distribution for TOX variation. (a) 4% variation. (b) 20% variation.

From the discussion above, a current extractor circuit that determines the total current from the CUT is needed. An extractor circuit is proposed and described in the next section.

3.3 BUILT IN CURRENT EXTRACTOR CIRCUIT

Process variation in IC fabrication process may lead to the deviation of circuit performance either in digital or analog circuit. This is becoming worst by the scaling of channel length to smaller process. As a result, there is a growing need to observe the impact of the process variation using appropriate test procedure so that fabricated chips can be well characterized. One of the simplest test procedures is by using dc test which is the supply current monitoring or simply called I_{DDQ} test.

There is internal and external I_{DDQ} test (Kim and Beom, 2006). Internal I_{DDQ} test needs an extra circuit incorporated with the desired circuit to be tested. Such circuit is called built-in current sensor (BICS). The advantages of using BICS are it can reduce the testing cost and time beside improved fault detection. A lot of designs for BICS have been proposed by researches. Current comparator concept with positive feedback was implemented in the BICS to monitor I_{DDQ} current (Kim and Beom, 2006). However, this type of design is very susceptible to process variation since it uses internal current generator. Robust BICS based on ratiometric of current and multiple sensing stages was presented for radio frequency (RF) circuit (Cimino et al., 2006) and mixed signal application (Liobe and Margala, 2007). These sensors are more robust to temperature and process variation.

What can be seen in all of these designs is the BICS contains two types of circuits. The first circuit is the current extraction circuit while the second circuit is the sensing element. The extraction circuit should be carefully designed so that the sensing element works well. In this work, a simple built-in current extractor (BICE) circuit is presented that able to extract I_{DDQ} current from analog circuit under test. In addition, this BICE is process and temperature independent. Moreover, it is not only able to extract the I_{DDQ} current but can be extended to detect other current as well. This will be beneficial for testing the internal node of the circuit which

the accuracy of its current is very critical to the overall performance of the circuit.

Figure 3.4 shows the proposed BICE circuit. The architecture is realized by an opamp, digital inverter, four PMOS and one NMOS transistors. Only one input pin is needed to trigger the BICE operation compared to the design by Kim and Beom, 2006 which requires two input pins. The output pin is not included in the design since BICE is a portion of BICS circuit that lack of sensing element. However the node Vsen in the circuit can easily be used as sensing node for the sensing element since it reflects the I_{DDQ} level in the CUT. This will be proved later in the next section.

There are two modes that support the operation of the BICE circuit. In the off mode, the test pin is tied to supply voltage, Vdd which indicates logic 1. In this mode BICE circuit is working in off state meaning that it will not extract any current from CUT. Drain current, I_{DDQ} will flow through transistor M_1 and enter the CUT. In addition no current will flow through the extraction circuit part since transistor M_2 is off which is essential for saving power during

Figure 3.4 Proposed BICE circuit.

normal CUT operation. During the test mode, I_{DDQ} will flow through transistor M_2. Transistor M_1 and M2 are designed so that their size are similar. Since the size is similar, their drain current will be equal. Therefore at both modes similar I_{DDQ} will enter the CUT. In order to function in the test mode, the test pin should be tied to ground which reflect logic 0. The I_{DDQ} level will be mirrored to the extraction circuit consist of transistor M_3, M_4 and M_5.

In order to efficiently copy I_{DDQ} from M_2 to M_3, both transistors should be identical in size and biasing meaning that their gate-to-source voltage, V_{GS} and drain-to-source voltage, V_{DS} are similar. To achieve this, an opamp functioning in negative feedback is needed. The negative feedback opamp will track the drain voltage of both transistors and produces the different at its output. This voltage different will be used as correction factor to sink more or less current from supply voltage by controlling M_4 gate so that at the end of the feedback their drain current will be equal. Their gate and source terminal are physically connected so the required biasing condition for M_2 and M_3 is achieved. The operation of BICE is summarized in Table 3.1 which neglected subtreshold leakage when the transistor is off.

The opamp is designed based on two stage opamp. The speed of the BICE operation depends on the speed of this opamp. The faster it operates, the sooner the result can be observed. However, in this study, the design is not aim for the speed of the opamp because the overall design of BICE is not optimized for speed. There is no

Table 3.1 BICE operation

Test input (Logic)	**BICE Mode**	**IM_1 (µA)**	**IM_2 (µA)**	**IM_3 (µA)**
0	Test	0	I_{DDQ}	I_{DDQ}
1	Off	I_{DDQ}	0	0

specific target in term of testing time of the CUT. So, if faster test time is desired, one can just simply redesign the opamp and optimized it for speed. Figure 3.5 shows the transistor level of the opamp. The design is optimized so that it consumed less power. Therefore subtreshold current is used to bias the opamp. The compensation of the opamp must be made well so that no oscillation will occur. The compensation capacitor (Cc) shown in Figure 3.5 is selected so that the phase margin for the opamp is above 60°.

This BICE is only interested in extracting dc current from analog circuit. In this work, smaller circuit such as biasing circuit has been chosen as the CUT. The CUT block in Figure 3.4 is a self biasing Vt reference bias current circuit as shown in Figure 3.1. The proposed BICE can be implemented in other type of analog circuits with minimal modification if appropriate.

3.3.1 SIMULATION RESULTS FOR THE BICE

The proposed BICE is simulated in TSPICE. A 90 nm PTM is used in this simulation to model the transistor. The DC operating point

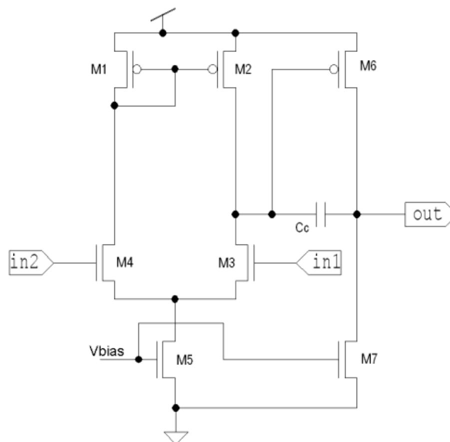


Figure 3.5 Opamp circuit.

analysis is conducted at different temperatures and process corners. Logic 0 is supplied to the test pin during the simulation. This will trigger BICE to function in the test mode so that extraction current can be observed as well as the percentage of extraction error and Vsen value. The simulation result is summarized in Table 3.2.

Table 3.2 indicates that in all process corners and temperatures the extraction error is still less than 1%. What is meant by error is the different between the extracted current that flow in transistor M_5 and the actual I_{DDQ} current that flow in the transistor M_2 as shown in Figure 3.4 during the test mode. The error percentage shows that how efficient the BICE copy the I_{DDQ} that flow into the CUT through M_2. Smaller extraction error shows that the copied current is closer to the actual I_{DDQ}. This BICE is insensitive to process and temperature variation because no matter at what temperature and corners, it is still able to copy the I_{DDQ} current even though the I_{DDQ} current change across different temperatures and corners. The highest extraction error recorded in the simulation is when the temperature is 120 °C in SS corner. In this condition the error is 0.2% which is still very small.

The extraction time is investigated by transient simulation conducted in TSPICE. The extraction time is defined as the period of time when BICE change its initial current to track the changes in I_{DDQ} current until it achieved steady state. This simulation is conducted in room temperature (27 °C) using the typical corner model. Figure 3.6 shows the BICE transient simulation.

In Figure 3.6, when I_{DDQ} change for the first time at 1µs, the extraction current tries to follow it. However it only succeeds in tracking the I_{DDQ} current only after 30µs. At 50µs, I_{DDQ} change from 22.1µA to 18.5µA. Only at 80µs, the BICE is in the steady state which shows the correct extraction current. In short, the extraction time for the BICE is 30 µs. To obtain faster extraction time, faster opamp should be designed.

Table 3.2 DC operating point simulation result

Temperature (°C)	Process	I_{DDQ}/IM_2 (μA)	Error (%)	Vsen (V)
0	FF	22.990	0.165	0.2407
	TT	23.707	0.051	0.2743
	SS	24.345	0.049	0.3041
20	FF	22.259	0.135	0.2334
	TT	23.001	0.022	0.2679
	SS	23.660	0.059	0.2984
27	FF	22.017	0.127	0.2308
	TT	22.769	0.018	0.2656
	SS	23.438	0.068	0.2963
40	FF	21.587	0.116	0.2259
	TT	22.363	0.004	0.2612
	SS	23.048	0.074	0.2923
60	FF	20.977	0.105	0.2182
	TT	21.795	0.014	0.2542
	SS	22.502	0.084	0.2859
80	FF	20.428	0.108	0.2104
	TT	21.294	0.002	0.2471
	SS	22.008	0.100	0.2794
100	FF	19.941	0.110	0.2025
	TT	20.856	0.050	0.2400
	SS	21.538	0.121	0.2726
120	FF	19.514	0.087	0.1945
	TT	20.474	0.103	0.2327
	SS	21.021	0.190	0.2654

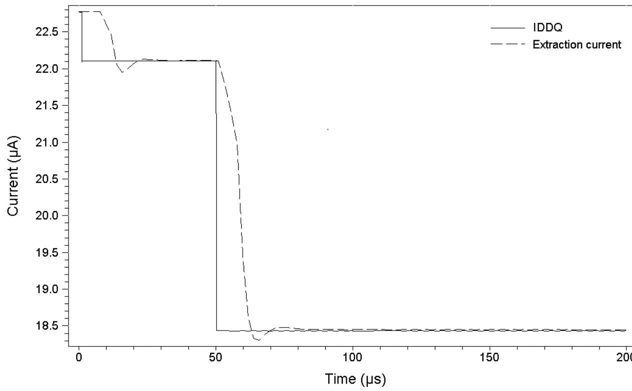


Figure 3.6 BICE transient simulation.

As has been mentioned earlier, the value of Vsen can be used as sensing node for sensing circuit. However this earlier prediction must be proved whether it is true or not. Figure 3.7 shows the relationship between I_{DDQ} and Vsen using the data presented in Table 3.2. The relationship is linear. As I_{DDQ} increases Vsen will also increase. From this result, Vsen can easily be mapped to I_{DDQ} value so that the value of I_{DDQ} can easily be observed just by monitoring Vsen. Depends on the testing strategy either current or voltage sensor can be implemented to sense the variation of Vsen which reflects the I_{DDQ} level.

By looking at the simulation results, this BICE can extract the I_{DDQ} from CUT. This extracted current can be used for testing purpose such as leakage and fault detection test. Further work can be done to investigate whether the BICE circuit can be implemented in smaller technology which is a challenging task due to smaller supply current is used.

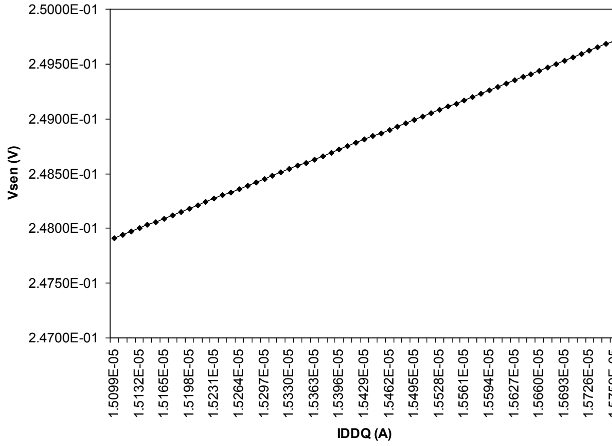


Figure 3.7 Vsen and I_{DDQ} relationship.

3.4 PROPOSED DIGITAL DETECTION METHODOLOGY

The method to detect Igate variation is described in Figure 3.8. First, the I_{DDQ} is extracted from the CUT. Then current comparator is used to implement Equation 3.1 to obtain Igtotal value from the CUT. The Igtotal is converted to voltage using I-V converter and finally the voltage is sense using 1 bit analog-to-digital (ADC) converter.

The CUT's I_{DDQ} is extracted using BICE as discussed in the previous section. One might notice that the actual voltage that supplies the current to the CUT is not actually V_{DD} due to the

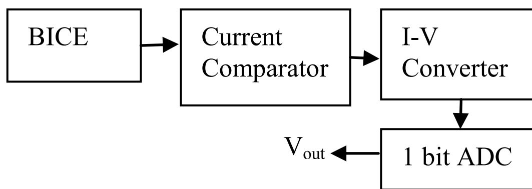


Figure 3.8 Igtotal detection method.

voltage drop across M_1 and M_2. However the voltage drop across M_1 and M_2 can be made as small as possible so that the voltage drop across the CUT is close to V_{DD}. The design of BICE is made so that it will not interfere with the normal operation of the CUT.

The current comparator and I-V converter circuit is shown in Figure 3.9. It is designed based on Kirchoff's Current Law at node N2. The subtraction equation for this circuit is,

$$I_{M7} = kI_{DDQ} - Iref \quad (3.2)$$

which $Iref = I_{DDQ}' = 22.8\ \mu A$ and

$$k = \left[1 + \left(V_{DSM6} - V_{DSM5}\right)\lambda\right] \quad (3.3)$$

The result of the current comparator is not exactly Igtotal due to the present of *k* in Equation 3.2. This is understandable because the simple current mirror topology is used in the current comparator circuit, which suffers from channel length modulation effect.

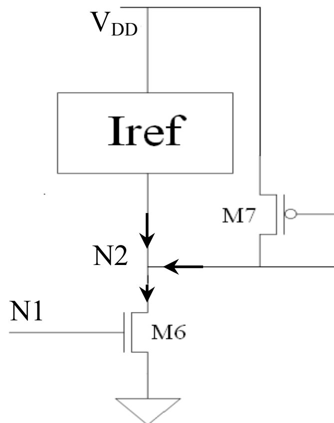


Figure 3.9 Current Comparator with I-V converter.

Although the result of the subtraction operation is not exactly equal to Igtotal, it does not affect much to the overall Igtotal detection scheme. Instead of using I_{M7} to detect Igtotal, the N2 node is use as detection node. The voltage at N2 node is the result of I-V conversion from the current comparator circuit.

The relationship between Igtotal and V_{N2} is described in Equation 3.4.

$$V_{N2} = \frac{\text{Igtotal}\,(m+n)}{p} + \frac{I_{M7}}{p} + V_{N1} \tag{3.4}$$

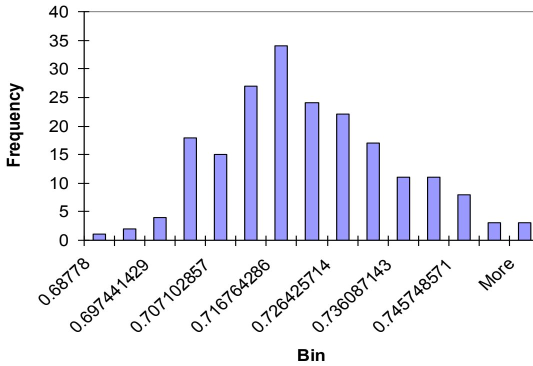
In Equation 3.4, *m*, *n* and *p* are constant. The purpose of Equation 3.4 is to show that V_{N2} has linear relationship with Igtotal. It is not meant to actually model the Igtotal accurately because Equation 3.4 is obtained by simple linear regression.

The 1 bit simple ADC is design to sense the voltage of V_{N2}. If V_{N2} exceed a certain threshold, which reflect the maximum tolerable Igtotal, the output of this 1 bit ADC is logic 1. On the other hand, it will output logic 0 if Igtotal is within accepted range.

3.5 SIMULATION RESULT AND DISCUSSION

The simulation approach is similar to the approach in section 3.2. The DC operating point Monte Carlo simulation with 200 iterations is conducted. The result of V_{N2} distribution is shown in Figure 3.10.

In Figure 3.10, the distribution of V_{N2} is almost similar to the distribution of Igtotal shown in Figure 3.3. Using mapping method the Igtotal variation is map to V_{N2} variation. Therefore by sensing V_{N2} it will reflect the Igtotal variation.



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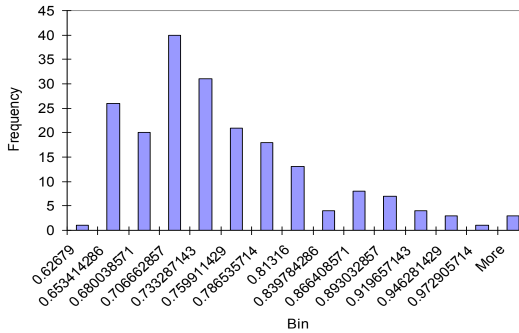
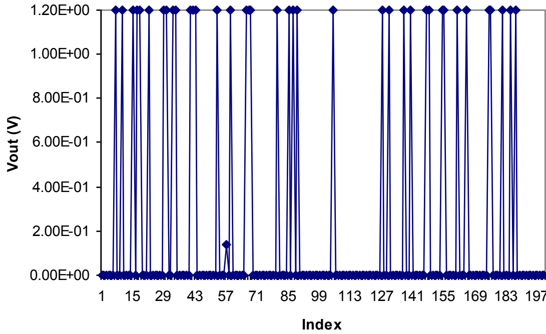


(b)

Figure 3.10 VN2 distribution. (a) 4% variation. (b) 20% variation.

The result of digital detection is obtained directly from the 1 bit ADC output, which is shown in Figure 3.11 with its corresponding Igtotal value. The X-axis denotes the Monte Carlo iteration points. The threshold for minimum detectable Igtotal is shown in horizontal line in Figure 3.11(b), which is at 7 nA. So if Igtotal is above 7 nA, the 1 bit ADC output, V_{out} will output logic 1 which indicates unacceptable Igtotal level. In contrast, if Igtotal is below 7 nA, the output will be logic 0 which mean the Igtotal is still within accepted level.



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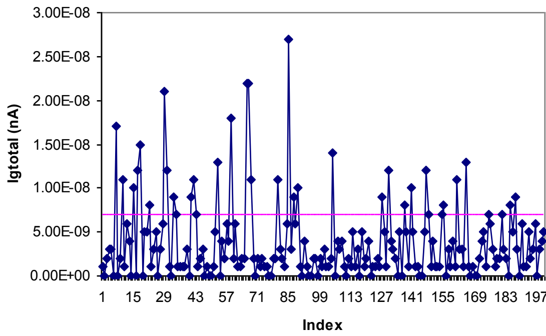

(b)

Figure 3.11 (a) Vout. (b) Igtotal.

3.6 CONCLUSION

In this work, a method to detect Igate variation is proposed. The detection is based on I_{DDQ} monitoring. The I_{DDQ} value is extracted from the CUT using a proposed BICE circuit. The BICE circuit will copy I_{DDQ} current and pass it to the sensing element for I_{DDQ} test. This circuit use negative feedback to stabilize the copied I_{DDQ}. One extra pin is used to trigger the operation mode. The operations are off mode and test mode which at both of this modes the operation of the CUT is not interrupted. In the off mode, the remaining BICE circuit is switch off to reduce power consumption.

This BICE can be used with sensing circuit to construct BIST circuit which suitable to use in online testing. Later, Igtotal is monitored which reflects the summation of individual Igate in every transistor in the CUT. The variation in Igtotal is mapped to other node as voltage and this voltage level is sense by 1 bit ADC. The simulation result shows that if Igtotal exceed the required threshold, the detection output V_{out} is set to logic 1. The output is logic 0 if Igtotal is below the threshold value.

REFERENCES

Allen, P. E. and D. R. Holberg. (2002). *CMOS Analog Circuit Design*. 2nd ed.: Oxford University Press, Inc.

Chen and H. Huang. (2006). CMOS leakage current meter. *U.S. Patent 20060012391A1*.

Cimino, M. et al. (2006). A robust 130 nm-CMOS built-in current sensor dedicated to RF applications. *Proc. Eleventh IEEE European Test Symp*. :151-158.

Dongwoo, L. et al. (2003). Simultaneous subtreshold and gate-oxide tunneling leakage current analysis in nanometer cmos design. *Proc* 4*th Int. Symp. on Quality Electronic Design*. :287–292.

Helms, D., E. Schmidt and W. Nebel. (2004). Leakage in CMOS circuits – an introduction. *Proc. 14th Int. Workshop on Power and Timing Modeling, Optimization and Simulation*. :17–35.

Kanj, R. et al. (2007). Gate leakage effects on yield and design considerations of PD/SOI SRAM designs. *Proc. 8th Int. Symp. on Quality Electronic Design*. :33–40.

Kim and J. Beom. (2006). Novel current sensing circuit for IDDQ test. *Proc. Thirtieth Int. Conf. on Electronics, Circuits, and Systems*. :375-378.

Liobe, J. and M. Margala. (2007). Novel process and temperature-stable BICS for embedded analog and mixed-signal test.

Proc. Thirtieth IEEE Int. On-Line Testing Symp. :231-236.

Mukhopadhyay, S. and K. Roy. (2003). Modeling and estimation of total leakage current in nano-scaled-CMOS devices considering the effect of parameter variation. *Proc. Int. Symp. on Low Power Electronics and Design.* :172–175.

Nanoscale Integration and Modeling Group (NIMO), 1 January 2007. Predictive Technology Model URL http://www.eas.asu.edu/~ptm/.

The International Technology Roadmap for Semiconductors 2004 (ITRS), Available: http://public.itrs.net/.