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A 2.4 GHZ CMOS TUNABLE IMAGE- REJECTION LOW-NOISE AMPLIFIER WITH ACTIVE INDUCTOR

Ler Chun Lee
Abu Khari A'ain
Albert Victor Kordesch

2.1 INTRODUCTION

Research and development in radio-frequency integrated circuits (RFICs) have become popular recently and this is due mainly to the high demand for wireless communication devices from the market. Among the various integrated circuits fabrication technologies in use, CMOS technology has become a very attractive option because of its low-cost and high integration.

Superheterodyne receiver is at present the most widely used receiver front-end architecture as it exhibits good RF performance. Proper image signal filtering is required and this is done through using external surface-acoustic wave (SAW) filters. However, this results in increased cost and device size (Maeda et al., 2006). To overcome the problem, recent research has focused on image-rejection low-noise amplifier (IR LNA) that uses a notch filter to reject the image signal (Samavati, Rategh and Lee, 2005; Baki and El-Gamal, 2002; Nguyen et al., 2005).

This chapter presents a 2.4-GHz CMOS IR LNA, as shown in

Figure 2.1. The IR notch filter was designed using only active inductor (without any passive inductor).

Unlike spiral inductor, active inductor has smaller die area, larger inductance, higher quality factor (Q) and inductance or Q tuning ability. The Q of the spiral inductor is usually low, this being due to wiring and substrate loss (Thanachayanont, 2002). Unfortunately, active inductor has poor noise performance, poor linearity and also higher power consumption compared to spiral inductor.

The proposed notch filter in IR LNA was designed using active inductor which has an equivalent inductance of 28 nH and $Q = 400$ at 1.34 GHz. Obviously spiral inductors cannot possibly achieve inductance and Q mentioned above at 1.34 GHz. However, with proper design, this paper demonstrates that the performance of the IR LNA designed using active inductor is comparable to that of IR LNA designed using spiral inductor.

This chapter is organized as follows: Section 3.2 introduces the concept and design of the active inductor, Section 3.3 discusses the design of the IR LNA circuit with simulation result presented in Section 3.4. Finally, Section 3.5 concludes the chapter.

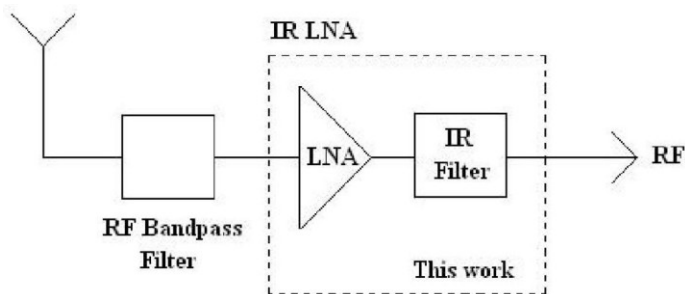


Figure 2.1 Typical superheterodyne receiver front-end.

2.2 DESIGN OF ACTIVE INDUCTOR

Active inductor can be designed using gyrator topology as shown in Figure 2.2. Parameters g_1 , C_1 , g_2 and C_2 are the parasitic conductors and capacitance at node N1 and node N2 respectively. The input impedance, Z_{in} of the gyrator circuit is calculated as follows:

$$Y_{in} = \frac{1}{Z_{in}} = g_1 + s C_1 + \frac{G_{m1} G_{m2}}{s C_2 + g_2} \quad (2.1)$$

where G_{m1} and G_{m2} are the effective transconductance of the gyrator circuit.

The active inductor proposed in (Xiao et al., 2004) was used in this design but with some modifications. It is able to tune inductance and Q almost orthogonally.

Figure 2.3 shows the circuit design for active inductor used in this chapter. M1 and M2 are used to form the G_{m1} in Figure 2.2. According to (Xiao et al., 2004), if $g_{m1} \approx g_{m2} \gg g_3$,

$$G_{m1}(s) \approx \frac{0.5g_{m1}}{1 + s(C_{gs1} + C_3)/(g_{m1} + g_{m2} + g_3)} \quad (2.2)$$

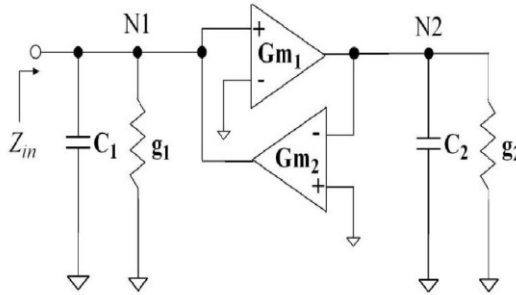


Figure 2.2 Gyrator topology.

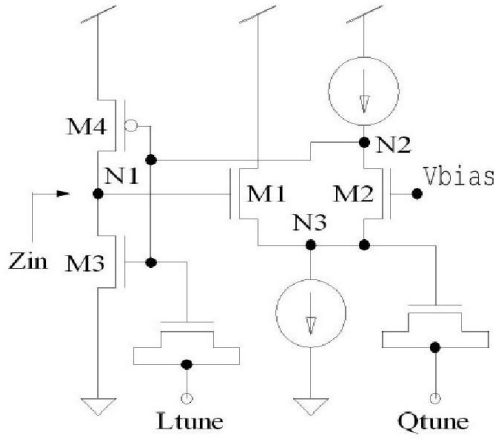


Figure 2.3 Simplified circuit diagram of the active inductor used in this design.

where g_3 and C_3 are the parasitic conductance and capacitance respectively at node N3. However, different from the active inductor proposed in (Xiao et al., 2004), $-G_{m2}$ of the active inductor in this paper is designed using inverter circuit formed by M3 and M4, where

$$-G_{m2} \approx -(g_{m3} + g_{m4}). \quad (2.3)$$

Parameter $-G_{m2}$ designed using an inverter has a higher G_m compared to $-G_{m2}$ designed using conventional common-source amplifier at the same power consumption and biasing condition.

The input impedance, Z_{in} , in Figure 2.3, can be calculated from Equations 2.1 – 2.3,

$$Z_{in} = C_1 \parallel g_1 \parallel \frac{sC_2 + g_2}{G_{m1}G_{m2}}$$

$$\approx C_1 \parallel g_1 \parallel \left(s C_2 + \left(g_2 - \frac{\omega^2 C_2 (C_{gs1} + C_3)}{g_{m1} + g_{m2} + g_3} \right) \right) \parallel 0.5 g_{m1} (g_{m3} + g_{m4}) \quad (2.4)$$

From Equation 2.4, the inductance can be tuned by varying C_2 while the Q of the active inductor can be tuned by varying C_3 . Hence two varactors are added at node N2 and node N3 for inductance and Q tuning purposes. Inductance and Q tuning can be done by varying the voltage at Ltune and Qtune nodes, respectively, as shown in Figure 2.3.

2.3 IR LNA CIRCUIT DESIGN

A notch filter used in IR LNA designed using active inductor had been demonstrated in (Sharaf, 2000). The notch filter was placed at the output port of the LNA. However, no notch frequency tuning using active inductor is shown in the previous literature. Since notch filter can only reject the image signal at a very narrow frequency, a tunable notch frequency for IR LNA is unavoidable.

Figure 2.4 shows the cascode LNA with the third-order passive notch filter introduced in (Samavati, Rategh and Lee, 2005). The filter has low impedance at the image signal frequency and high impedance at the wanted signal frequency. The varactor, C_l is used to tune the notch frequency of the IR notch filter. Due to the low Q of the spiral inductor, the cross-connected differential pair transistors were used to generate negative resistance to compensate the losses in the filter. Since the incoming signal had been amplified by transistor M1, the noise contributed from notch filter becomes less significant.

Figure 2.5 shows the simplified circuit diagram of the proposed IR LNA. The inductor in the IR notch filter can be replaced by active inductor as in Figure 2.3. Since the notch frequency of the IR notch filter can be tuned by active inductor, the varactor in Figure 2.4 can

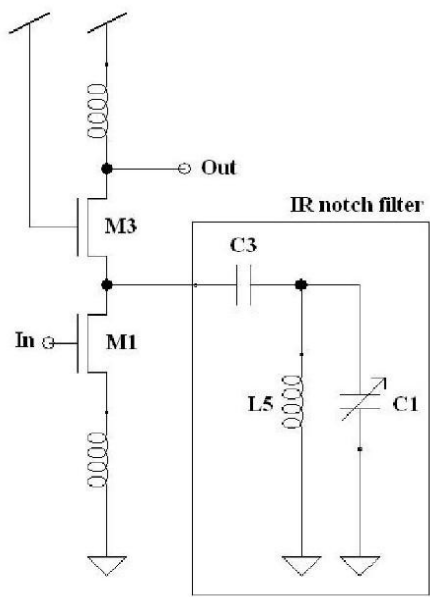


Figure 2.4 Simplified IR LNA with a third-order filter circuit diagram.

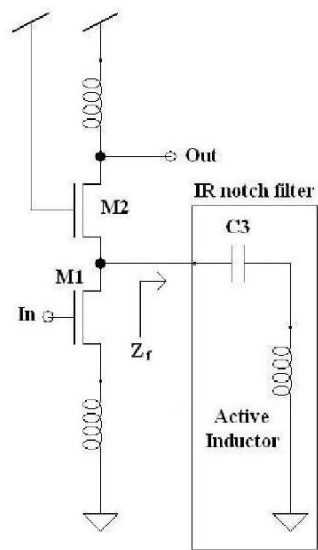


Figure 2.5 Proposed IR LNA circuit diagram.

be eliminated. Furthermore, active inductor usually has higher Q compared to spiral inductor, thus eliminating the need for active compensation circuits that are usually noisy and dissipate more power. The input impedance of the IR notch filter, Z_f can be calculated as follows,

$$Z_f = \frac{s^2 L_{active} C_3 + 1}{s C_3} \quad (2.5)$$

where L_{active} is the inductance of the active inductor. The image signals are located at

$$\omega_{image} = \pm \frac{1}{\sqrt{L_{active} C_3}} \quad (2.6)$$

The complete circuit of the IR LNA is shown in Figure 2.6. Components L_g , L_s , g_{m1} , C_{gs1} and C_{ex} in Figure 2.6 provide 50 Ω input matching at 2.4 GHz. The LC tanks (L_o and C_o , L_{out} and C_{out}) provide a DC bias current path and resonance at the desired frequency. The second-stage common-source amplifier is added for measurement purpose only.

2.4 SIMULATION RESULTS

The IR LNA is implemented with Silterra's 0.18 μm one poly and six metal layers standard CMOS process. The thick top metal was used for spiral inductors to increase Q . The spiral inductors are designed and simulated using OEA SPIRAL, as shown in Table 2.1. The complete layout of the IR LNA is shown in Figure 2.7. Spiral inductors still occupied most of the die area. However our work successfully reduced the usage of the spiral inductors from five to four, without degrading the performance of the IR LNA too much.

Table 2.1 shows the inductance and Q of the spiral inductors used

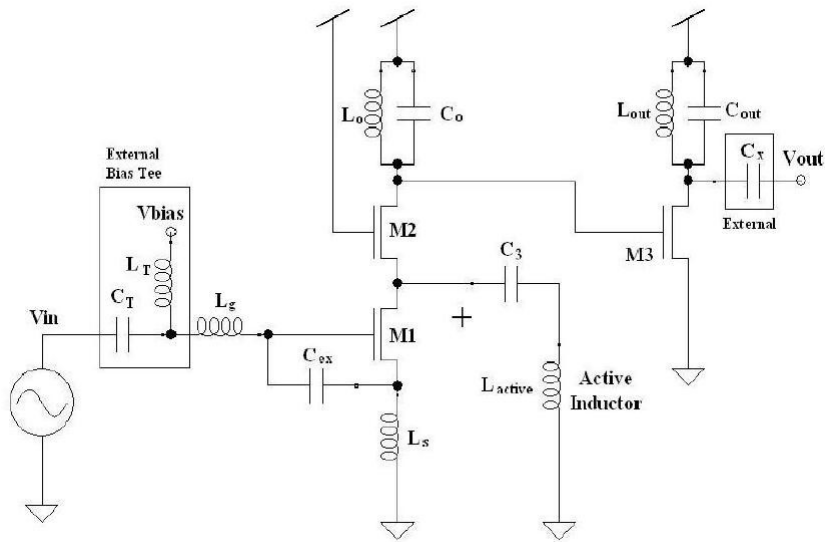


Figure 2.6 Complete proposed IR LNA design circuit.

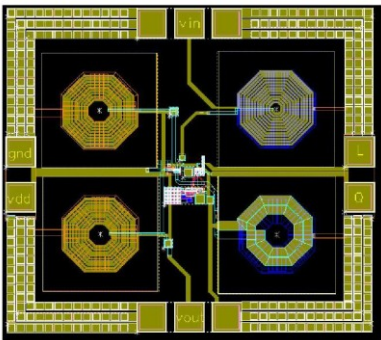


Figure 2.7 Complete layout of the proposed IR LNA circuit.

Table 2.1 Simulated spiral inductor performance at 2.4 GHz

Spiral inductor	Inductance (nH)	Q
L_g	13	7
L_s	0.7	8
L_o, L_{out}	10	7

in this design. As mentioned above, the active inductor used in the IR notch filter has inductance of 28 nH and $Q \approx 400$ at the image frequency. All the capacitors in Figure 2.6 were implemented using metal-insulator-metal (MIM) capacitor. Capacitance of the C_o , C_{out} , C_{ex} , and C_3 at 2.4 GHz is 0.34 pF, 0.34 pF, 0.125 pF and 0.5 pF, respectively.

The IR LNA was simulated using HSPICE with Silterra's BSIM 3v3 MOSFET model. The post layout simulations of the IR LNA are summarized in Table 2.2. S11 and S21 of the IR LNA are plotted and shown in Figure 2.8. It shows that the notch frequency is located at 1.34 GHz with IR of -28 dB. Figure 2.9 shows notch frequency tuning using active inductor.

2.5 CONCLUSION

This chapter demonstrates the possibility of using active inductors in CMOS IR LNA design. The proposed IR LNA achieves low noise figure, high gain, high IR and 330 MHz tuning range for IR while dissipating not more than 10 mW for first-stage LNA. The

Table 2.2 Summary of the simulated IR LNA performances

Parameters	Proposed IR LNA
Operating frequency	2.4 GHz
Image frequency	1.34 GHz
Die area (excluding GSG pads)	0.49 mm ²
S11/S21	-23.5 dB/27 dB
NF	2.2 dB
Input 1 dB compression point	-26 dBm
IR	-28 dB
IR notch filter tuning range	1.08 to 1.41 GHz
Power dissipation: All IR LNA First stage IR LNA only	20 mW 10 mW

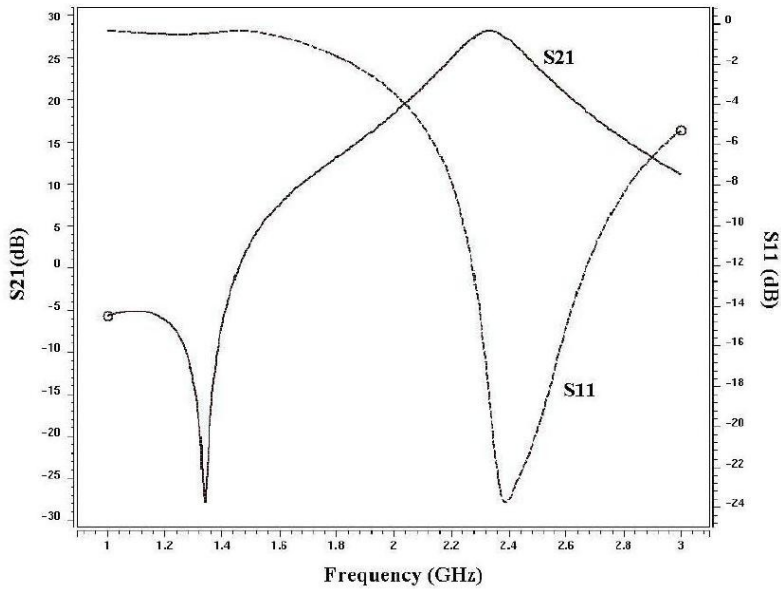


Figure 2.8 S11 and S21 of the proposed IR LNA.

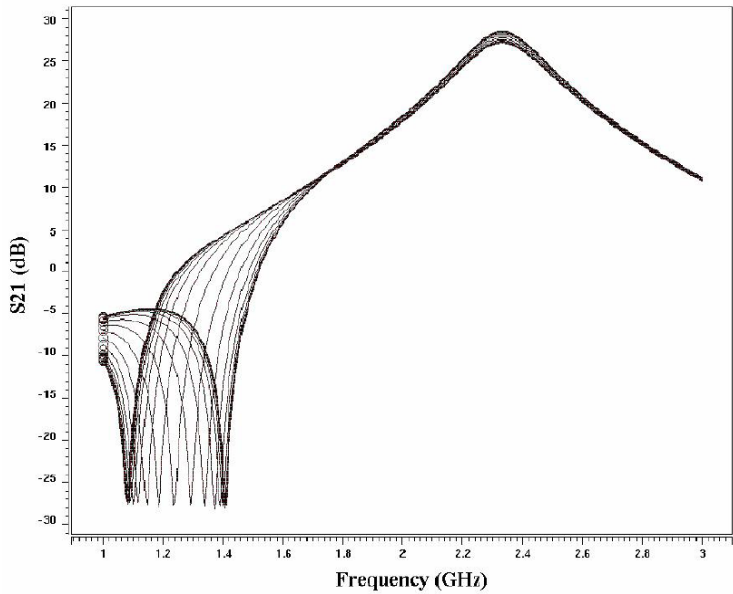


Figure 2.9 Notch frequency tuning using active inductor.

proposed IR notch filter used a much smaller die area compared to previous designs since it eliminates the use of one spiral inductor and a large varactor in the the IR notch filter design.

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