

UNIVERSITI TEKNOLOGI MALAYSIA

**BORANG PENGESAHAN
LAPORAN AKHIR PENYELIDIKAN**

TAJUK PROJEK : AUTOMATIC SEARCH FOR BREAK POINTS IN PRINTED CIRCUIT
BOARD USING INTELLIGENT VISUAL SYSTEM BASED ON DSP
ALGORITHMS

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Abstract

One of the key components in the electronics industries is the production of the printed circuit board (PCB). Since the existing technology is going towards full digital implementation, it is envisioned that the manufacturing of PCB will ever growing. In conjunction with this development, Malaysia has taken an important step. Currently there are 37-listed PCB manufacturing companies nation-wide.

As important as producing the PCB is to produce a zero-defect PCB. This is to ensure a high quality PCB that translates to reliable and quality digital end products. Initially, the bare PCBs (PCB without components attached to it) were inspected randomly using manual inspection system, which involves human operators. This technique is quite costly since it is highly error-prone due to human error. A more sophisticated way of doing the inspection is the use of in-house circuit testing (ICT) technique. This technique uses a very expensive machine that checks the conductivity of the PCB using probes. However, the limitation of this technique is it can only detect defects that are based on either shorts or open.

The objective of this project thus is to provide an alternative inexpensive and comprehensive defect detection technique. The basic technique of the proposed technique is to detect the defect based on the digital image of the PCB using image processing techniques. Defect detection using image processing itself is not a new field as it has been applied in the industries. However, what makes this proposed project a novel one is the implementation of wavelet transform that has assisted in detecting as many as 14 defects that could occur on the PCB.

This project has successfully implemented this wavelet-based defect detection and has successfully detected 100% defects on synthetic PCB images and more than 95% accuracy using real PCB images. This project was exhibited in the Expo Science and Technology 2002 in Kuala Lumpur and has won a bronze medal.

Abstrak

Salah satu komponen penting didalam industri elektronik ialah menghasilkan papan cetak litar "*printed circuit board (PCB)*". Memandangkan teknologi kini yang menghalak kearah dunia digital sepenuhnya, maka penghasilan PCB ini diramalkan akan bertambah dengan lebih pesatnya. Untuk ini, negara Malaysia telah mengorak langkah yang tepat dalam pertumbuhan bidang ini. Buat masa ini, terdapat 37 syarikat berdaftar PCB diseluruh negara.

Seperkara yang penting juga didalam penghasilan PCB ialah menghasilkan PCB ralat-sifar. Ini adalah bertujuan untuk memastikan mutu PCB yang dihasilkan bermutu tinggi supaya hasil produk yang dikeluarkan juga bermutu tinggi dan bolehharap. Di peringkat awalnya PCB kosong (PCB tanpa komponen) diperiksa secara rawak dengan menggunakan kaedah manual, iaitu menggunakan tenaga manusia. Teknik ini agak mahal memandangkan boleh berlakunya kesilapan agak tinggi disebabkan oleh faktor manusia. Satu kaedah yang agak canggih ialah menggunakan kaedah ujian litar dalaman "*in-house circuit testing*" (ICT). Kaedah ini memerlukan peralatan yang mahal yang akan memeriksa pengaliran arus didalam PCB menggunakan prob. walaupun bagaimanapun terdapat limit didalam kaedah ini kerana ujiannya adalah terbatas kepada mengesan litar buka atau litar pintas sahaja.

Dengan permasalahan diatas, projek ini bermatlamat untuk menyediakan satu kaedah alternatif yang murah dan menyeluruh didalam mengesan kerosakan PCB. Teknik asas yang di cadangkan ini menggunakan kaedah pemprosesan imej. Kaedah pemprosesan imej pada PCB ini walaupun bagaimanapun bukanlah satu kaedah yang baru. Kelainan didalam kaedah yang diutarakan ini adalah didalam penggunaan jelmaan wavelet yang dapat membantu mengesan sebanyak 14 kerosakan pada PCB.

Projek ini telah berjaya melaksanakan pengesanan kerosakan pada PCB dengan menggunakan kaedah jelmaan wavelet dengan ketepatan 100% untuk imej PCB buatan dan lebih 95% untuk imej PCB asli. Projek ini telah memenangi pingat gangsa didalam expo sains dan teknologi 2002 di Kuala Lumpur.

Table of Contents

Acknowledgement	ii
Abstract	iii
Abstrak	iv
Table of Contents	v
List of Figures	viii
CHAPTER 1: INTRODUCTION (7 Pages)	
1.1 Project Background	1
1.1.1 PCB Fabrication Process: An Outline	1
1.1.2 Inspection	2
1.1.3 Defects	3
1.2 Motivations	3
1.3 Objectives	5
1.4 Scopes of Work	5
1.5 Organization of the Report	7
CHAPTER 2: STEREO VISION IN A COMPUTER ENVIRONMENT (9 pages)	
2.1 Overview	8
2.2 PCB Inspection Approaches	8
2.2.1 Reference Comparison Approach	8
2.2.2 Design Rule Checking Approach	10
2.2.3 Hybrid Approach	11
2.3 The Need for a Better Method	11
2.4 Chapter Summary	16

CHAPTER 3: DEVELOPMENT OF THE WAVELET-BASED INSPECTION

SYSTEM (19 Pages)

3.1 Overview	17
3.2 Wavelet Transform	17
3.2.1 Basic Operation of the Wavelet Transform	18
3.2.2 Discrete Wavelet Transform	18
3.3 Wavelet Transform for Image	21
3.4 Differencing Operation	22
3.5 Defects Localization	22
3.5.1 Connected-Component Labeling Operation	24
3.5.2 Windows Coordinate Searching Operation	25
3.5.3 Mapping Operation	25
3.5.4 Windowing and Defect Extraction	26
3.6 Development of <i>Inspect</i>	27
3.7 Operational Flow of <i>Inspect</i>	32
3.8 Example Using <i>Inspect</i>	33
3.9 Chapter Summary	35

CHAPTER 4: EXPERIMENT AND PERFORMANCE ANALYSIS (13 Pages)

4.1 Overview	36
4.2 Experimentation	36
4.2.1 Image Difference	37
4.2.2 RLE-Based Image Difference Algorithm	41
4.2.3 Wavelet-Based Image Difference Algorithm	41

4.3 Result Using <i>Inspect</i>	45
4.4 Discussions and Conclusions	48
 CHAPTER 5: CONCLUSIONS AND RECOMMENDATIONS (4 Pages)	
5.1 Overview	49
5.2 Conclusions	49
5.3 Achievements	51
5.4 Recommendations	54
 REFERENCES	 55

ACKNOWLEDGMENTS

I would like to express my appreciation to the Ministry of Science, Technology, and Environment for the financial support without which the project could not have been carried out. In this regard, I would also like to thank Research Management Centre (RMC) for the excellent and systematic management of the grant as well as the moral support given during the course of this research.

My sincere thanks also go to Mr. Zuwairie Ibrahim, my master student, as well as Mr. Rokhamsani Ghazali, my research officer, who have done a great and tremendous amount of contributions towards the success of this project.

I am also grateful to Universiti Teknologi Malaysia for providing a convenient and conducive atmosphere for undertaking this research.

Finally, I would like to thank all the staff and colleagues in the Faculty of Electrical Engineering for their valuable assistance and friendly treatment throughout the period of the research.

CHAPTER 1

INTRODUCTION TO PCB INSPECTION

1.1 Project Background

Printed circuit board or in short PCB fabrication process is a multidisciplinary process. The most critical part in the PCB manufacturing is the etching process where the copper board will undergo 'peeling' process whereby the circuit layout will be preserved while the rest of the copper background will be washed out. In order to minimize scrap caused by the wrongly etched PCB panel, inspection has to be done. Among the practises is to inspect for any defect visually employing human operators. Not only that this process is time consuming, it is also highly prone to errors due to humans' factors. The next trend then is to use a computerized inspection system. However, all of the inspections are done after the etching process where any defective PCB found is no longer useful and is simply thrown away. Since etching process costs 70% of the entire PCB fabrication, it is definitely uneconomically to simply discard the defective PCBs. Hence, this project proposes an automatic visual inspection on the PCB before the etching process so that any defect that could be found on a PCB would be able to be reprocessed.

1.1.1 PCB Fabrication Process: An Outline

Aithal, et. al [1] gives the stages involved in PCB fabrication process in some detail. Following paragraphs briefly describe the stages involved in the PCB fabrication process. Figure 1.1 illustrates the various stages in the PCB fabrication process.

Boards with thin layer of copper on one side are used for fabrication of single-sided PCBs. These boards are cut into pieces. These pieces of board are called panels.

The input item for the PCB fabrication process is the artwork. Artwork is a film with the PCB pattern designed on it. Based on the artwork, stencil that is a mask of circuit pattern is built for circuit printing process. Here, the designed circuit pattern is printed over the copper foil with blue ink, which acts as etch resist for subsequent etching stage.

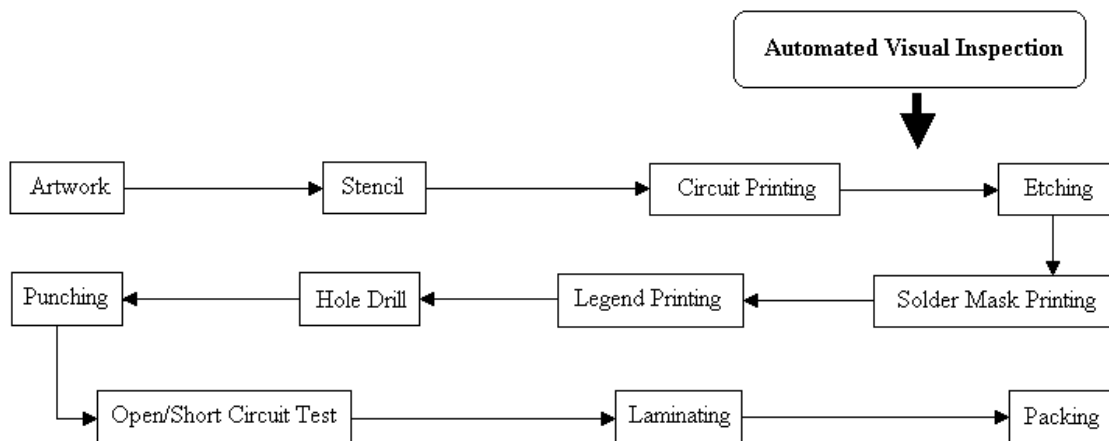


Figure 1.1 : PCB fabrication process

Once the circuit printing is done, the etching process takes place. This process is an irreversible process. Copper foil is etched by spraying the etchant to the panel as the panel moves on the conveyor. The etchant will bare the unwanted copper foil, which must be etched away to leave the copper pattern.

Solder mask (green ink) printing is needed to make sure there is no short circuit occurs during soldering. The solder mask is typically applied by screen-printing using solder mask film, which enables the entire board surfaces to be covered, except for the holes and pads. Next, the legend is screen printed onto PCBs to identify the components. This printing operation is performed using legend print film.

At the hole drill stage, the board is drilled with 2 minimum holes. These 2 holes are important for the alignment purpose either in assembly or inspection process. Once the panel is drilled, the next stage is punching. Here, all necessary holes are created or punched. The punched board goes to electrical test to check if there is any open or short circuit occurs on the board. Finally, the PCB is laminated to prevent oxidation before packing.

1.1.2 Inspection

At various stages of the fabrication process, inspection is done. If the panel is accepted at that stage, it is passed on to the next stage. Otherwise, the panel goes back to rework, to the same stage of operation. But in some of the cases, the panel is rejected. For such cases, the panel inspection is critically important.

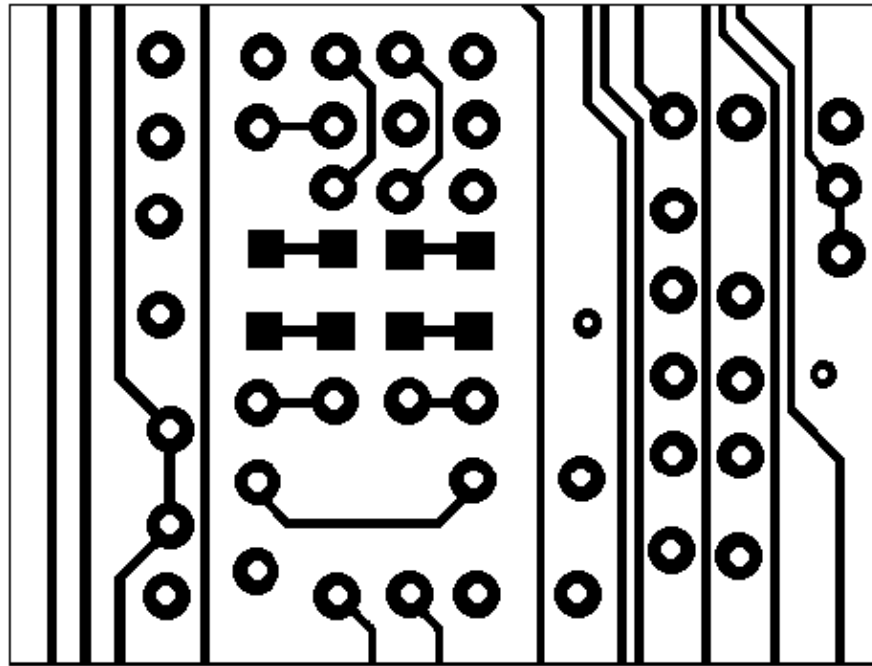
Current practice in PCB fabrication requires etching process. This process is an irreversible process. The printing process, which is done before etching process, caused most destructive defects found on the PCB. Any misprint will cause the etched board to be useless. Since laminated board constitute most of the total production cost, it is important that the board is properly inspected before being etched. Otherwise, the wrongly etched board will be thrown away. This, in return, requires a system to detect online or in real-time any defect caused by the printing process.

1.1.3 Defects

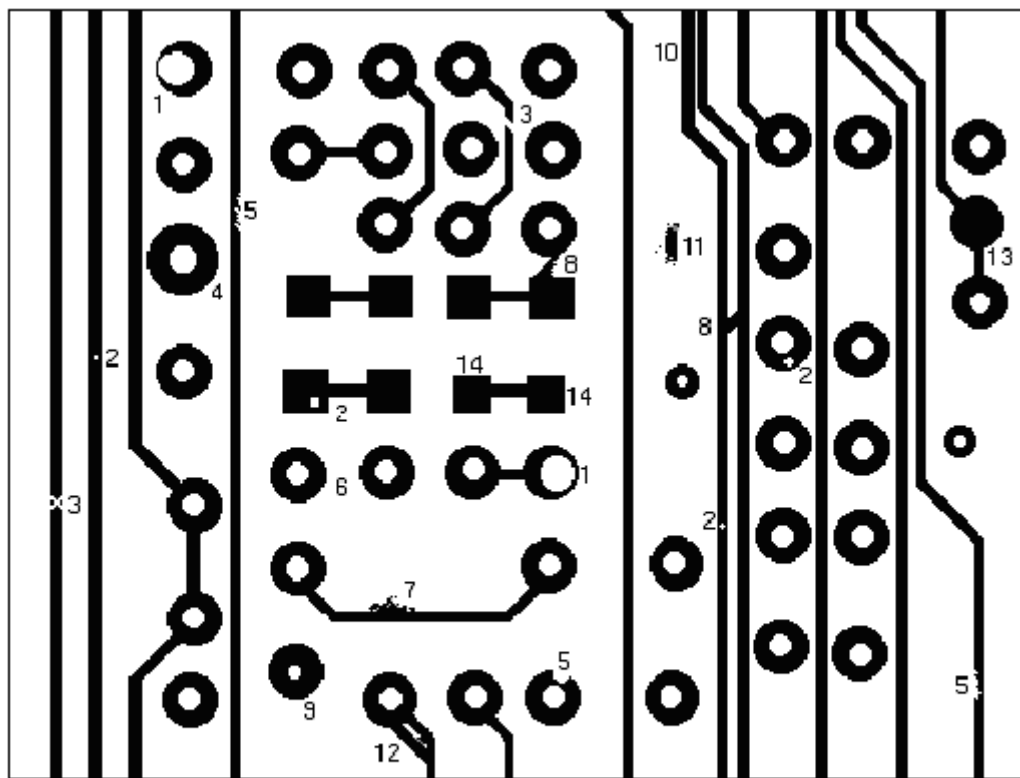
A variety of defects can affect the copper pattern of PCB. Some of them are identified as functional defects, whereas the others are visual defects. Functional defects seriously cause a damage to the PCB, meaning that the PCB will not function as needed. Visual defects do not affect the functionality of the PCB in short term. However, in a long period, the PCB will not perform well since the improper shape of the PCB circuit pattern could contribute to potential defects. Thus, it is crucial to detect these two types of defects in the inspection phase. Figure 1.2 (a) shows an artificial defect-free PCB image pattern. Figure 1.2 (b) shows the same image pattern as in Figure 1.2 (a) with a variety of defects on it. The printing defects and anomalies that will be looked at, for example, are breakout, short, pin hole, wrong size hole, open circuit, conductor too close, underetch, spurious copper, mousebite, excessive short, missing conductor, missing hole, spur and overetch. These defects are shown in Figure 1.2 (b).

1.2 Motivation

This project is motivated mainly by the need for more efficient techniques in inspection of the PCB panel in PCB fabrication process. Normally, a couple of operators are assigned in each station to manually check the PCB panels. This technique is not economical in a long run as it takes many man hours. In addition, humans are prone to making errors especially due to fatigue. Moreover, it is impossible to check the entire PCB panels at every location without any delay. Instead, the printed laminate is sampled a certain interval of quantity for manual inspection.



(a)



- | | | | | |
|----------------------|---------------------|------------------|--------------------|--------------------------|
| 1. Breakout | 2. Pin Hole | 3. Open Circuit | 4. Underetch | 5. Mousebite |
| 6. Missing Conductor | 7. Spur | 8. Short | 9. Wrong Size Hole | 10. Conductors too close |
| 11. Spurious copper | 12. Excessive Short | 13. Missing Hole | 14. Overetch | |

(b)

Figure 1.2 : (a) An example of good PCB patterns (b) An example of defective PCB patterns

As the electronic circuitary technology advances, the PCB pattern becomes denser and complicated to facilitate smaller end products. Thus, manual inspection is not applicable anymore. Meanwhile, the advances in computers in term of high speed, large memory with low cost have resulted in better and cheaper equipment for image processing. Hence, there exist a possibility of introducing and implementing an automated PCB inspection system to remove the subjective aspects of manual inspection. At the same time, the automated PCB inspection system provides real time assessment of the PCB panel.

From the literature review, it is noted that there has been an increasing number of applications for wavelets and multiresolution analysis including (but not limited to) image compression [2], image denoising [3] and edge detection [4]. Up till now there is still no clear advantages of wavelets in industrial inspection application, especially for PCB inspection. This is a secondary motivating factor for the thesis.

The emphasis here is on the improvement of inspection time using wavelet-based technique. The algorithm proposed in this thesis has been tested on three PCB sample images. The classification or analysis of the defects detected is beyond the scope of this thesis.

1.3 Objective

The objective of this project is to design and develop an algorithm for automated visual PCB inspection that will automatically detect and locate the printing defects occurred on printed circuit boards. The primary concern of this project is to make use the advantages of wavelet, related to multiresolution analysis (MRA) in order to detect and locate the printing defects with a minimal inspection time experimentally. The technique proposed should produce the output that is suitable for defect classification stage. Once the algorithm is developed, it will be tested with samples of PCB pattern. A model for the actual implementation of this inspection system will be shown later in the report.

1.4 Scope Of Work

In designing and developing a new defect detection and localization algorithm for automated visual PCB inspection, the scopes of the project have been defined as follows:

1. The whole PCB manufacturing stages comprise of bare-board fabrication, loaded board assembly and soldering process. For every stage, an automated visual inspection can be applied to facilitate the reliability test of the product. The algorithm is designed for the inspection of bare PCB panels only. The inspection for loaded PCB could be a potential future project under different grant scheme. Research work related to the component insertion inspection and solder joints inspection can be revised in [5-10].

2. There are three types of printed circuit boards available today [1]. They are:
- Single sided boards: where the entire circuit is laid on one side of the board and the holes should be drilled on the board for mounting of components or for interconnection of components.
 - Double sided boards: with the circuit on both sides of the board and electrical connection is establish by drilling holes through the board and plating copper through the holes.
 - Multilayer boards: two or more pieces of PCB panel are stacked up together. Electrical connections are established from one side to the other and to the inner layer by drilled holes, which are subsequently plated through with copper.

Although it is possible to apply the proposed algorithm for the inspection of multi-layer boards and also the double-sided boards, this project concentrates more on the single sided boards inspection for experimental purpose.

3. Automatic PCB inspection algorithm is designed to detect any one of the 14 types of defects mentioned previously. These 14 types of defects are expected to occur after the printing process. Thus, the defects caused by design-rule violation and the defects classifications of defects detected are beyond the scope of the project.

4. This project emphasis on the development of an efficient and fast algorithm implemented of PC. Even though higher speed could be achieved using dedicated hardware or using DSP processor chips, it is beyond the scope of this project to evaluate or design the actual hardware system.

1.5 Organization of the Report

This report is organized as follows. Chapter 2 gives some reviews of the background, mainly on the comprehensive approaches of the automated visual PCB inspection followed by the research methodology for the project. Mathematical relationships used in the development of the proposed algorithm are presented in this chapter. Chapter 3 describes the development and implementation of the algorithm in a program called *Inspect*. This software was developed using many image library functions from *MVTools* libraries compiled under the Visual C++ environment. Chapter 4 presents some of the experimental results obtained using the proposed technique. Performance accuracy and computation time are discussed in this chapter. Comparison with run-length-encoded (RLE) technique is also presented. Finally, chapter 5 ends this report with conclusions as well as some indications on the future direction of the project.

CHAPTER II

OVERVIEW ON EXISTING PCB INSPECTION SYSTEM

2.1 Overview

This chapter starts with a review of approaches existed in automated PCB inspection. The advantages and disadvantages of these techniques are addressed. Previous work related to this project is also highlighted in this chapter. At the end of this chapter, wavelet-based technique for PCB defect detection and localization is proposed to overcome the weaknesses of existing techniques and algorithms experimentally in term of defect detection, defect localization and the overall inspection time.

2.2 PCB Inspection Approaches

Numerous PCB inspection algorithms have been proposed in the literature to date. Moganti, et. al [11] divided the PCB inspection algorithms into three main categories: reference comparison (reference-based) approach, design-rule checking (non-referential) approach and hybrid approach which involved a combination of reference comparison and design-rule approach.

2.2.1 Reference Comparison Approach

The reference comparison approach compares the reference PCB image to the tested PCB image. There are two major techniques: image comparison technique and model-based technique.

The simplest method for image comparison technique consists of comparing both images pixel-by-pixel using XOR logic operators (also called image difference operation). It is based on the assumption that, any difference between the reference and the test image is considered as a defect. The operation is simple but the main constraint found in this image comparison technique is on achieving a precise alignment of the reference PCB and the test PCB for image registration. Instead of XOR logic operator, image mathematical operation is also useful. For instance, the work carried out by Wen-Yen, et. al [12] did the direct subtraction of the reference to the test image to produce *Positive (P)*, *Negative (N)* and *Equal (E)* pixels. Defects are

detected on P and N pixels. After that, defect classification is done based on P , N and E pixels.

Other method utilizes the features extracted from both the reference and the test PCB image. Jarvis [13] extracted the features of both PCB image by using 5×5 or 7×7 binary element. The unmatched features are verified further in order to categorize whether the features are defects or not. However, this method requires a big number of templates. As an example, for a 512×512 pixels of PCB image, 12 222 features are extracted and these 12 222 features shall be processed for defects detection.

The features of a PCB image can be extracted in a different way. Hara, et. al [14] extracted the features of boundary lines and small line-width patterns by using 2 types of extraction operators. Next, these features will be compared. When the corresponding points on the reference PCB pattern and the test PCB pattern exhibit the same features, the pattern is determined as having no defects. Otherwise, a defect is determined.

Model-based methods begin with conversion of images into a predefined model before inspection execution takes part based on the model. An early proposal use graph-matching technique. Under this technique, the defective PCB image can be successfully recognized but the position of each defect cannot be located. The major difficulty of this method is related to the matching complexity. Ja and Suk [15] introduced tree representation scheme of PCB image. Although the tree representation technique is less complex than graph-matching technique, yet the location of the defects still cannot be retrieved. Another model-based method compares two PCB images based on their connectivity [16] but the connectivity defects are limited to missing hole, short circuit or excessive short and open circuit only. Ninomiya et. al [17] extended the connectivity method by making use the operations of dilation and erosion in connectivity comparison method to detect fatal defects like short circuit, open circuit, lack of pattern width and lack of spacing.

As opposed to connectivity method, other alternative is based on a variant of the N-tuple technique. Ouslim and Curtis [18-19] exploited this technique in order to detect the three most occurring faults: overetch defects, underetch defects and annular ring inspection (drilled holes dimension violation and missing of pads). This technique is able to detect the defects as small as 1 pixel.

The inspiration to process the PCB images in compressed run length encoding (RLE) is realized by Ji-joong, et. al [20], Ercal, et. al [21-23] and Hou, et. al [24]. Ji-joong, et. al introduced a modified run length code (MRLC) as a compressed form of a bitmap image. However, the algorithm to process the MRLC data to extract the defects is not outlined in their paper. Under the same idea, Ercal et. al and Hou et. al convert a binary image to RLE data. Consequently, they came out with a systolic algorithm to produce differenced image but the process is applied on RLE data. RLE-based algorithm is claimed as a way to minimize the storage of data and also the inspection time effectively.

The latest work of reference-based approach is carried out by Nam-Hyeong, et. al [25]. They design a PCB inspection system that is able to detect the defects on the test image based on the stored reference image by matching them using image difference operation. Block matching is performed to solve the misalignment between the two PCB images. Pre-processing such as thresholding, dilation and decision making is applied to the difference image in order to detect open and short defects. The inspection system is claimed as a significantly faster system when compared to the existing techniques but a lot of work should be done if the same system is going to be implemented to detect more defects, rather than open and short defects.

2.2.2 Design Rule Checking Approach

Generally, this approach tests the design-rule of PCB images to determine whether the pattern falls within the required dimensions. They work on the idea that a pattern is defective if it does not conform to the design specification standards of a PCB.

As an example, neighbourhood-processing techniques such as morphological processing is used frequently, which consists two basic operations: erosion and dilation. Seyfullah and Onural [26] first separate a PCB pattern into conductor, hole and substrate by giving them the initial value of 1,2 and 0 respectively. Then, they apply an algorithm based on dilation and erosion operation for defect detection related to the violation of the minimum land width (MLW) requirement, minimum conductor spacing (MCS) requirement and minimum conductor trace width (MCTW) requirement.

Higher form of morphological processing have also been used. The examples are opening (erosion followed by dilation), closing (dilation followed by erosion),

skeletonization, thinning and connectivity preserving shrinking (CPS). Ahmed and Jain [27] combine the morphology operations and graph-matching technique. Graph-matching technique is applied for rule verification purposes. Experimental results of this technique indicate a 100 percent detection of all shorts, opens and minimum width violations. Qin-Zhong and Danielson [28] introduce a new version of operation based on morphology operation called connectivity preserving shrinking (CPS) for PCB inspection. Jelloul and Mohamed [29] introduce two new algorithms of dilation and connectivity preserving shrinking to increase the time efficiency. Morphological method is used again by Borba and Facon [30] by using three inspection rules to detect the defects from lack and/or excess of copper.

The main advantage of the design-rule checking approach is it does not require a reference PCB image. Thus, the approach is not subjected to the alignment problem. Since the technique verifies the design-rule, the disadvantage is it might miss defects that do not violate the rules [11]. Furthermore, rule standardization is needed for the entire image of the inspected PCBs.

2.2.3 Hybrid Approach

The hybrid approach increases the defect detection efficiency of the PCB inspection algorithm by using a combination of both referential and non-referential techniques. Effort carried out by Charette et. al [31] is an example, where they have utilized template matching as a first stage and dimensional verification technique as a second stage to detect the PCB defects. The strengths of both approaches can be exploited to overcome the weaknesses. This is the main advantage of the hybrid approach.

2.3 The Need for a Better Method

Numerous techniques have been proposed under model-based method. They are graph-matching technique, tree representation technique, connectivity technique and RLE-based technique. Both graph-matching and tree representation techniques effectively identify the defective board but they are not able to provide the localization of the defects detected. Connectivity technique on the other hand is only capable to localize the defects related to the connectivity such as missing hole, short

circuit or excessive short and open circuit. Thus, to achieve a good localization of the defects, RLE-based technique is the best technique compared to graph-matching technique, connectivity technique and tree representation techniques.

Ercal and Hou claimed that RLE-based technique is an effective way to minimize the storage of data. However, as the technology improves, the hard disk and memory (RAM and ROM) becomes less expensive and thus, the limitation of storage data is not a serious problem anymore.

They also claimed that RLE-based technique could be used to reduce the computation time of a PCB inspection algorithm. However, experimental result shows that it takes about 6.23 seconds to convert a 400 x 400 pixels bitmap image into RLE data. The conversion is done using MATLAB. The simulation result indicates that the bitmap to RLE conversion consumes a lot of time. Furthermore, the RLE data needs to be reconverted into bitmap image for visualization of defects after the systolic image difference algorithm on RLE data is done. To achieve faster inspection response, Moganti and Ercal [32] design an offline segmentation algorithm to divide a PCB images into many individual basic patterns. The segmentation algorithm is essential to facilitate the distribution of image data in parallel processing for faster inspection response.

Wavelet transform has become a very prominent tool in many areas of signal and image processing. This is mainly related to its multiresolution processing. The subject of multiresolution image processing has been explored by a number of researchers for a past few years. A few of them have been discussed as in [4] in the area of edge detection using multiresolution technique. Research in this subject discovers another potential application of wavelet transform in image processing, particularly in PCB inspection system. In this thesis, an algorithm for defect detection is presented, which is the modified version of the image difference algorithm based on wavelet transform.

As before, two images are needed, the reference image and the test image. Note that, in this thesis, the reference image and the test image are taken from the previous research works or synthetically generated. Then, second level wavelet transform is applied to the reference image. The reference image and also the wavelet outputs are stored in memory. This step is done offline once only as indicated by the dash box in Figure 2.1.

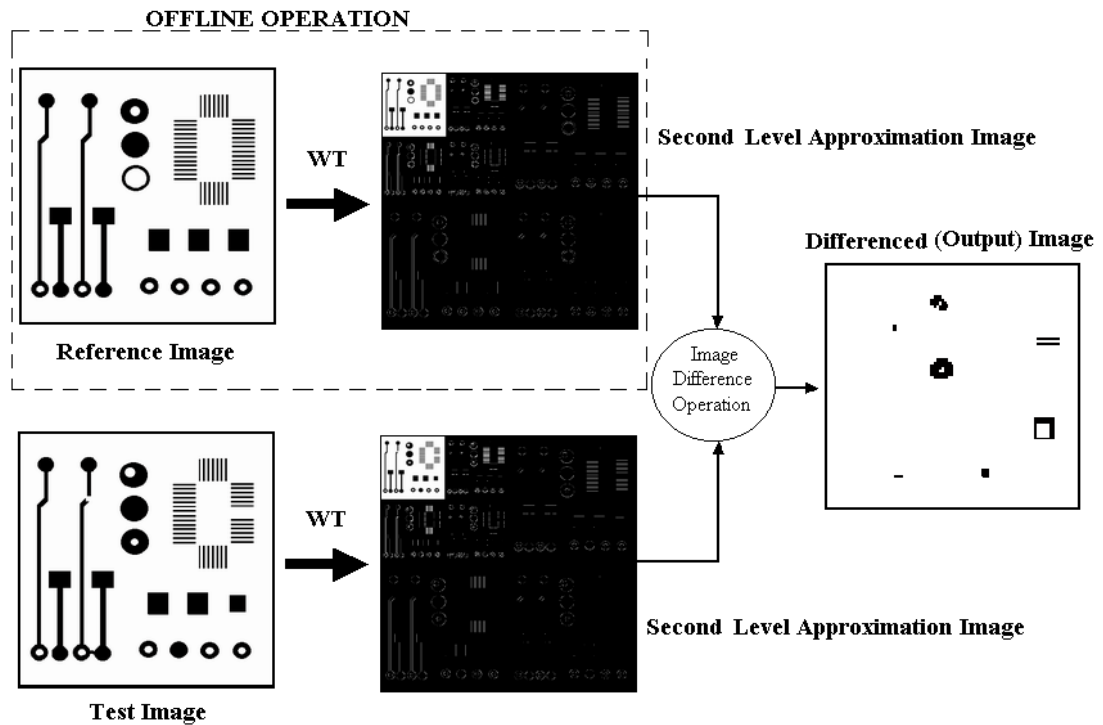


Figure 2.1: Wavelet-based image difference algorithm

Similarly to the reference image, second level wavelet transform is also applied to the test image but now in an online fashion. The flow of the algorithm, which is illustrated in Figure 2.1, consists of the example of a reference, a test image, the resultant wavelet transform output and also the defect detected in the output image of image difference operation.

Figure 2.1 clearly shows that, referring to the image difference operation, instead of taking both the fine resolution reference image and the test image into the image difference operation, wavelet transform is first applied to both images. For every level of decomposition, the wavelet transform maps an input image to another with half of the resolution. The mapped image is then taken as an input image for subsequent iteration to produce smaller and smaller images. Since the proposed algorithm involved two iterations of wavelet transform, a second level approximation image is produced. This image is named as coarse image. The coarse image size and also the resolution of the image are much reduced by a factor of 16 in comparison to its original image.

The main advantage of this algorithm is due to the fact that, computational time for a small data is shorter than a big data. Since the size of the second level approximation image is reduced by 16 times, this small data is taken for image

difference operation in order to test the occurrence of defects with a minimal execution time.

It is possible to detect all the printing defects occur by simply applying the image difference operation between the coarse reference image and coarse test image. The coarse image processing is only applied to defects detection procedure. However, the defects localization should be highlighted on the original image for better visual perception.

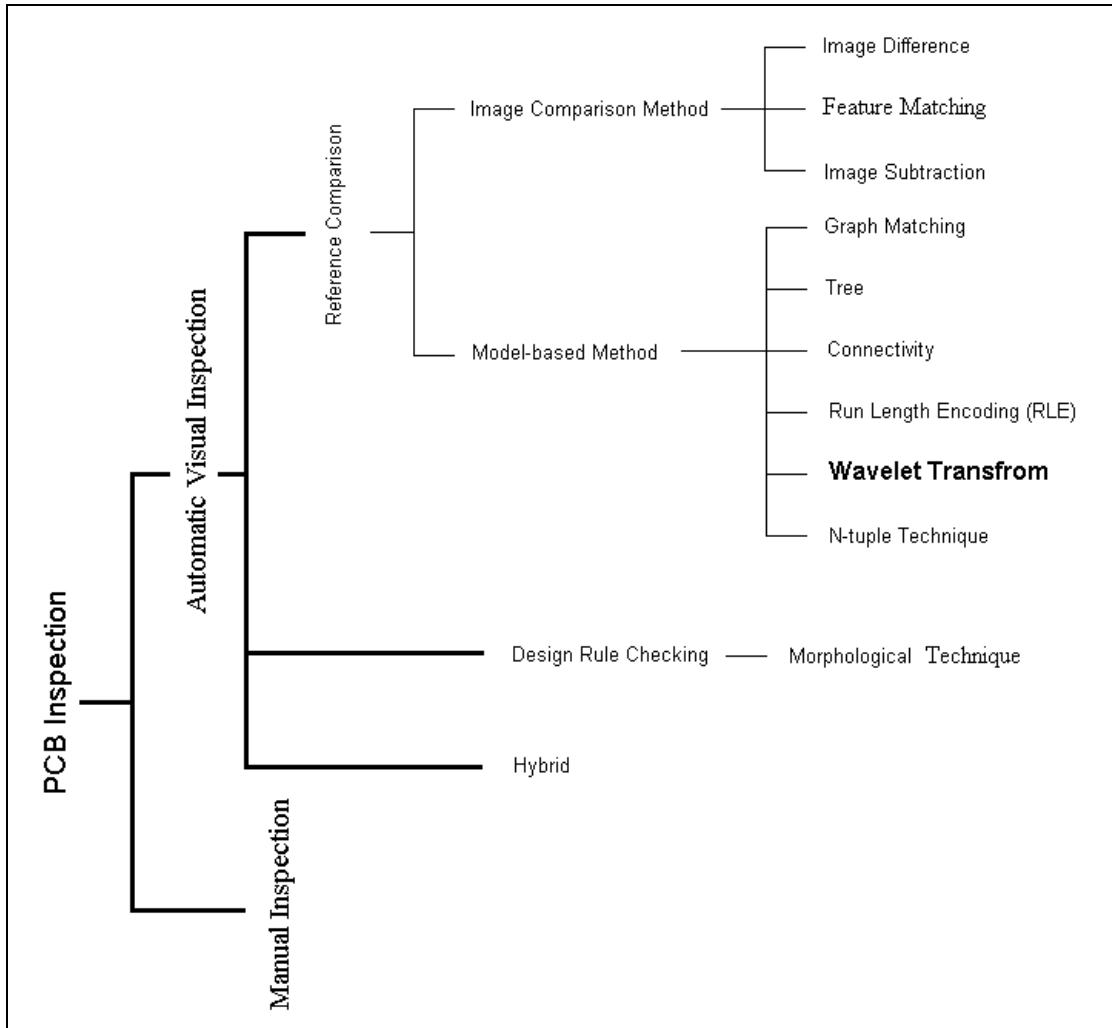


Figure 2.2: Classification of PCB inspection approaches

As a result due to the comprehensive literature on the PCB inspection approaches, the overall approaches, methods and techniques can be classified as depicted in Figure 2.2. This project has introduced a new model-based PCB inspection technique using wavelet transform as shown in Figure 2.2, indicated by bold face typeset.

As an addition, Table 2.1 shows several commercial PCB inspection systems until 1996 given by Moganti, et. al [11]. The table clearly shows that most of the commercial systems make use both the design-rule checking and comparison method for defect detection. Although the hybrid approach is generally chosen, this project concentrates on the reference comparison approach separately.

Table 2.1 : Commercially available bare PCB inspection systems

System	Inspection Methods	Image System	Resolution	Scan Rate	Features/Benefits
AOI-System AOI-20	Design Rule Checking (8 kinds of detection sensors) and Comparison method	20 CCD Cameras Reflection/Transmission lighting	1 mil	6.00 sq. ft/min	Continuous operation is possible through the use of conveyor system
Blarria BIOP-5002	Simultaneous use of Design Rule Checking and Image Comparison	Two CCD Cameras Halogen Lamp Lighting	1 mil	6.00 sq. ft/min	Bleno driven user-friendly software for easy and fast setup. Fast unit under test change over using vacuum adaptor system
Dai-Nippon Screen OPI-5220	Design Rule Checking and Comparison method	LED light, CCD line sensor Reflection/Transmission lighting	1 mil	19.20 sq. ft/min	Complete Comparison Inspection Inspection function of product with special shape
Shin-Nippon Steel PT-2130	Design Rule Checking and Comparison method	Halogen Lamp, Multi-Directional illumination Speedy CCD Camera	1 mil	33.33 sq. ft/min	Continuous Variable Resolution (0.2 to 1 mil) Fastest Speed
Orbotech PC-1450	Design Rule Checking and Comparison Method (Golden Board or CAD download)	Reflective and Diffusive Omni lighting	Variable resolution 0.25-0.9 mil	18" x 24" pixels 38-160 sides/hour	3-10 mil line width technology

Orbotech V-309i/x	Design Rule Checking and Comparison Method (Golden Board or CAD download)	Fluorescent technology (Blue Laser)	Variable resolution 0.4-1.0 mil	18" x 24" pixels 77-180 sides/hour	3-10 mil line width technology for high volume PCB shops
Orbotech PC-1490	Design Rule Checking and Comparison Method (Golden Board or CAD download)	Reflective and Diffusive Omni lighting	Variable resolution 0.20-0.5 mil	18" x 24" pixels 45-130 sides/hour	3-6 mil line width technology for high volume PCB shops
Orbotech PC-1411	Design Rule Checking and Comparison Method (Golden Board or CAD download)	Reflective and Diffusive Omni lighting	Fixed resolution 0.5 mil	18" x 24" pixels 45 sides/hour	Low cost startup, On-line verification
Orbotech Vision Blaser	Design Rule Checking and Comparison Method (Golden Board or CAD download)	Fluorescent technology (Blue Laser)	Variable resolution 0.20-0.5 mil	12" x 12" pixels 80-180 sides/hour	2-4 mil line width technology for high volume PCB shops

2.4 Chapter Summary

PCB inspection approaches can be classified into three main groups: reference comparison approach, design rule checking approach and hybrid approach. This chapter has briefly discussed the advantages and disadvantages of each approach. Among the various approaches, image comparison approach is chosen and model-based inspection is emphasized in this project. Wavelet-based technique is introduced as a solution to minimize the inspection time of a PCB inspection system.

CHAPTER 3

DEVELOPMENT OF THE WAVELET-BASED INSPECTION SYSTEM

3.1 Overview

This chapter presents the development of the wavelet transform-based technique into the framework of the PCB detection. The other important algorithm towards proper inspection is the defect localization i.e. locating the position of the defects with respect to the PCB. These two algorithms are the main thrusts for the developed program called *inspect*. Developed using the C++ platform, *inspect* has been designed such that it can be used either to detect either in on-line or off-line mode. The functional features of *inspect* are discussed later in this chapter.

3.2 Wavelet Transform

Wavelet transform is a time-frequency transform. In the past Fourier analysis has been the dominant transformation method for analyzing signals in the frequency domain. However, a very crucial drawback of the Fourier analysis is that it does not preserve the time aspect of the signal. Hence, Fourier analysis is found to be useful only for stationary and time-invariant signals where time information is not important. However, most practical signals found in real life today are non-stationary and time varying like the ECG and EEG. In this kind of signals, both the frequency and time information are important.

Even though there are other time-frequency analysis methods such as the Short Time Frequency Transform (STFT), Gabor transform, and the Rayleigh transform, wavelet transform has gained a rapid popularity. This is due to the fact that wavelet transform is able to localize such that is able to concentrate on the time information at low frequency while it concentrates on the frequency information at high frequency. This flexibility is enough to make wavelet transform to be very useful in preserving the time frequency information (note: wavelet transform cannot pin point exactly at what time a particular frequency occurs, in fact no other transform could. Wavelet transform gives only the range of time).

3.2.1 Basic Operation of the Wavelet Transform

Wavelet transform works on the basis of scaling and translating the mother wavelet (basic wavelet). Let suppose $f(t)$ is the signal in the time domain. The wavelet analysis of this signal then is given by

$$C_{a,b} = \int_{-\infty}^{\infty} f(t) \frac{1}{\sqrt{a}} \psi\left(\frac{t-b}{a}\right) dt$$

The parameter a is called the dilation factor and has a value greater than zero, and the parameter b is the translation parameter which is a real number. $\psi(t)$ is the mother wavelet. Hence, $C_{a,b}$ is the translated and scaled version of the mother wavelet for a particular a and b . The above formula is the continuous wavelet transform formula.

3.2.2 Discrete Wavelet Transform

Of interest to this project is the discrete version of the wavelet transform. While continuous transform is quite straight forward in its implementation, the discrete version needs further explanation. This report will attempt to cover only that part which is related to the project. Interested reader in this subject can refer to many text books that cover the subject in great details such as in [35] and [40].

An easier way to compute the discrete wavelet transform for a discrete signal is via a mathematical notion of convolution between the signal and the wavelet filter. As given by Mandal, et. al [38], the expression is as follows:

$$h_p[q] = \sum_{m=0}^{\infty} h_{p-1}[m]g[m-2q]$$

where $h_p[q]$ is the output coefficient of the p^{th} level at q^{th} location and $g[.]$ is the wavelet filter coefficients.

Wavelet filter consists of two different filters: lowpass and highpass filters. To simplify the explanation, Haar wavelet is selected, which is the simplest and the oldest wavelet among other wavelet families. The explanation will be done through a simple example given below.

Consider taking the wavelet transform on the input signal shown in Figure 3.xx using Haar wavelet [39]

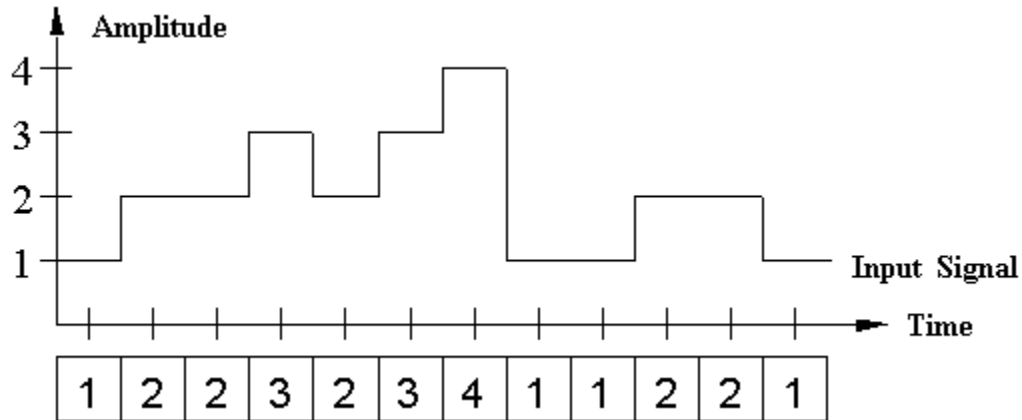


Figure 3.1: Discrete input signal

The two entries Haar wavelet coefficients for the lowpass and the highpass filters are given in Table 3.1.

Table 3.1 : Haar wavelet filter

	First Coefficient	Second Coefficient
Low Pass Filter, $\{c_0, c_1\}$	$\frac{1}{2}$	$\frac{1}{2}$
High Pass Filter, $\{c_1, -c_0\}$	$\frac{1}{2}$	$-\frac{1}{2}$

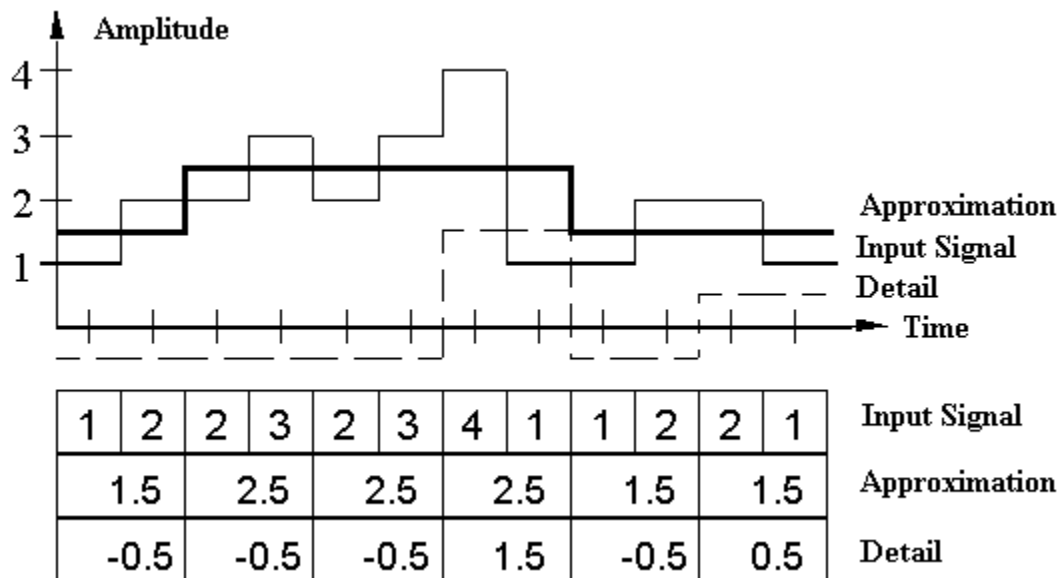


Figure 3.2: Original signal, approximation and detail

The convolution between the Haar lowpass filter and the input signal produces approximation of the signal as shown in Figure 3.2. The difference between the input signal and the approximation is called the detail. The detail is obtained by convolving the

input signal with the Haar highpass filter. The convolution steps are shown in Figure 3.3. Note that the length of the approximation and the detail is reduced by a factor of two with respect to the input signal. In this case, a 12-length input signal is transformed to a 6-length of approximation and detail.

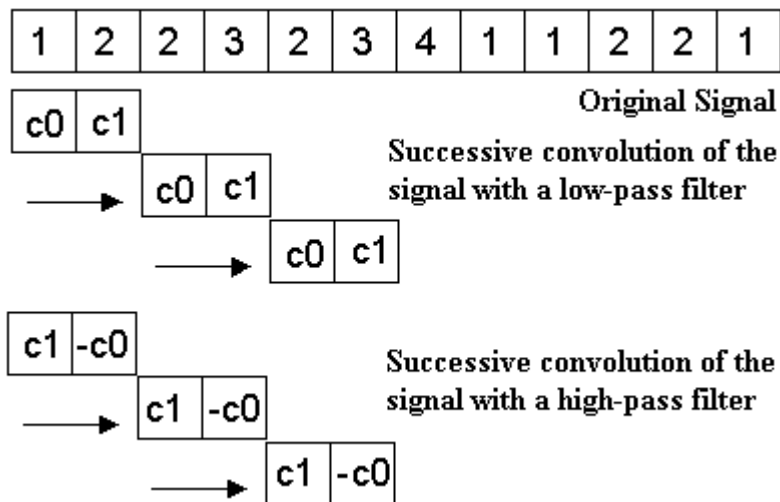


Figure 3.3: Convolution steps

This computation can be applied more than once which forms multilevel decomposition of the signal. As an example, Figure 3.4 shows the wavelet decomposition tree representing four levels wavelet transform.

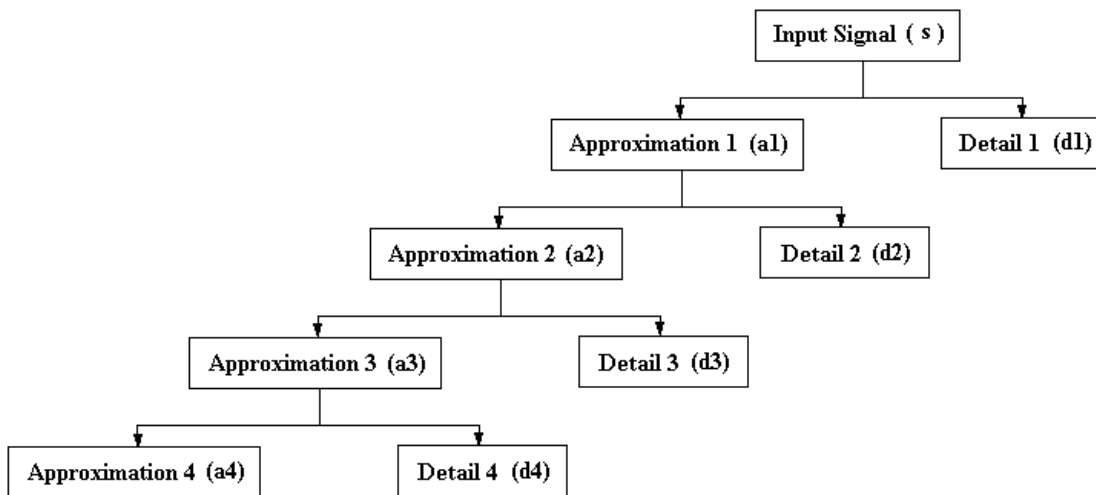


Figure 3.4: Wavelet decomposition tree

3.3 Wavelet Transform for Image

The previous discussion concentrate on the 1-D discussion and implementation of the wavelet transform. Images, however, are two-dimensional discrete signals. Nevertheless, discrete wavelet transform (DWT) can still be applied to images and in many cases, the implementation of wavelet transform on an image can be broken by applying two one-dimensional transforms, one on the column-wise data and the other on the row-wise vector (the order can be interchanged). Hence, in term of the previous explanation, the DWT on an image can be computed first by performing the row/column wise convolution followed by a column/row wise convolution.

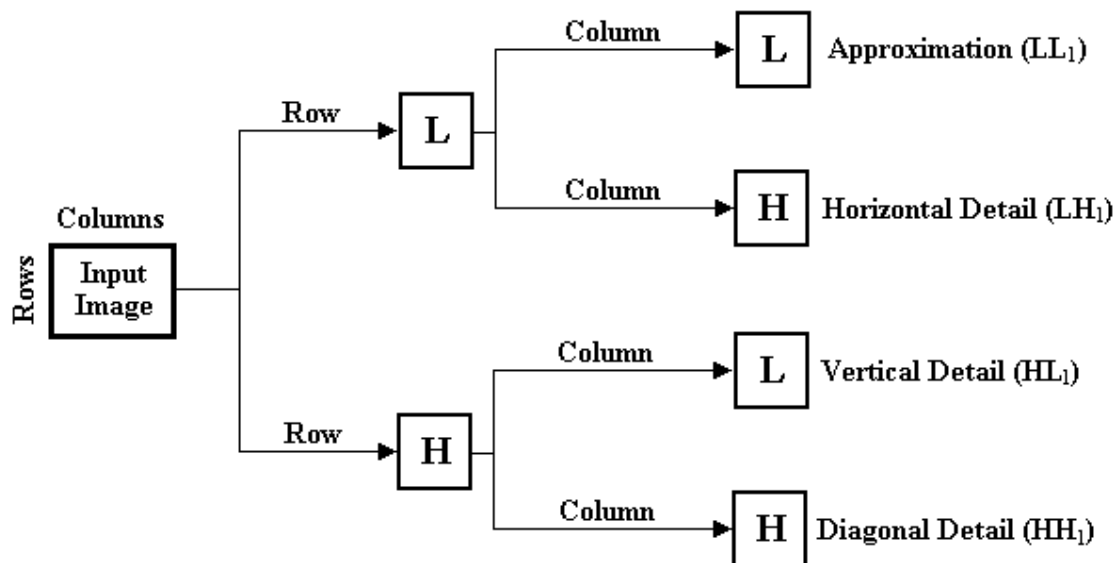


Figure 3.5: Two-dimensional DWT (first level)

Similarly, DWT on an image can be performed multilevel. First level will result in a four sets of output subimages: approximation or also called as the low-low (LL) composition, horizontal detail or low-high (LH_1) composition, vertical detail or high-low (HL_1) composition, and diagonal detail or high-high (HH_1) composition. The subscript indicates the level of the DWT. This concept is illustrated in Figure 3.7 in this figure, the row wise convolution is performed first followed by the column wise convolution. Note that the symbol **L** and **H** denote the lowpass and highpass filter respectively. The second level decomposition is applied only on the LL_1 part. As a result this part will be further decompose into another four sets of subimages, i.e. approximation level (LL_2), horizontal

detail (LH_2), vertical detail (HL_2), and diagonal detail (HH_2) as depicted by Figure 3.6. Further decomposition then can be further applied to the approximation level. At each level, the image gets coarser and coarser which indicates low resolution.

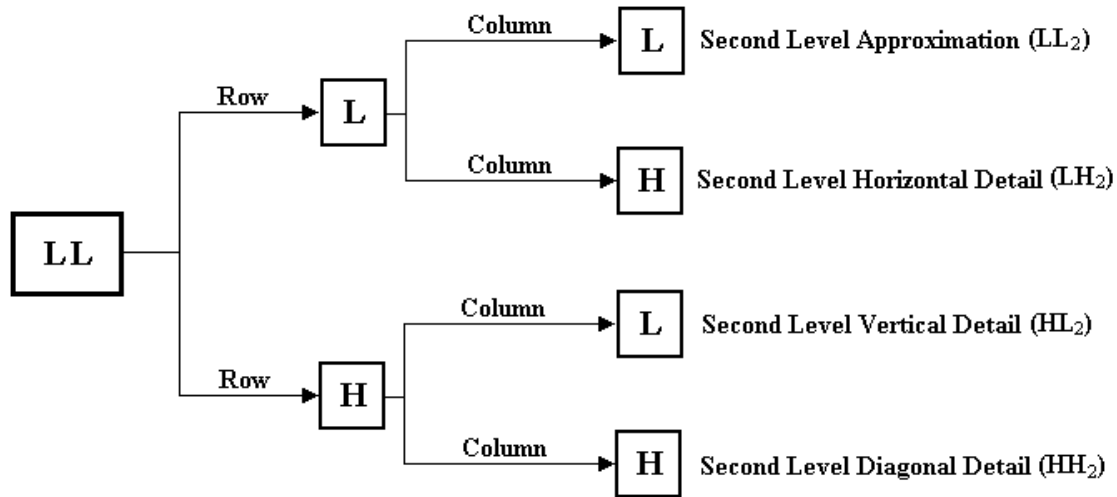


Figure 3.6: Two-dimensional DWT (second level)

Figure 3.7 shows the result applying wavelet transform to an image at 3 levels.

3.4 Differencing Operation

In this project, the image difference is applied to the output of the second level wavelet transform. The first advantage of this technique is that the wavelet transform can be treated as image-to-image transformation. This will enable the wavelet coefficients to be treated as an image and thus allow the image difference operation to be carried out. After that, based on coarse differenced image, the defect localization will be computed in the compressed coarse resolution image. However, the defective areas are marked on the fine resolution original image of the tested PCB. The second advantage is the computation time. It has been found that the wavelet-based algorithm is faster than the full resolution image difference operation as well as the RLE-based technique. Figure 2.1 in Chapter 2 shows the concept of the image difference based on the wavelet transform.

3.5 Defects Localization

The purpose of the defect localization algorithm is to highlight the defective areas on the tested. The defect localization algorithm consists of four core operations, namely:

connected-component labeling operation, window coordinates searching operation, mapping operation and windowing and defect extraction operation.

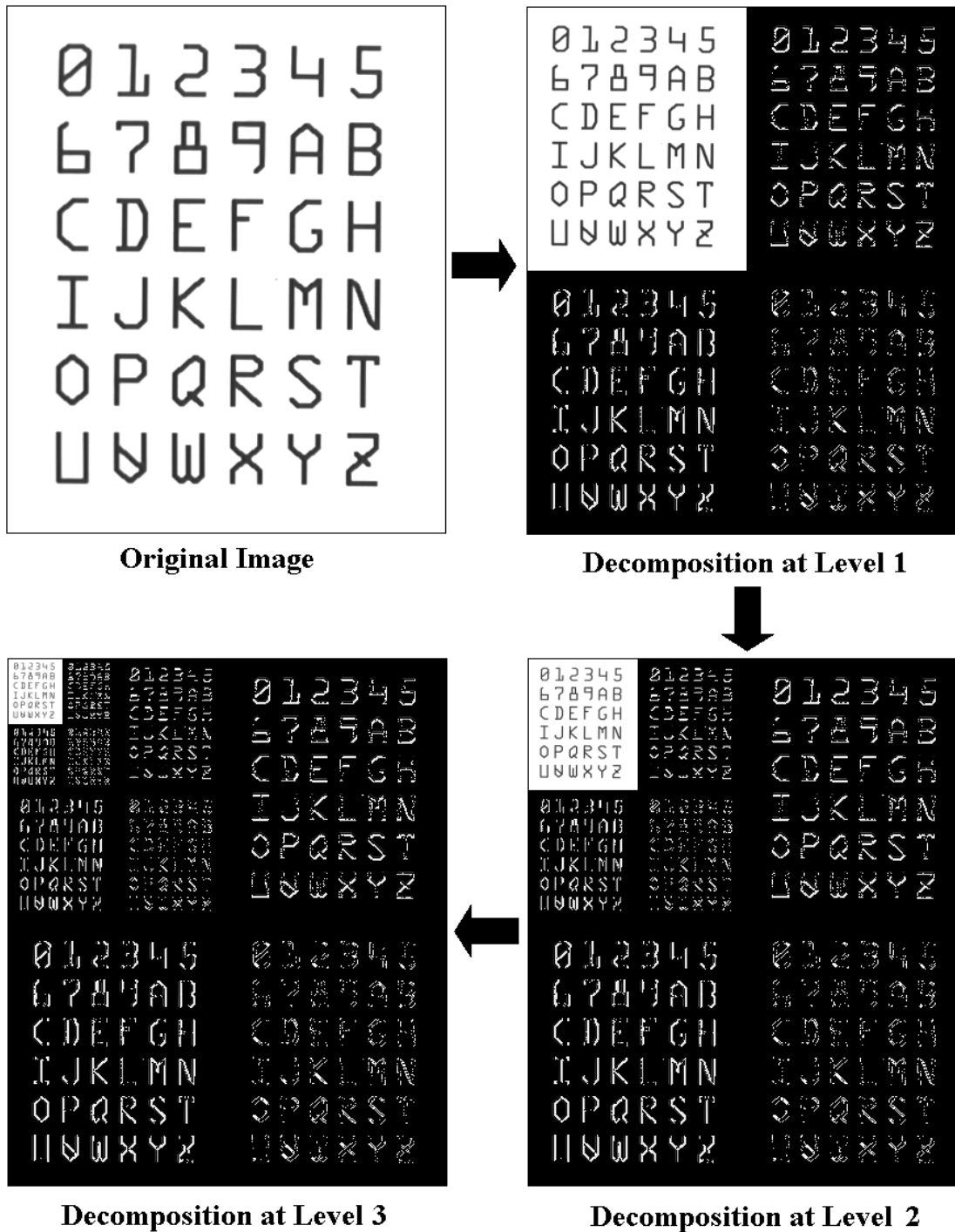


Figure 3.7: Input image and output images of DWT

3.5.1 Connected-Component Labeling Operation

This operation returns the information of the coarse differenced image, which is a binary image, to identify each object in the image. The output of the connected-component labeling operation is the two-dimensional output array that has the same size as the coarse image size. The objects in this array are distinguished by integer values. As an example, consider a small area of a coarse differenced image represented in a two-dimensional 10x10 array shown in Figure 3.8.

0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	0
0	0	0	0	0	0	1	1	1	0
0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
0	0	0	0	1	1	1	0	0	0
0	0	0	0	1	1	1	0	0	0
0	0	0	0	1	1	1	0	0	0

Figure 3.8: An example of a small area in a coarse differenced image

The output array, using 8-connectivity, of the connected-component labeling is shown in Figure 3.9. The algorithm successfully identifies two objects in the coarse level. As shown each object is assigned has been classified using values on 1 to 2. These objects represent defective areas.

0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	2	2	2	0
0	0	0	0	0	0	2	2	2	0
0	0	0	0	0	0	0	2	0	0
0	1	1	1	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
0	0	0	0	1	1	1	0	0	0
0	0	0	0	1	1	1	0	0	0
0	0	0	0	1	1	1	0	0	0

Figure 3.9: The output of the 8 connected-component labeling operation

3.5.2 Window Coordinates Searching Operation

The result from the previous subsection is then pass to this processing module. The objective of this module is to search for the four coordinates of the each object so that a window surrounding the object can be determined. As in the previous module, this search is also done on the coarse resolution image (i.e. the output of the differenced image from the second-level DWT). With Figure 3.10 as the input to this module, the result of this operation is shown in Figure 3.11. Note $RowMin$, $RowMax$, $ColMin$, and $ColMax$ are the four coordinates correspond to minimum row, maximum row, minimum column, and maximum column values respectively.

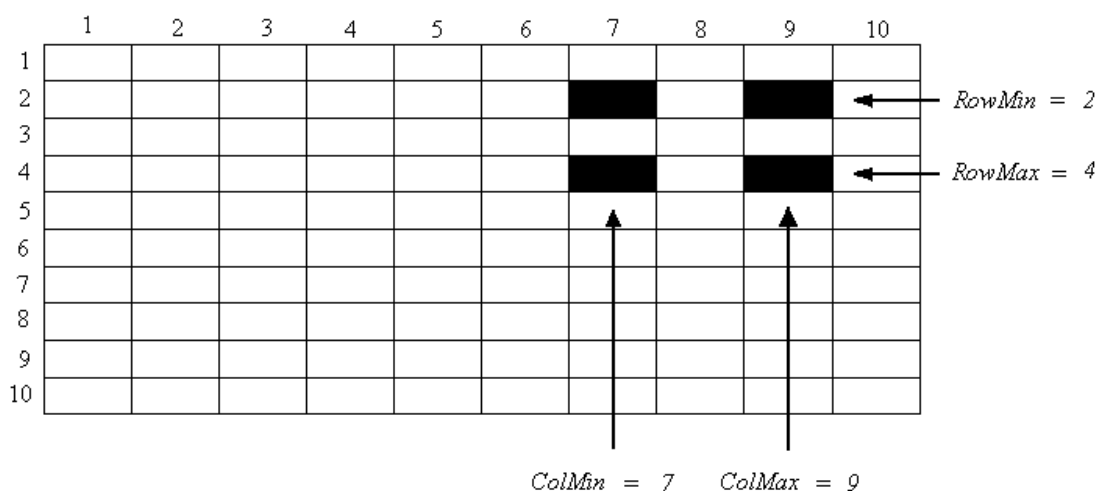


Figure 3.10: Representation of $RowMin$, $RowMax$, $ColMin$ and $ColMax$ for the object number 2

3.5.3 Mapping Operation

This module then will map the four coordinates found in the previous operation to the actual position in the full resolution image. However, the mapping scheme cannot be taken lightly as ineffective mapping technique will cause distortion to the individual drawn window. Considering the results obtain from the previous subsection. If the 10x10 array in Figure 3.10 is to be enlarged 8 times to 80x80, then each of the four coordinates will also be enlarged 8 times. However, realizing that each coordinate now represents a range of values (8 in this particular example), each of the four coordinates has 8 possible values. This phenomenon is shown in Figure 3.11. In order to accomplish as one-to-one mapping so that a proper window of the defective object can be drawn, the following rules are employed.

- 1) The mapped values for *RowMin* and *ColMin* should be the minimum value within the range.
- 2) The mapped values for the *RowMax* and *ColMax* should be the maximum value within the range.

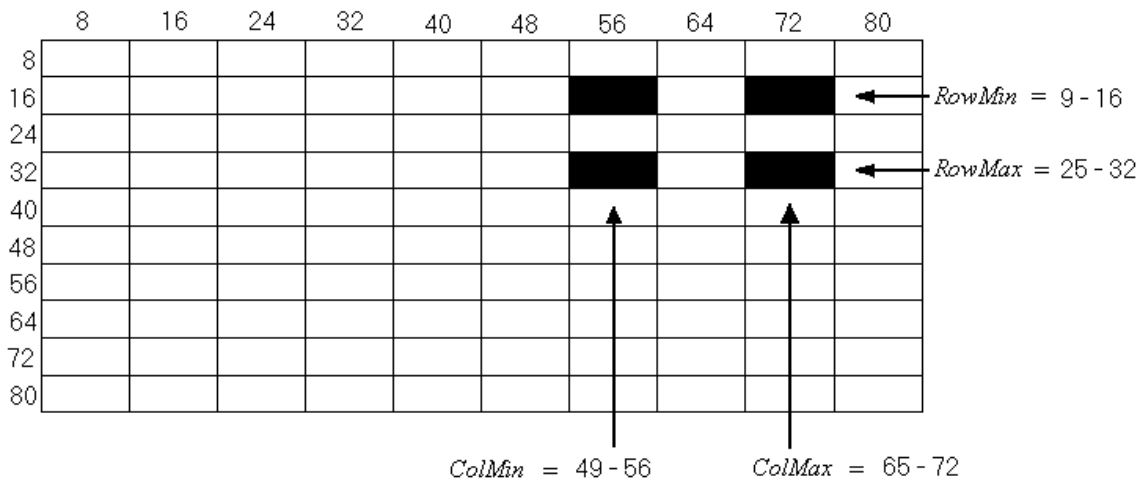


Figure 3.11: The resized image (enlargement factor, $E = 8$)

3.5.4 Windowing and Defect Extraction

Once the appropriate four coordinates have been found on the full resolution, a borderline using these four coordinates is drawn. The object surrounding by this borderline indicates the defect found on the PCB. After the defective areas are windowed successfully, it is possible to segment each defective area is shown in an individual image.

The overall flow of the proposed algorithm is shown in Figure 3.12

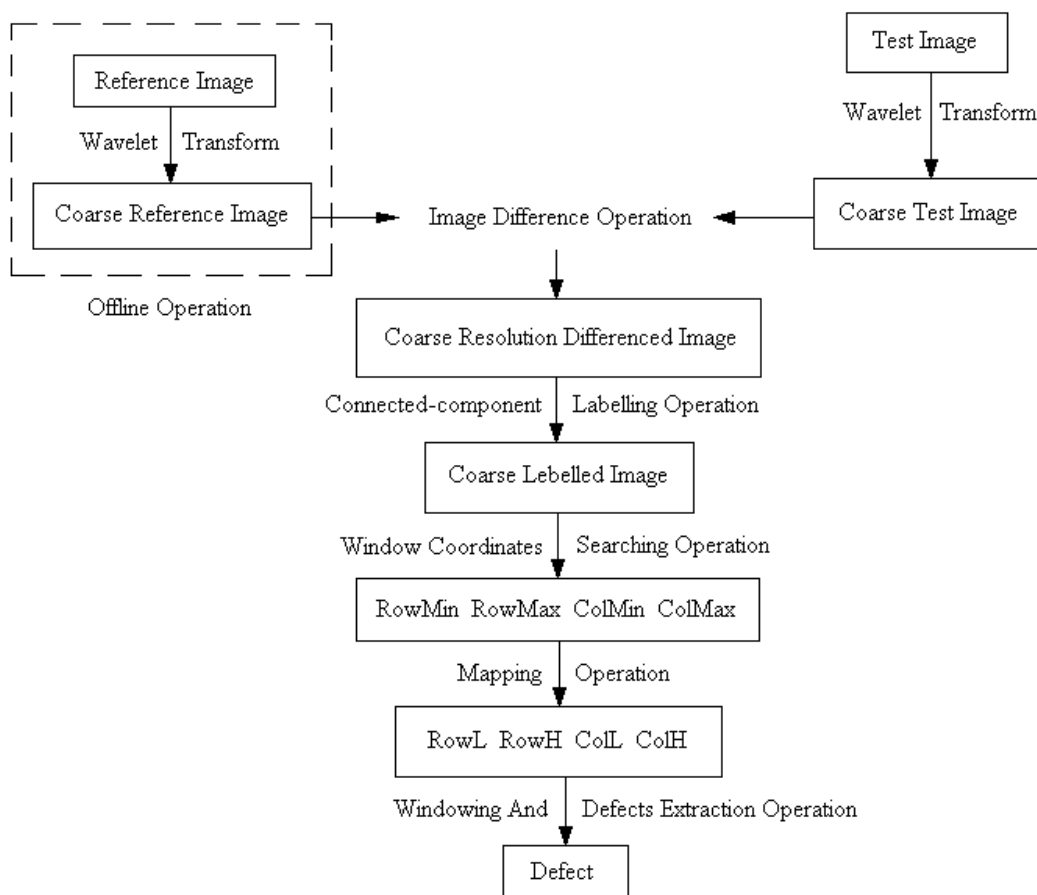


Figure 3.12: The overall flow of the proposed algorithm

3.6 Development of *INSPECT*

The entire algorithms discussed this far have been incorporated in a program called *Inspect*. This program was developed using image libraries developed by Coreco Imaging called *MVTools* (MV stands for machine vision) and was compiled using Visual C++ environment. The GUI for this program when first run is shown in Figure 3.13 below. The application buttons and menus are also shown in the figure while the explanation on the function for each button on the second toolbar is given in Table 3.2. Figure 3.14 to Figure 3.19 shows the submenus that are available under the main menu. Note, the *search* menu is not used.

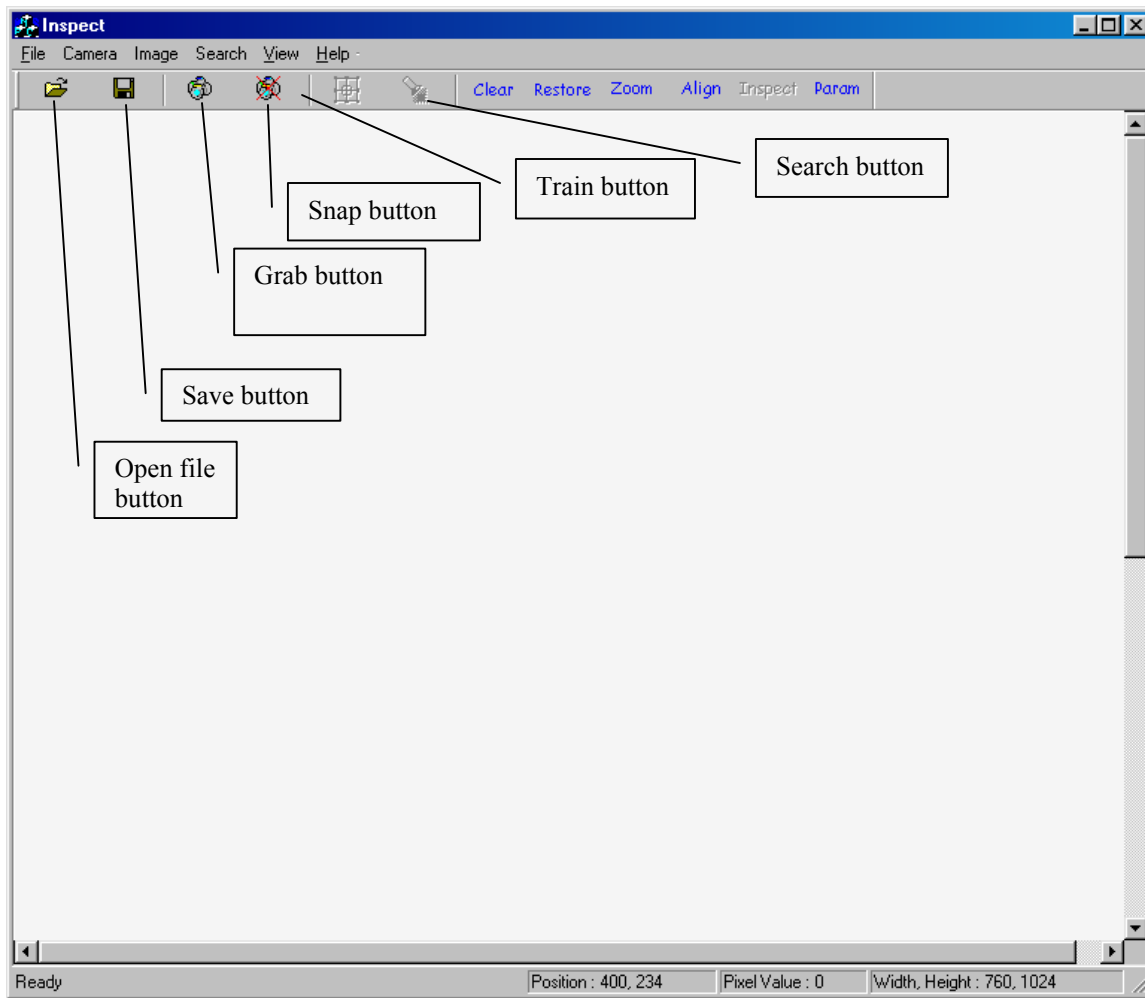


Figure 3.13: GUI for *Inspect*

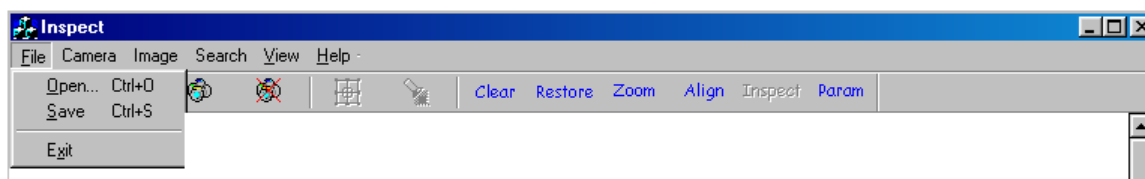


Figure 3.14: Operations available under *File* option. (See Table 3.2 for details)

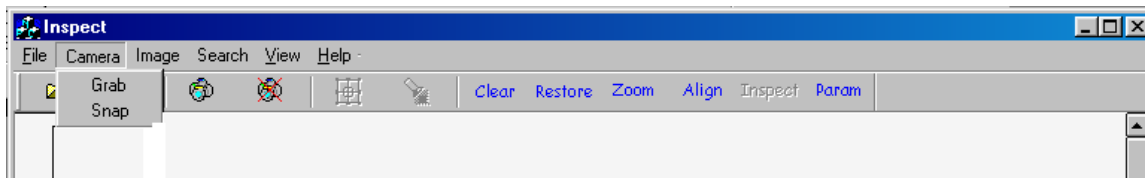
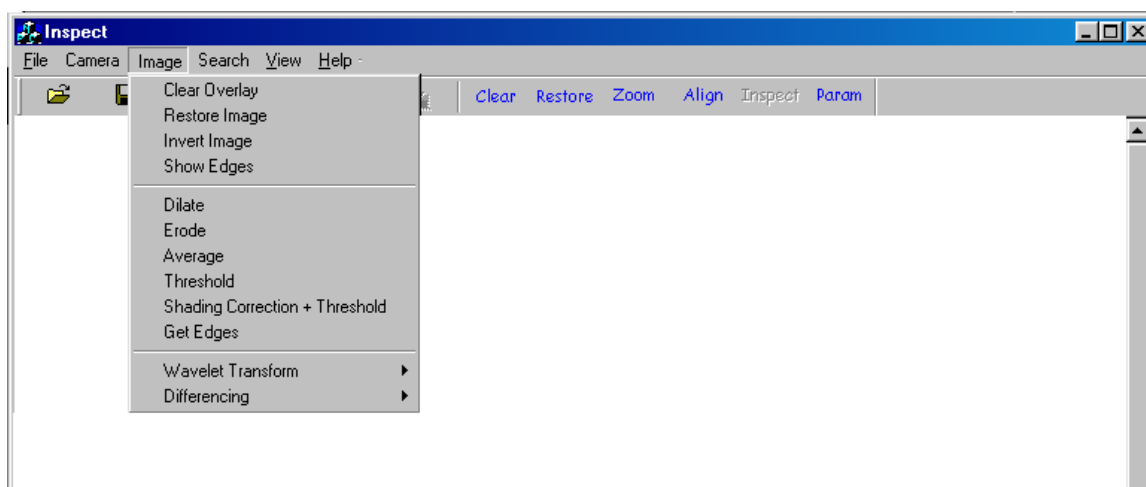


Figure 3.15: Operations available under *Camera* option. (See Table 3.2 for details)

Table 3.2: List of Main Buttons and Their Functions.

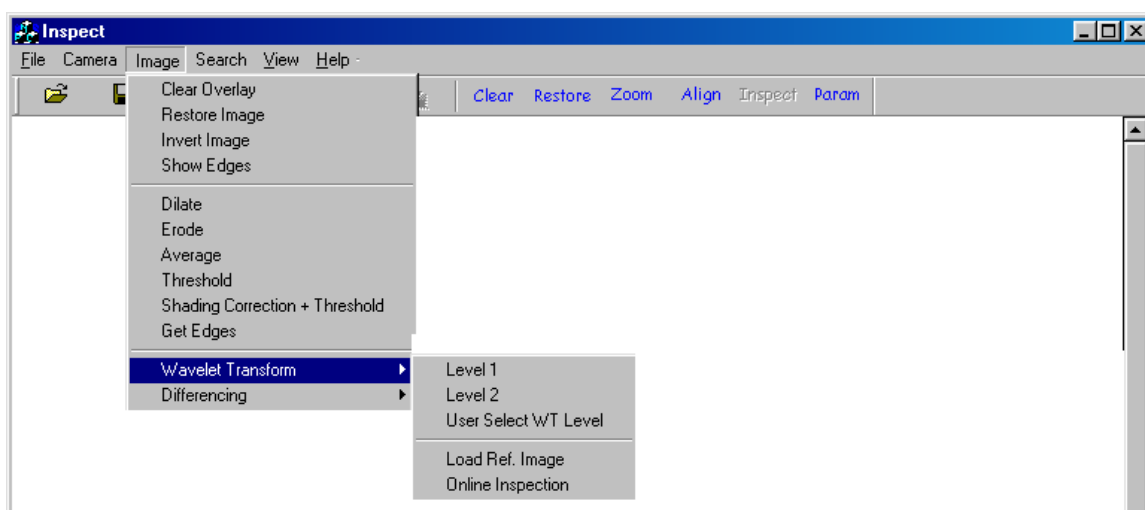
Button	Function
Open	To load an image file with .bmp format.
Save	To save current image in .bmp format
Grab	To show live image of the screen.
Snap	To freeze the live image on screen
Train	To train the selected pattern area as a reference point.
Search	To search the location of the trained pattern in the test image.
Clear	To clear the overlay graphics on the displayed image.
Restore	To redisplay the original image.
Zoom	To zoom in/zoom out the current image
Align	Not currently used
Inspect	To initiate automatic detection of the defect
Param	To pop up the parameter values so that user can change the default values

**Figure 3.16: Operations available under *Image* option**

The explanation for each submenus is given in Table 3.3 below.

Table 3.3: List of Image Submenu Buttons and Their Functions.

Button	Function
Clear overlay	Similar to <i>clear</i> button in Table 3.2.
Restore image	Similar to <i>restore</i> button in Table 3.2.
Invert	To show live image of the screen.
Show edges	To overlay all the edges onto the current image.
Dilate	To perform the dilate operation.
Erode	To perform the erode operation.
Average	To find the average value for the image.
Threshold	To threshold value set in the pop-up menu.
Shading correction	To perform the shading correction so that lighting is balanced throughout the image.
Get edges	Not currently used
Wavelet transform	To perform the wavelet transform. See Figure 3.19
Differencing	To perform the difference operator. See Figure 3.20

**Figure 3.17: Operations available under *Wavelet Transform* option.**

From Figure 3.17 above, *Level 1* option performs a first level wavelet transform, *Level 2* option performs a second level wavelet transform. *User Select* allows the user to

specify the desired level of wavelet transform. *Load Ref. Image* is to load the good image that will be the basis of comparison. *Online Inspection* is to perform the online wavelet transform plus differencing.

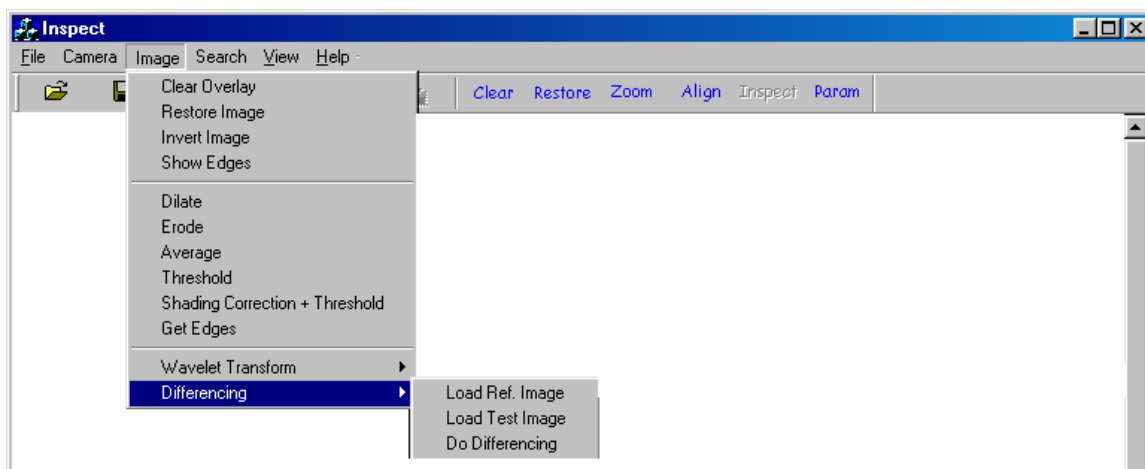


Figure 3.18: Operations available under *Differencing* option

From Figure 3.18 above, *Load Ref. Image* is to load an image that will be the reference from the differencing process. *Load Test Image* is to load a second image (test image) for differencing process. *Do Differencing* will perform the differencing process and show the result immediately on the screen.

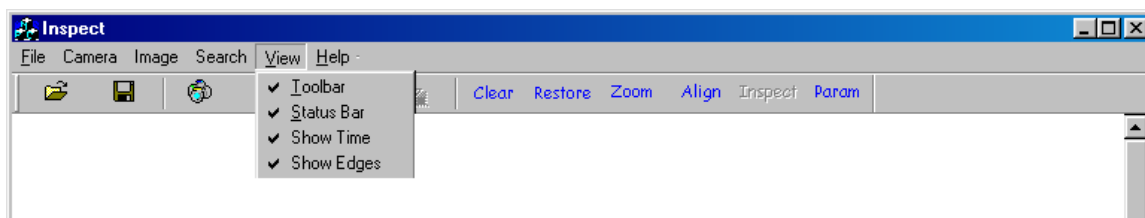


Figure 3.19: Operations available under *View* option.

The view submenu as shown in Figure 3.19 enables selected toolbars to be displayed on the main program. Once the selected item is checked, the associated toolbar will be displayed. Otherwise, information within the toolbar will be hidden.

3.7 Operational Flow of *INSPECT*

Inspect can be operated on either two modes: on-line and off-line modes. In the off-line mode, the program does not activate the frame grabber which connects to the CCD camera and thus no live images are taken. Instead, in this mode, the program is used to simulate the wavelet-based differencing operation using saved images. The other difference in the off-line mode is that the detection of the defect is done in a manual basis i.e. the user has to do several clicks of the mouse button to do the wavelet transform and the differencing (see Figure 3.17 and Figure 3.18). Figure 3.20(a) shows the operational flow on the off-line mode. In the on-line mode, the program activates the frame grabber and thus able to receive live images from the camera. The detection of the defect is activated simply by pressing the **inspect** button (see Table 3.2). Figure 3.20(b) shows the operational flow for the on-line mode.

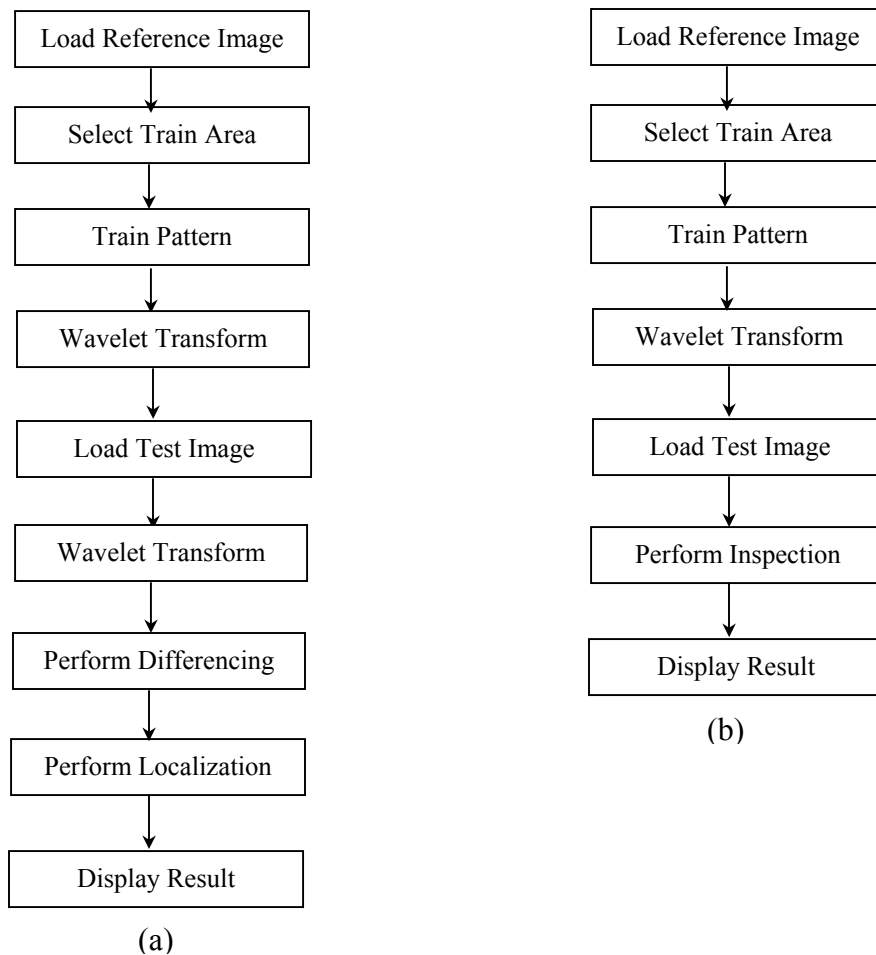


Figure 3.20: Operational flow for *Inspect* (a) Off-line mode (b) On-line mode

3.8 Example Using *Inspect*

The following example illustrates the use of *Inspect* in the off-line mode. First the reference image has to be loaded into the memory and 2nd stage Haar wavelet transform is applied (see Figure 3.21). Next, a reference template needs to be trained. This template serves as a reference point in the text image for aligning purpose before differencing takes place. The area is drawn by dragging the mouse pointer at the specified area (see Figure 3.22).

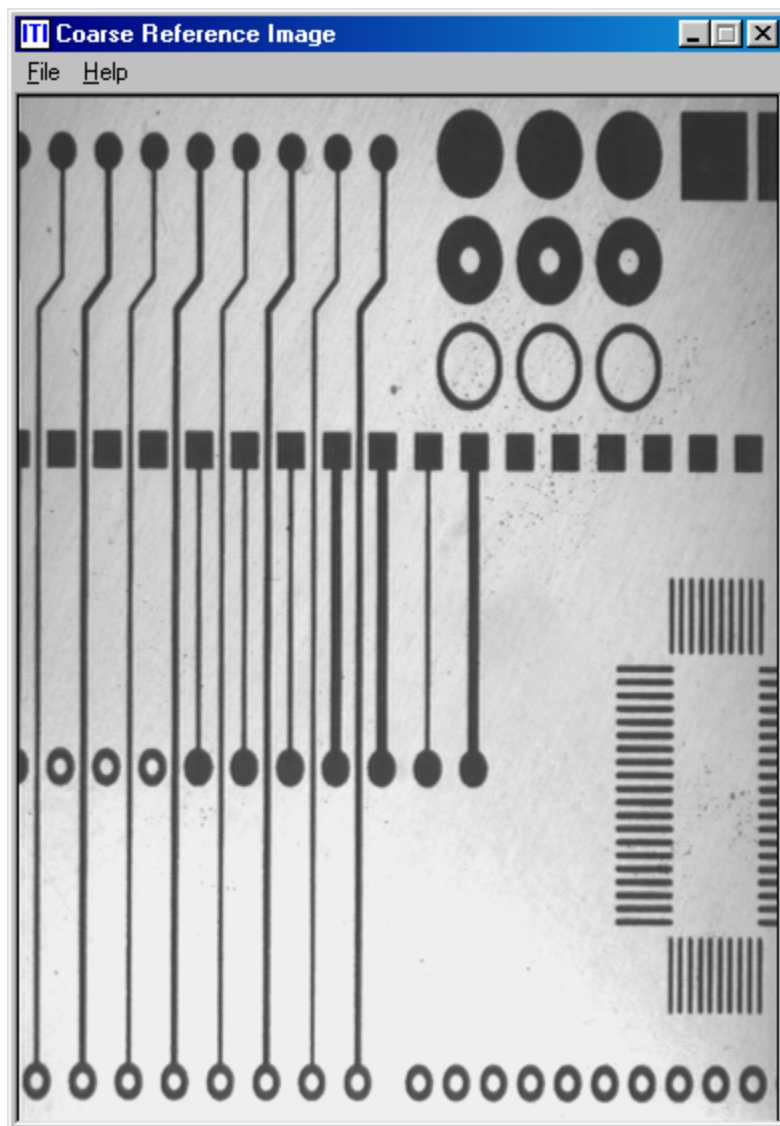


Figure 3.21: Coarse Reference Image

Once the area has been specified, the train button is pressed in order to complete the training process. This process is done only once to the reference image unless a new

reference image is used. Next the test image with defects will be loaded into the program and the 2nd stage Haar wavelet will be applied as shown in Figure 3.23.

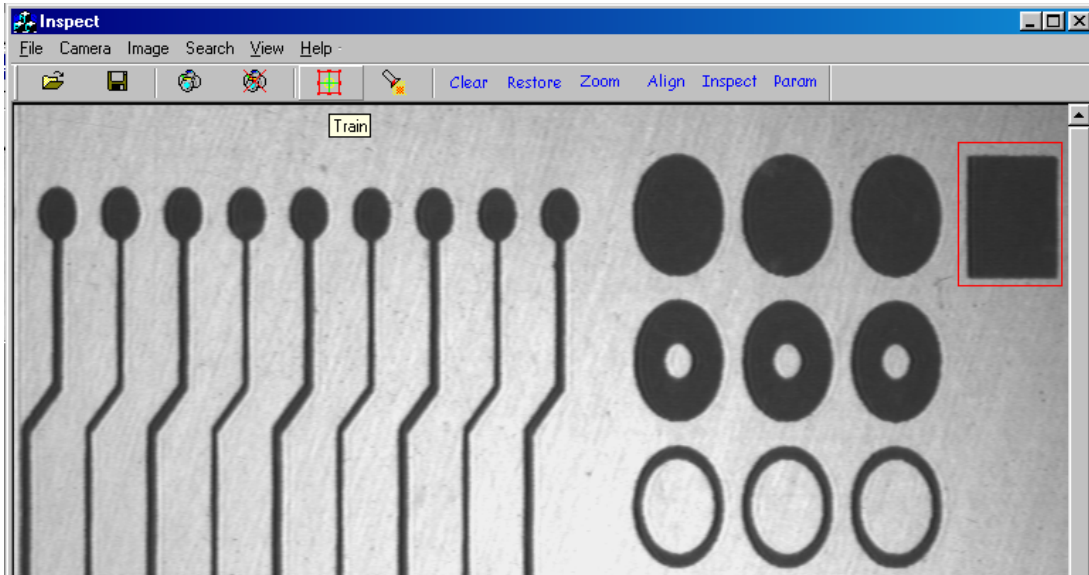


Figure 3.22: Training of the selected area marked by the red rectangle.

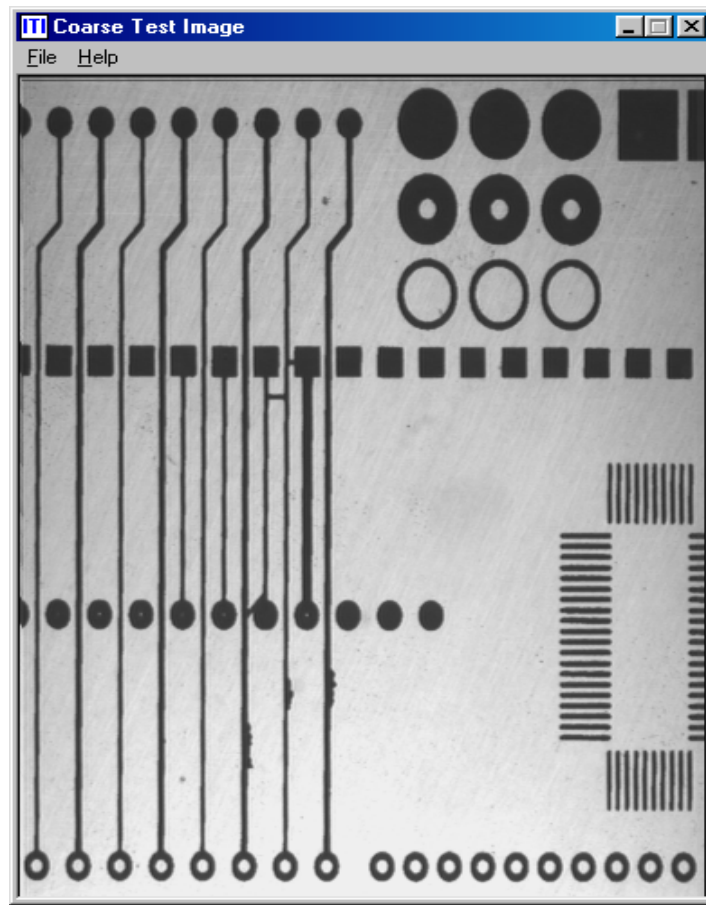


Figure 3.23: Test Image with Defects

The results on the wavelet transform, differencing, and localization are shown in Chapter 4.

3.9 Chapter Summary

This chapter has described the key algorithms in the defect detection i.e. wavelet transform and localization operations. In this project Haar wavelet has been utilized up to the second stage only. The main purpose of applying the wavelet transform is to reduce the image size while maintaining the content of the original image. As a result faster detection time has been achieved. The localization operation simply locates the detected defects by drawing a rectangle around the defects on the original image. Since the detection is done on a smaller (coarse) image, a mapping scheme to locate the actual position of the defect in the original (fine) image from the coarse image has to be done.

The second part of the chapter described the computer program developed to perform the PCB defect detection based on the main two algorithms above. *Inspect*, as the program is called, was developed using image processing libraries compiled under the C++ environment. This program has been programmed to run either in an off-line or on-line mode.

CHAPTER 4

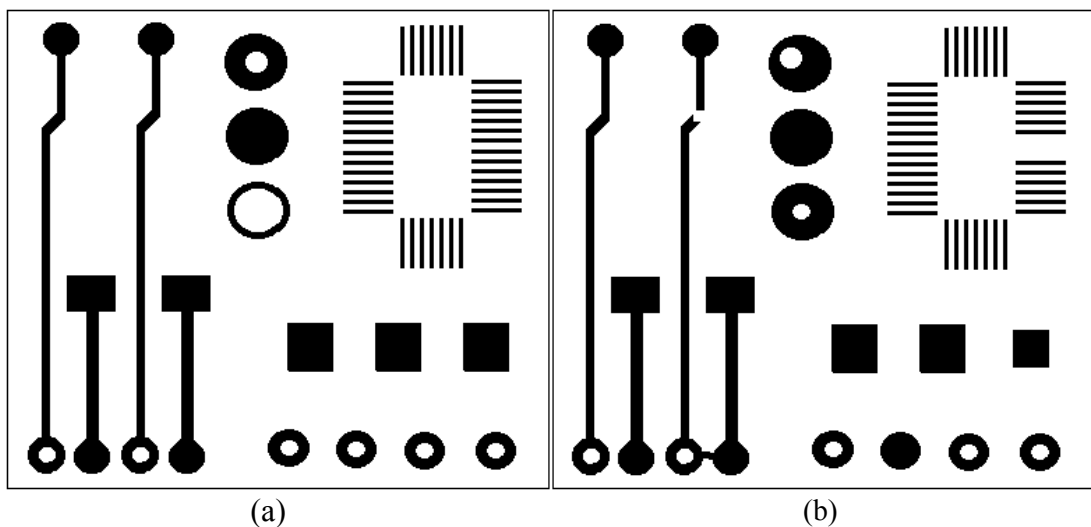
EXPERIMENTS AND PERFORMANCE ANALYSIS

4.1 Overview

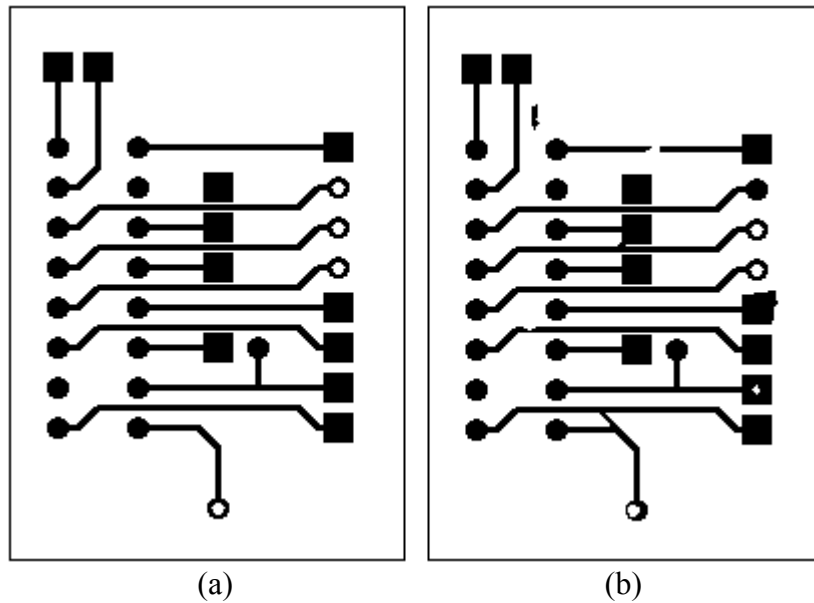
This chapter presents experimental results of this project. The findings are gathered based on some existing algorithms and also from the proposed wavelet-based PCB defect detection and localization algorithm. A number of different techniques and algorithms are analysed based on the following three major factors: defect detection, defect localization and inspection time. These three factors are considered in order to meet the objectives of this project. In order to give a fair comparison, MATLAB was used as the based software.

4.2 Experimentation

The machine used was an 800 MHz Pentium III computer with 256 MB memory. The proposed technique should be able to detect any one of the 14 types of defects defined in Chapter 1. Three different techniques are chosen for the evaluation. These are the image difference operation, RLE based image difference algorithm and the proposed wavelet-based technique. For the purpose of assessment, three different pairs of good and defective PCB images have been prepared as depicted in Figures 4.1, 4.2 and 4.3. These three figures representing various sizes of the PCB images, the number of defects and the shape of defects occurred.



**Figure 4.1: 400 x 400 sample 1 PCB image (a) Good PCB image
(b) Defective PCB image**

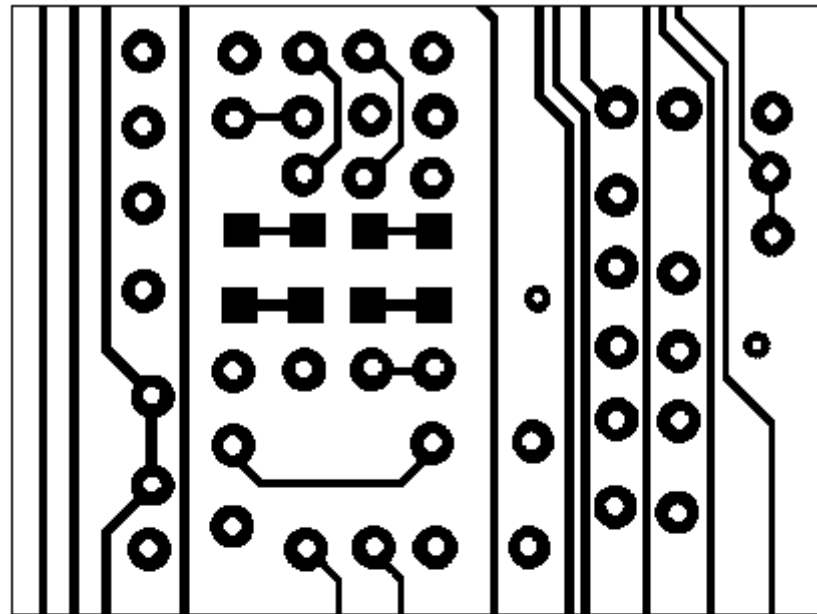


**Figure 4.2 : 280 x 200 sample 2 PCB image (a) Good PCB image
(b) Defective PCB image**

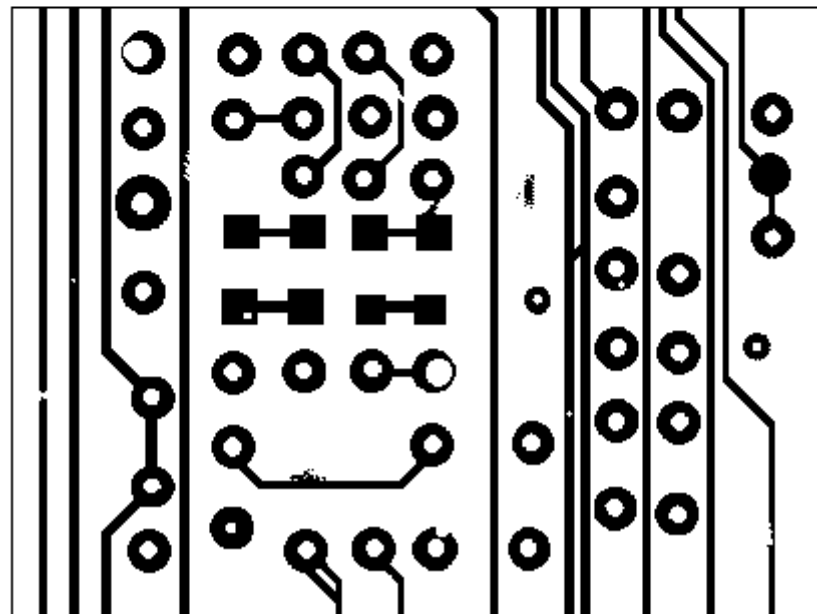
4.2.1 Image Difference

Image subtraction is the foremost step in the PCB inspection algorithm carried out by Wen-Yen et. al [12]. The way the input images are operated is similar to the image difference operation. In fact, image subtraction operation involves pixel-by-pixel scanning, same as image difference operation. Thus, image difference operation is considered for the assessment.

It is possible to detect the defects occur on the test PCB image by simply applying the image difference operation between the reference PCB image and the tested PCB image. Figures 4.4, 4.5 and 4.6 show the results of differenced image of the three different PCB samples. The defect localization results are also included. These results are obtained by the use of the defect localization algorithm as proposed in the Chapter 3. However, the computation is done on the fine resolution differenced image. As time is one of the industries major factors, it is essential to see the performance of the algorithm in term of inspection time of the full resolution image difference operation. The inspection time is given in Table 4.1.

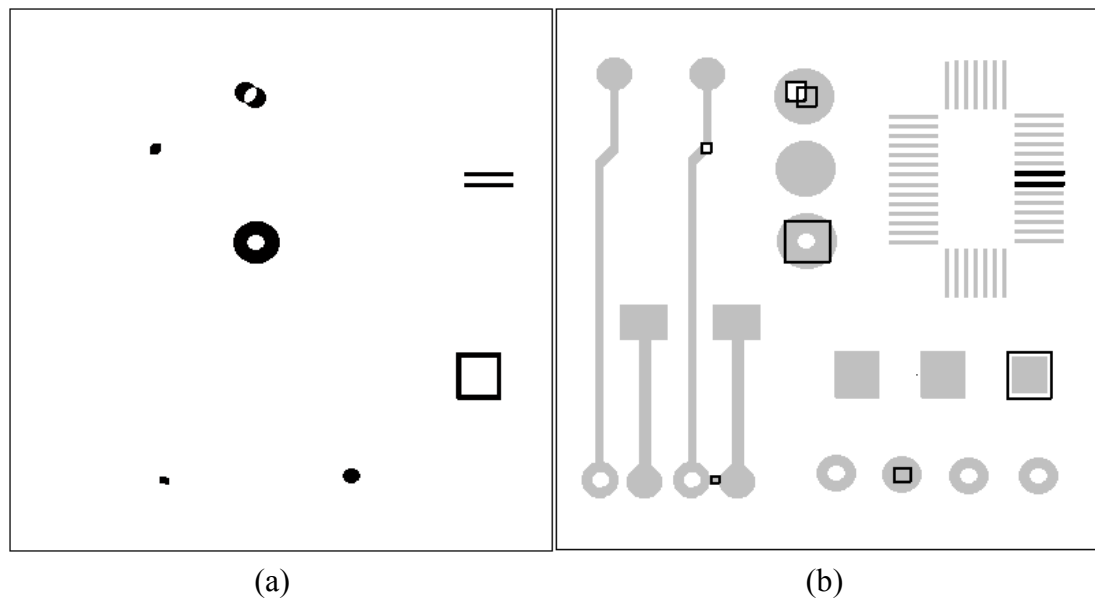


(a)

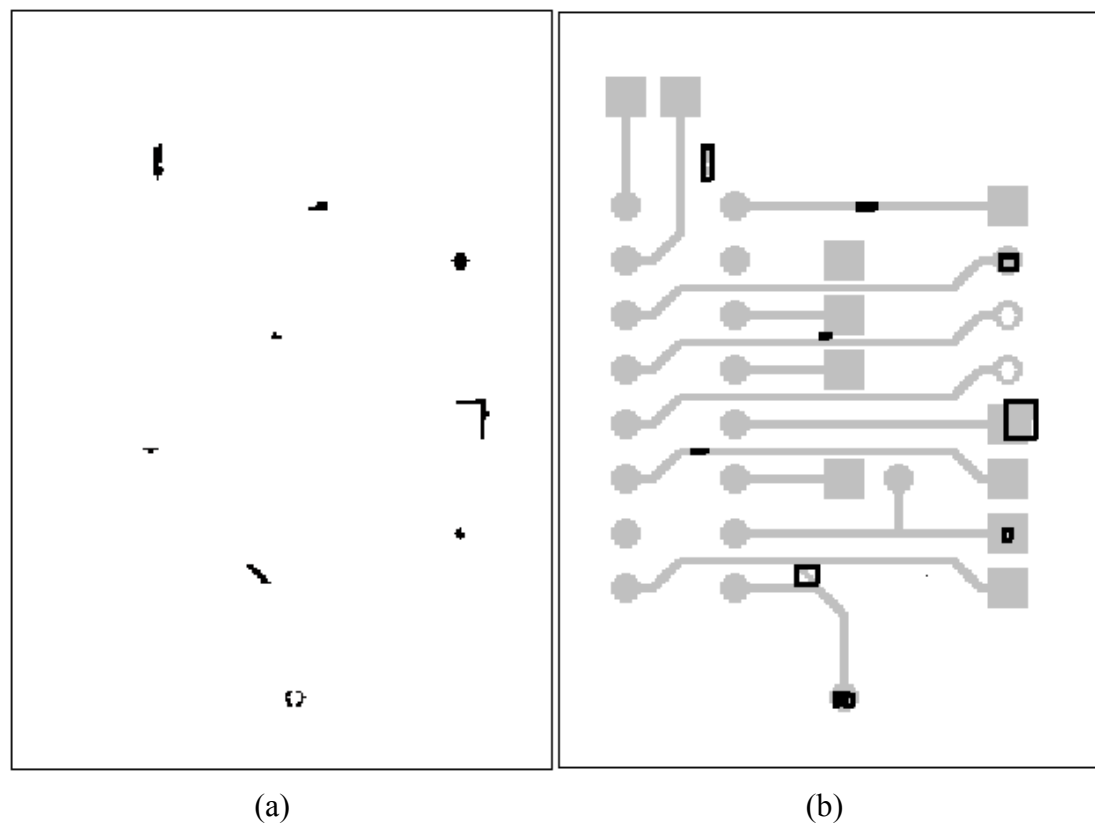


(b)

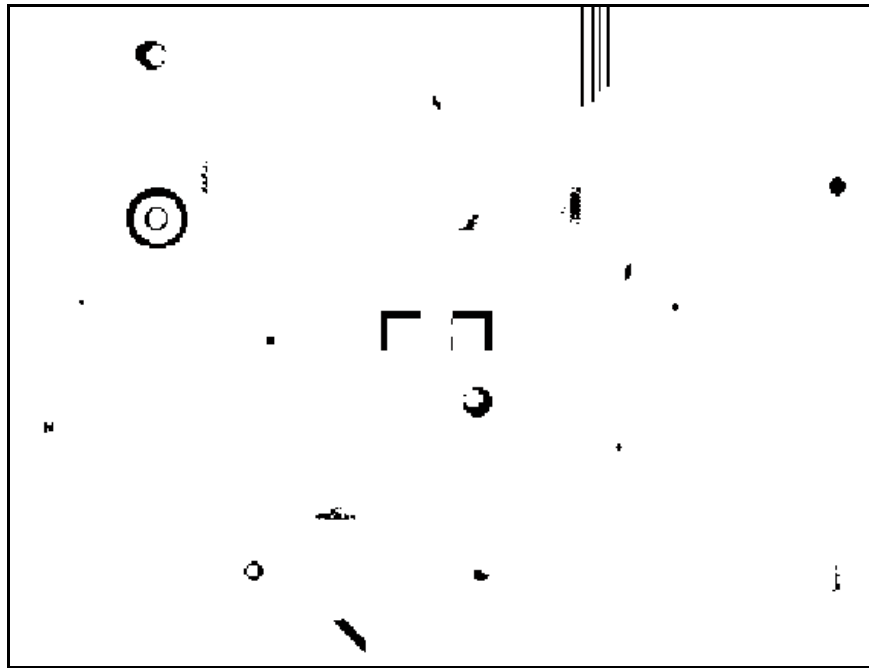
Figure 4.3: 304 x 400 sample 3 PCB image (a) Good PCB image
(b) Defective PCB image



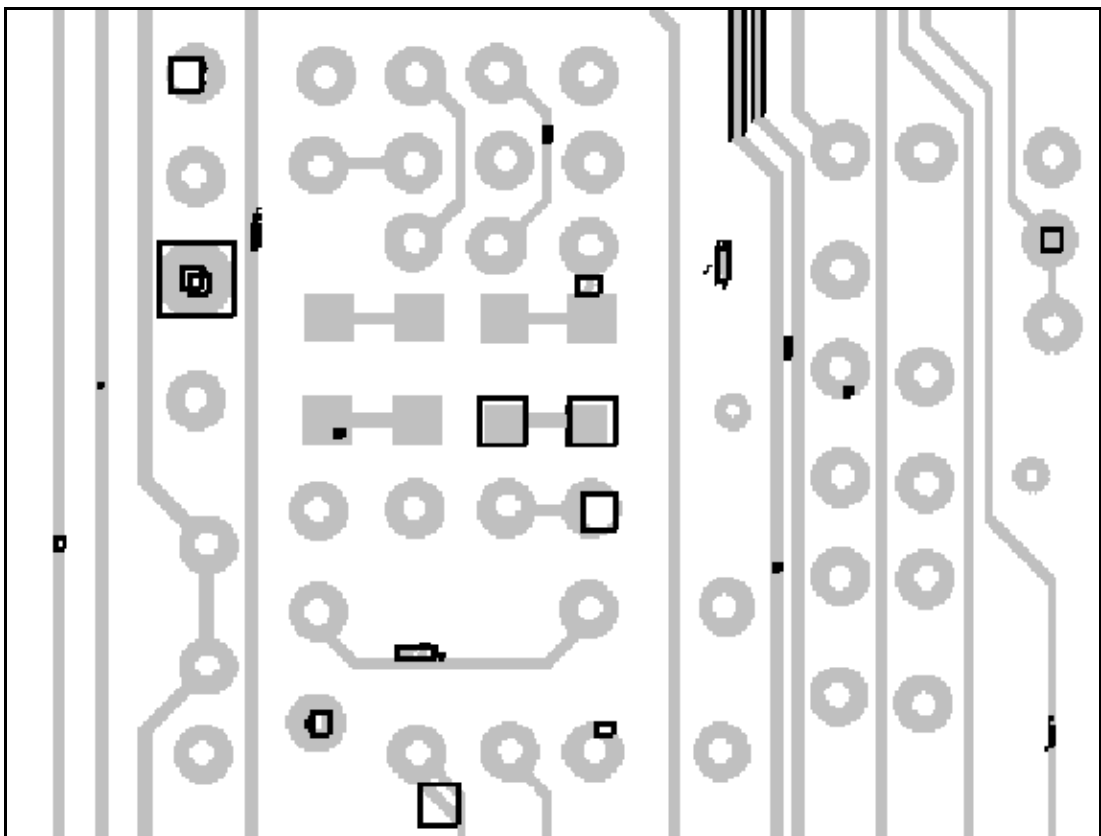
**Figure 4.4: (a) Fine resolution differenced image of the first sample PCB image
(b) Defects Localization based on (a)**



**Figure 4.5: (a) Fine resolution differenced image of the second sample PCB image
(b) Defects localization based on (a)**



(a)



(b)

**Figure 4.6: (a) Fine resolution differenced image of the third sample PCB image
(b) Defects localization based on (a)**

Table 4.1 : Inspection time of the full resolution image difference operation

Operation	Inspection time (s)		
	Sample 1 (400 x 400)	Sample 2 (280 x 200)	Sample 3 (304 x 400)
Read Input	00.020	00.020	00.030
Image Difference	07.251	02.784	06.359
Labelling	00.060	00.040	00.061
Window Coordinate Searching	17.846	08.182	57.421
Mapping And Windowing	00.050	00.010	00.080
Defect Extraction	00.812	01.070	03.924
Show Output	00.150	00.201	00.381
Total	26.189	12.307	68.256

4.2.2 RLE-based Image Difference Algorithm

Basically, as proposed by Ercal, et. al [21-23], the aim of the RLE-based image difference algorithm is actually to obtain the differenced image as achieved via pixel-by-pixel image difference operation. Except that, the image difference operation is done using RLE-based technique. Thus, the results of the RLE-based image difference operation should be similar to the results shown in Figure 4.4, Figure 4.5 and Figure 4.6. RLE-based image difference algorithm will not be tested. Instead, this work only obtains the time consumed by the bitmap to RLE conversion of tested PCB image as well as the RLE to bitmap conversion of differenced image in RLE domain. Table 4.2 below shows the conversion time of the RLE-based image difference algorithm when applied to the three samples of the PCB image.

4.2.3 Wavelet-based Image Difference Algorithm

The cost of processing with respect to computation time is dependent critically on the size of the input image. The aim of the wavelet-based PCB defect detection and localization is to minimize the inspection time related to the defect detection and localization algorithm. Hence, the wavelet-based technique is expected to give a better performance in term of inspection time due to the reduced size of the input image for defect detection and localization. The algorithm is done on the coarse images rather than on the original full resolution images. From the study

conducted it has been found that the 2nd stage wavelet transform is the optimum choice. Figure 4.7, Figure 4.8, and Figure 4.9 show the result of applying the 2nd stage wavelet transform to three images. The defects detection procedure is only applied for the coarse level processing. However, the defects localization should be highlighted on the original test image for better visual perception. Defects detected by the proposed algorithm are marked with black line on grey colour PCB traces. The inspection time for taking this transform is given in Table 4.3.

Table 4.2 : Conversion time of the RLE-based technique

Operation	Conversion time (s)		
	Sample 1 (400 x 400)	Sample 2 (280 x 200)	Sample 3 (304 x 400)
Bitmap to RLE conversion of tested PCB image	06.399	02.293	05.868
RLE to bitmap conversion of differenced PCB image	00.190	00.371	00.171
Total conversion time	06.589	02.664	06.039

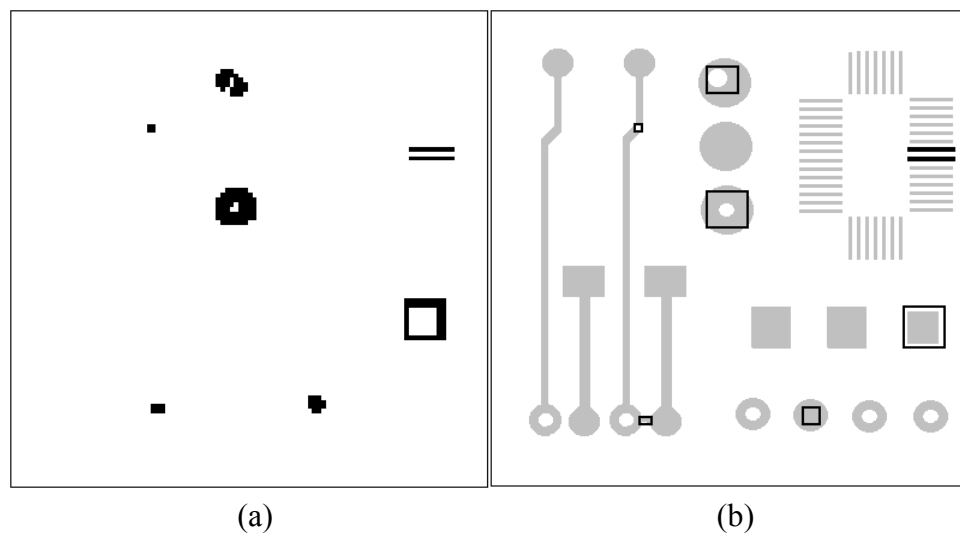


Figure 4.7: (a) Second level coarse resolution differenced image of the first sample PCB image (b) Defects localization based on (a)

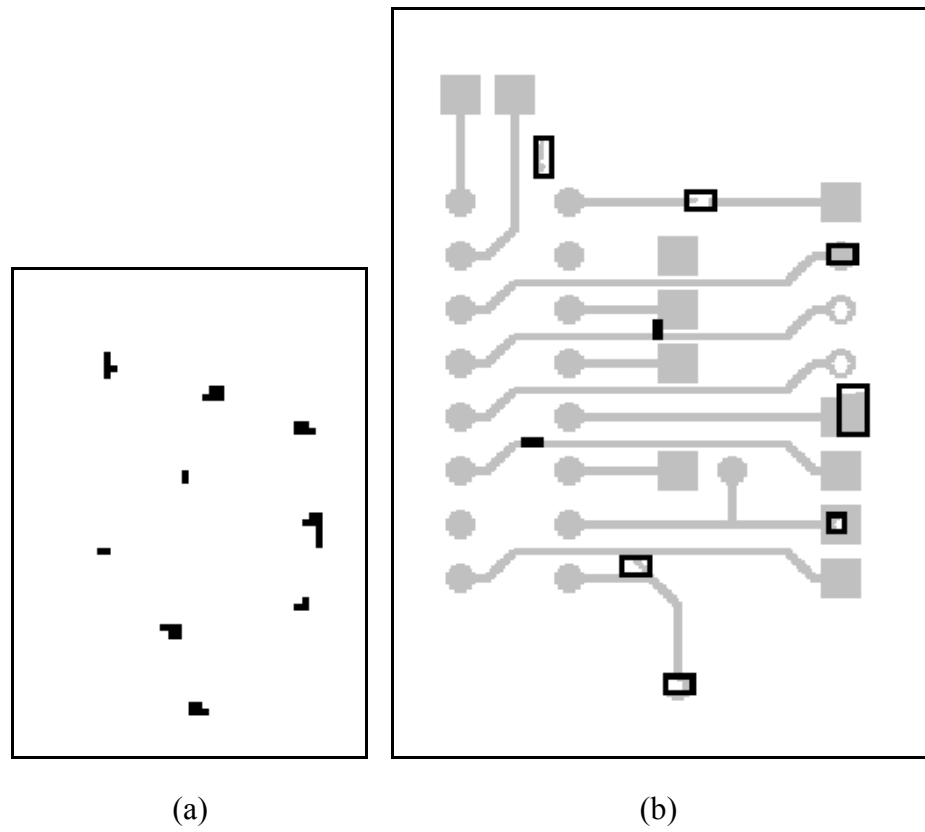
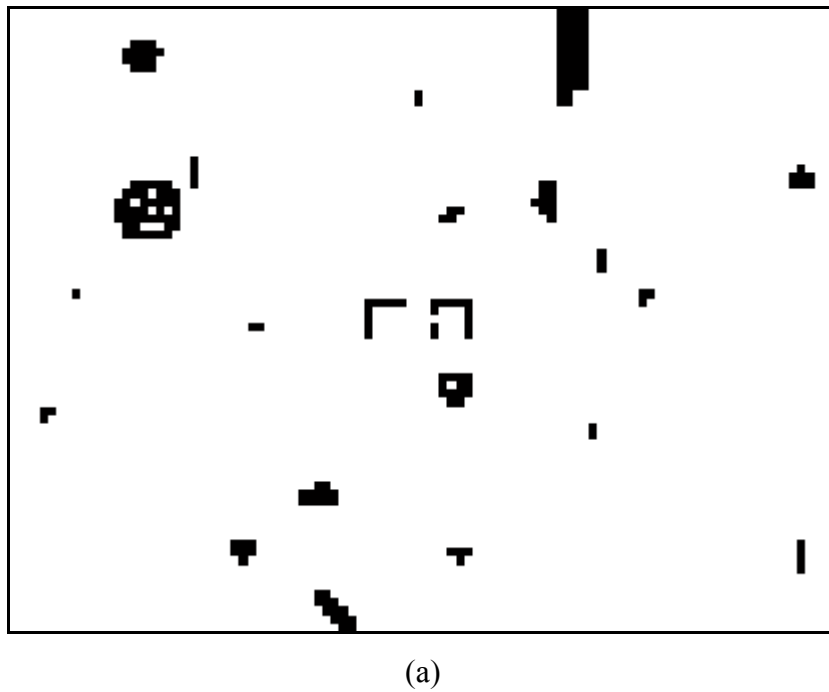
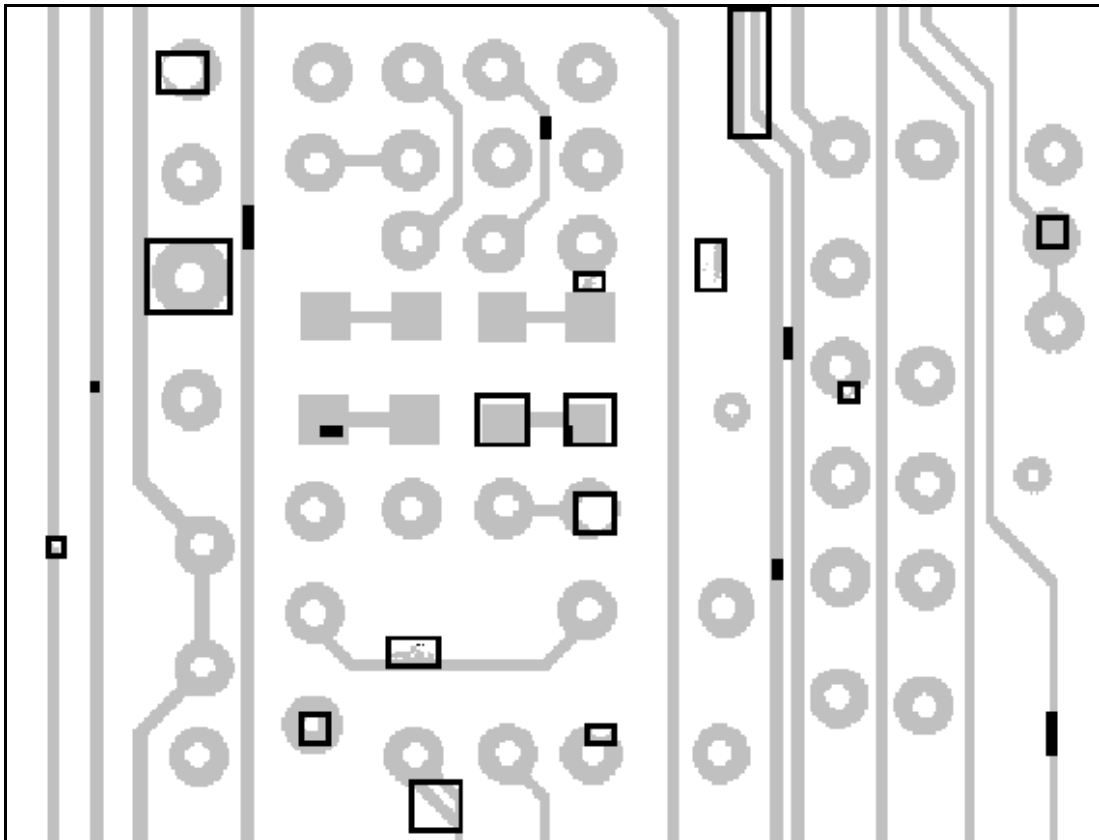


Figure 4.8: (a) Second level coarse resolution differenced image of the second sample PCB image (b) Defects localization based on (a)





(b)

Figure 4.9: (a) Second level coarse resolution differenced image of the third sample PCB image (b) Defects localization based on (a)

Table 4.3: Inspection time of the second level wavelet-based technique

Operation	Inspection time (s)		
	Sample 1 (400 x 400)	Sample 2 (280 x 200)	Sample 3 (304 x 400)
Read Input	0.030	0.010	0.030
Wavelet Transform	1.162	0.441	0.721
Image Difference	0.200	0.070	0.120
Labelling	0.020	0.020	0.020
Window Coordinate Searching	1.993	1.452	4.826
Mapping And Windowing	0.030	0.020	0.050
Defect Extraction	0.990	1.023	2.775
Show Output	0.261	0.220	0.250
Total	4.686	3.256	8.792

4.3 Result Using *Inspect*

To verify the result, the same test has been conducted using the *Inspect* software. Figure 4.10 shows the reference image while Figure 4.11 shows the test image with obvious defects.

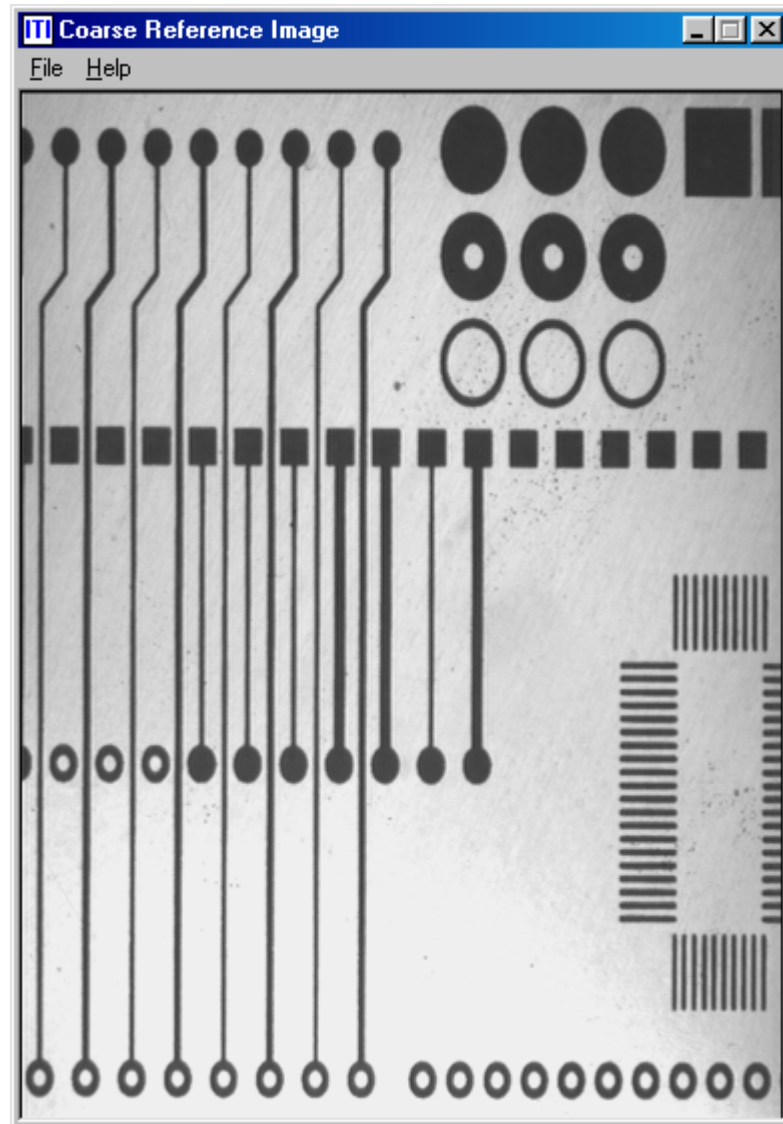


Figure 4.10: Reference Image (2nd Stage Wavelet Transform Applied)

The differencing will be done in such a manner that the positive output (those regions which exist in the reference image but not in the test image i.e. missing parts) will be separated from the negative output (those regions that do not exist in the reference image but appear in the test image i.e. unwanted parts). The reason for separating this result is to reduce the effect of noise in each individual output so that the overall output will have less noise when both positive and negative outputs are combined. Positive and negative outputs are shown in Figure 4.12 (with their pixel values reversed for printing purposes).

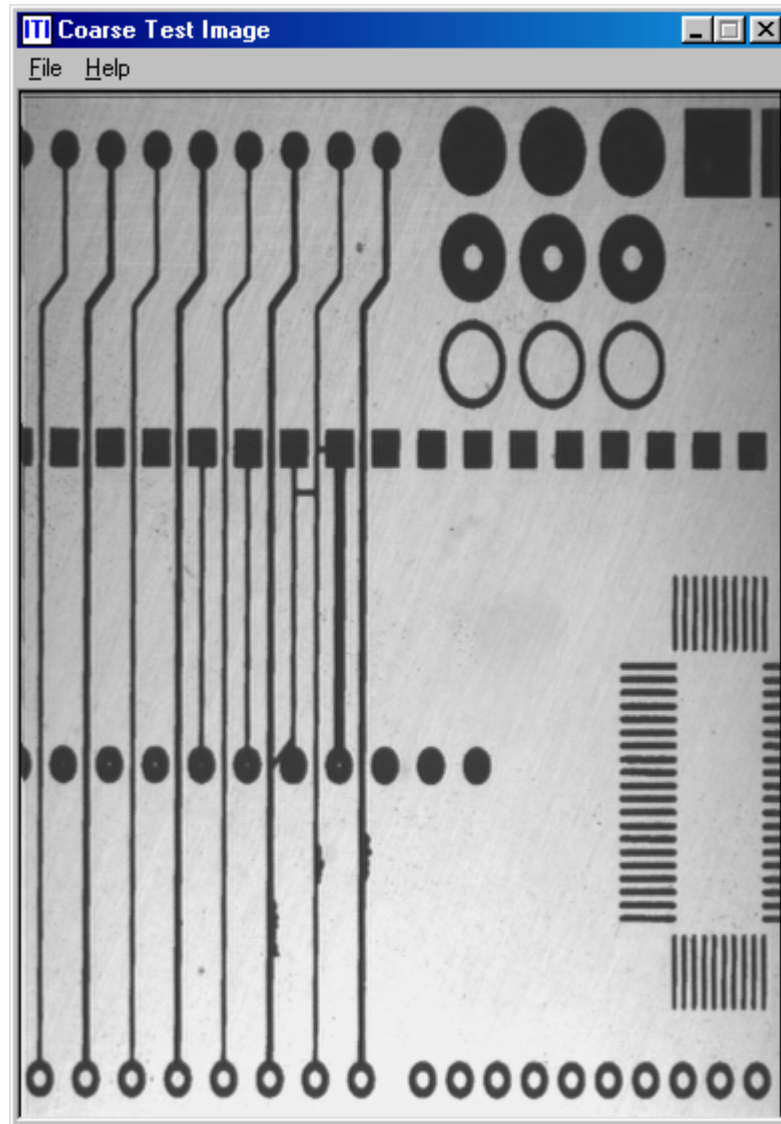


Figure 4.11: Test Image (2nd Stage Wavelet Transform Applied)

The combined result from the positive and the negative outputs is shown in Figure 4. 13. Once the overall result for image differencing has been obtained (in the coarse level), the localization operating will take place so that the defect will be highlighted on the fine (original) image. The location will be superimposed on the original image with a red marker as shown in Figure 4.14.

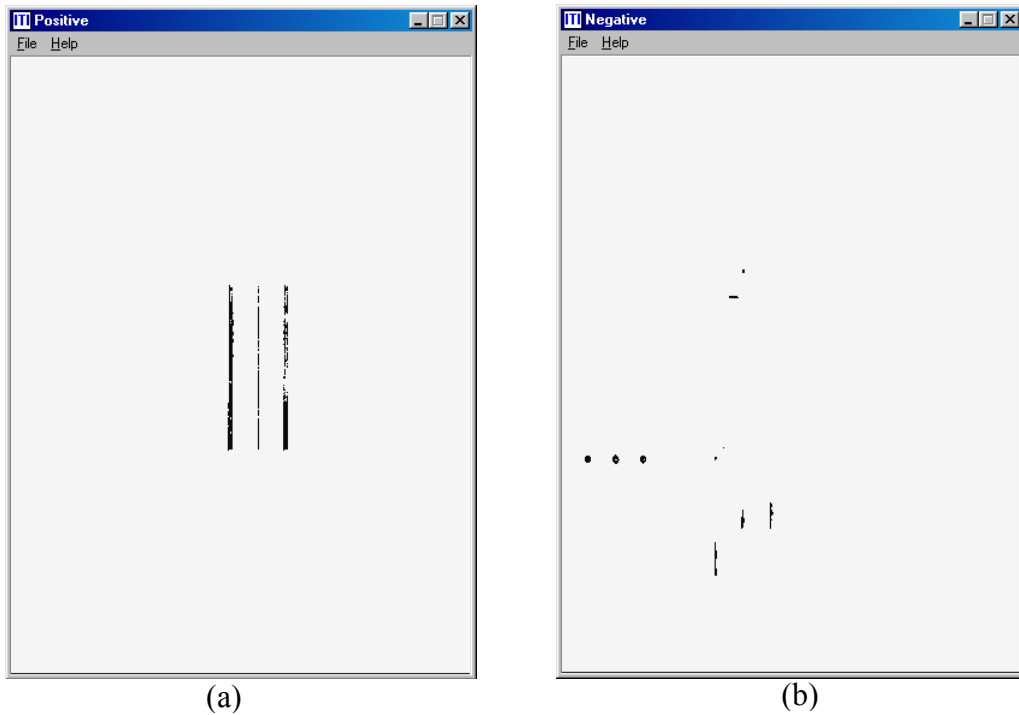


Figure 4.12: Differencing output (a) Positive values (b) Negative values



Figure 4.13: Combined Differencing result.

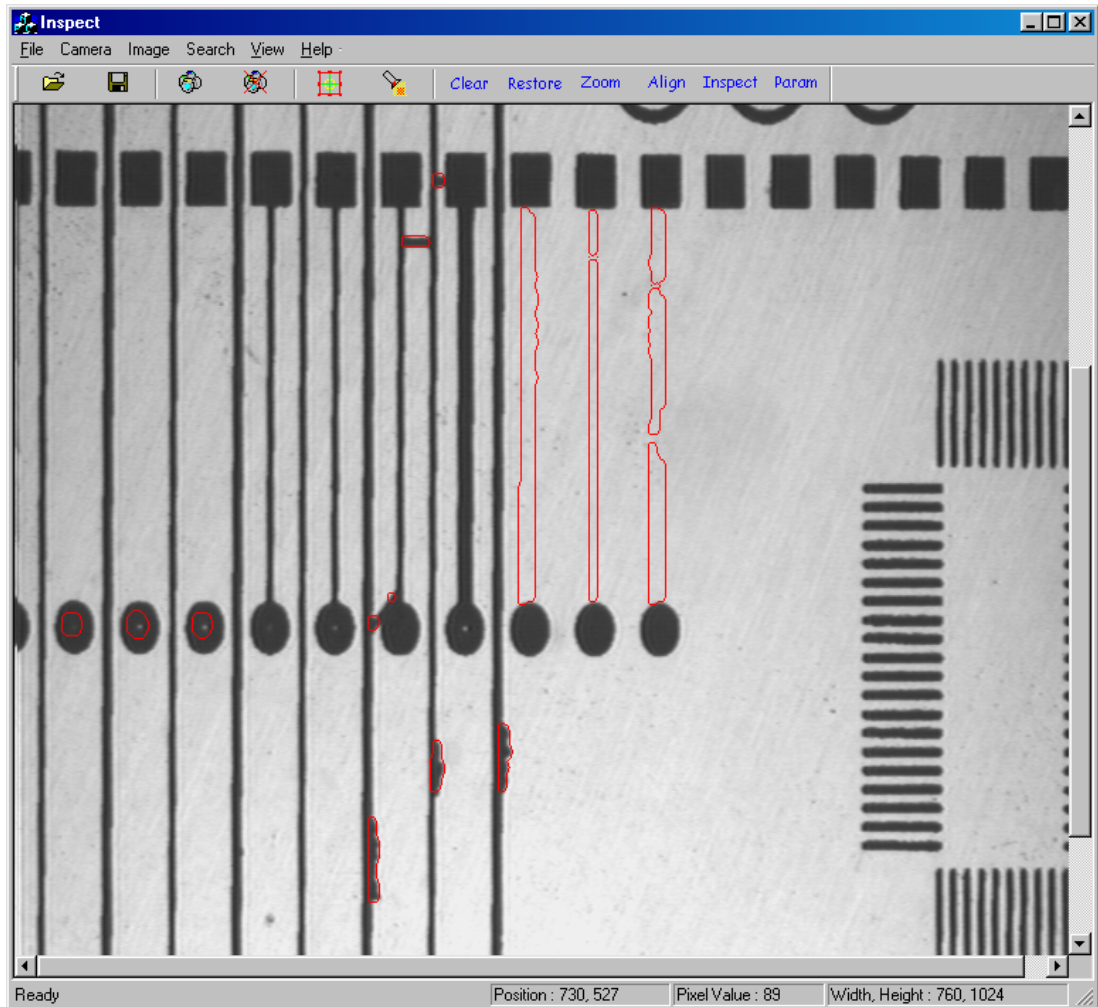


Figure 4.14: Detected defects highlighted on the original image

4.4 Discussions And Conclusions

From the proposed algorithm point of view, cost comparison between wavelet-based and non-wavelet processing with respect to time requirements suggests that wavelet-based processing provides considerable advantage over the non-wavelet one.

Due to these results, the proposed algorithm is expected to detect successfully several types the defects such as breakout, short, pin hole, wrong size hole, open circuit, conductor too close, underetch, spurious copper, mousebite, excessive short, missing conductor, missing hole, spur and overetch. The localized area in these figures will be used as the inputs to the classification stage, which is the subsequent stage after the defects detection had been achieved.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Overview

This chapter summarizes the work undertaken in accomplishing the project. The entire project has taken approximately two years to complete. As a consequence, some achievements have been attained during this period and they will be highlighted in this chapter. Towards the end of the chapter, some suggestions and recommendations for future work that can be carried out are proposed.

5.2 Conclusions

Automatic Search for PCB Defect Using Intelligent Vision System Based on DSP Technique is the project undertaken in this report. This project was funded by the Ministry of Science, Technology, and Environment under the program called IRPA (Intensified Research in Priority Area). The objective of this project is to come up with a faster and reliable detection of defects that could occur on a PCB (printed circuit board). There are two main algorithms designed for this purpose and they are wavelet-based differencing and defect localization.

After extensive research, finally a technique based on the current DSP technique has been formalized. The heart of the algorithm is the operation called the wavelet transform. In short, the wavelet transform reduces the size of the original image without significantly sacrificing the details of the image. This in effect has made the computation for defect detection at a faster speed to be possible. Since there are many functions that could be employed as the basis for the wavelet function, it has been shown in this report that Haar function was found to be the optimum. This function allowed the computation of the wavelet transform to be done in-place (simple averaging) with faster computation speed as compared to other wavelet functions. In addition, since the wavelet transform can be applied in a multilevel way i.e. employed repeatedly, it has been decided that the 2nd stage wavelet transform gives better performance. This 2nd stage wavelet is performed on the reference image (only once) and on the tested image before the differencing operation takes place.

Once the differencing operation is done, the output is then pass to the defect localization algorithm. The idea is to locate these defects on the PCB image so that these defects can be highlighted.

The general process towards defect detection can be summarized as follows:

1. Obtain the 2nd stage wavelet transform of the good sample PCB as this will be the reference image.
2. Acquire the test PCB image (in this project, a CCD camera using a frame grabber that is capable of acquiring 30 frames/sec was used).
3. Perform the 2nd stage wavelet transform on the acquired image. This is done on-line.
4. Using the approximation subimage perform the differencing operation between the 2nd stage reference image and the 2nd stage test image.
5. Employ the connected component labeling operation to identify the area of individual defect.
6. Employ the window coordinates searching operation to locate the exact location of the defects.
7. Employ the mapping operation to locate the actual defects location with respect to the original size of the image.

All the above operations have been programmed and compiled into a software program called *Inspect*. In addition to the above main processing, *Inspect* has been programmed to included the following functions in order to improve further the accuracy of the detection:

1. Translation: to align the acquired test image with that of the reference image. This process is also commonly known as image registration technique. The purpose of this registration is to ensure that differencing operation is done properly.
2. Signed differencing: there two parts in signed differencing. Instead of using the customary absolute differencing, positive differencing and negative differencing have been performed. Positive differencing will pick up those areas exist in reference image but not in tested image while negative differencing will pick up those areas exist in tested image but not in reference image. The idea of such differencing is to isolate unwanted noise.

3. Thresholding: this operation is done to the output of positive differencing and negative differencing so that isolated noise pixels are filtered away.
4. XOR-ing: the purpose is to combine the thresholded positive and negative differencing results. This result is then passed to the localization algorithm.

In conclusion this project has made its objective and has been implemented successfully. The next section describes the achievement that this project has gained.

5.3 Achievements

In undertaking this project, within the two years period, several papers (journal and conferences) have been published. These papers are listed below:

1. Zuwairie Ibrahim, Syed Abdul Rahman Syed Abu Bakar, Zulfakar Aspar, "Wavelet Based Algorithm for Image Comparison Technique in Application of Coarse-To Fine Inspection of Printed Circuit Board (PCB)", *Malaysian Science and Technology Congress on Physical Sciences and Engineering*, Melaka, Malaysia, Oktober 2001.
2. Z. Ibrahim, S.A.R. Al-Attas, Z. Aspar, "Analysis of the Wavelet-based Image Difference Algorithm for PCB Inspection", *Proceedings of the SICE Annual Conference (SICE 2002)*, Osaka, pp. 1525 – 1530, August 2002.
3. Zuwairie Ibrahim, Syed Abdul Rahman Al-Attas, Zulfakar Aspar and Musa Mohd Mokji, "Coarse Resolution Defect Localization Algorithm for an Automated Visual Printed Circuit Board Inspection", *28th Annual Conference of the IEEE Industrial Electronics Society (IECON 2002)*, pp 2629-2634 , Sevilla, Spain, November 5-8, 2002.
4. Zuwairie Ibrahim, Syed Abdul Rahman Al-Attas, Zulfakar Aspar and Musa Mohd Mokji, "Performance Evaluation of Wavelet-based PCB Defect Detection and Localization Algorithm", *2002 IEEE International Conference on Industrial Technology (ICIT 2002)*, pp. 226 – 231, Bangkok, Thailand, December 11-14, 2002.

5. Rudi Heriansyah, Syed Abdul Rahman al-Attas, and Muhammad Mun'im Ahmad Zabidi. "Decomposition of PCB Image into Basic Primitive Patterns using Morphological Operations" *Malaysian Science and Technology Congress 2002 (MSTC 2002)*, Malaysia, Sep. 19-21, 2002.
6. Zuwairie Ibrahim, Syed Abdul Rahman Syed Abu Bakar, Zulfakar Aspar, Rokhamsani Ghazali, "Performance Evaluation of Wavelet-based Algorithm for Printed Circuit Board (PCB) Inspection", *Jurnal Teknologi D*, Universiti Teknologi Malaysia (accepted for Publication)

In addition, this project has also won a bronze medal in the Science and Technology Exhibition held at Putra World Trade Center in Kuala Lumpur in year 2002. Figure 5.1 to Figure 5.4 shows some of the pictures used during the expo. Figure 5.1 and Figure 5.2 show the bare good PCB sample and the defective PCB sample respectively. Figure 5.3 shows on-line setup where the camera is scanning the defective PCB. The scanning is done with the help of synchronous red lighting. The close-up picture of the scanning PCB with the lighting is shown in Figure 5.4. Finally, Figure 5.5 shows the overall system setup with the programming running on the background.

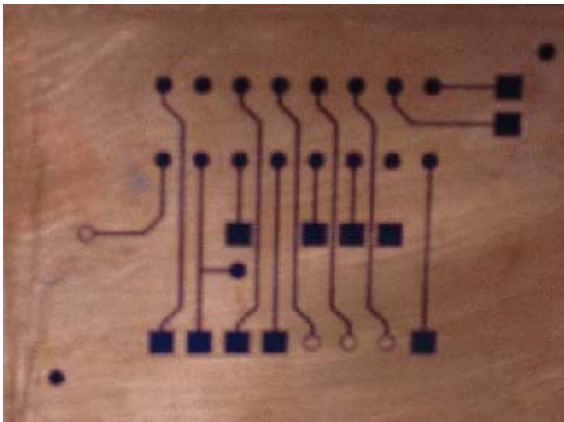


Figure 5.1: Good PCB sample

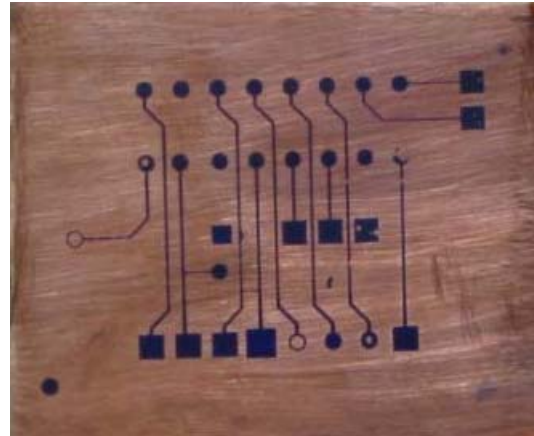


Figure 5.2: Defective PCB sample

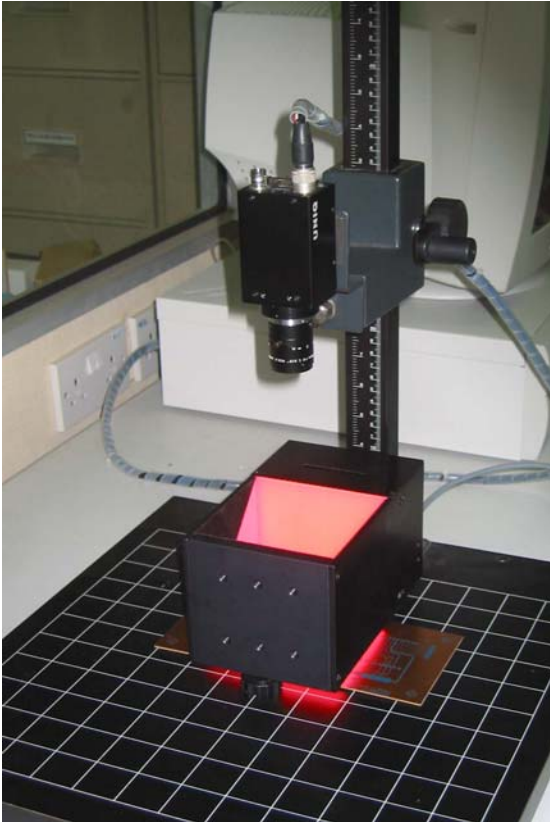
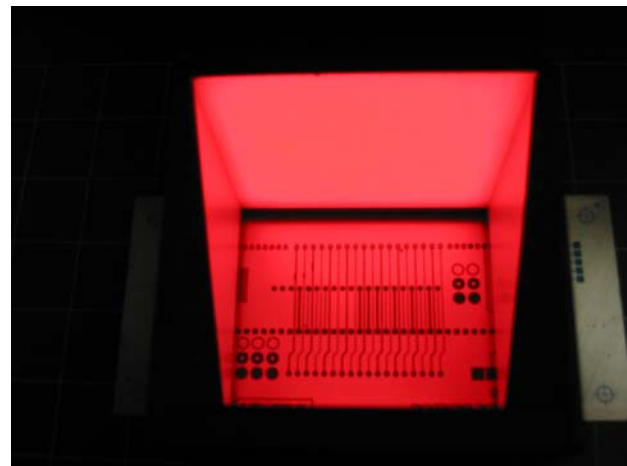


Figure 5.3: Scanning operation in progress. Synchronous lighting helps to improve the quality of the acquired image.

Figure 5.4: Close-up look in the scanning area.



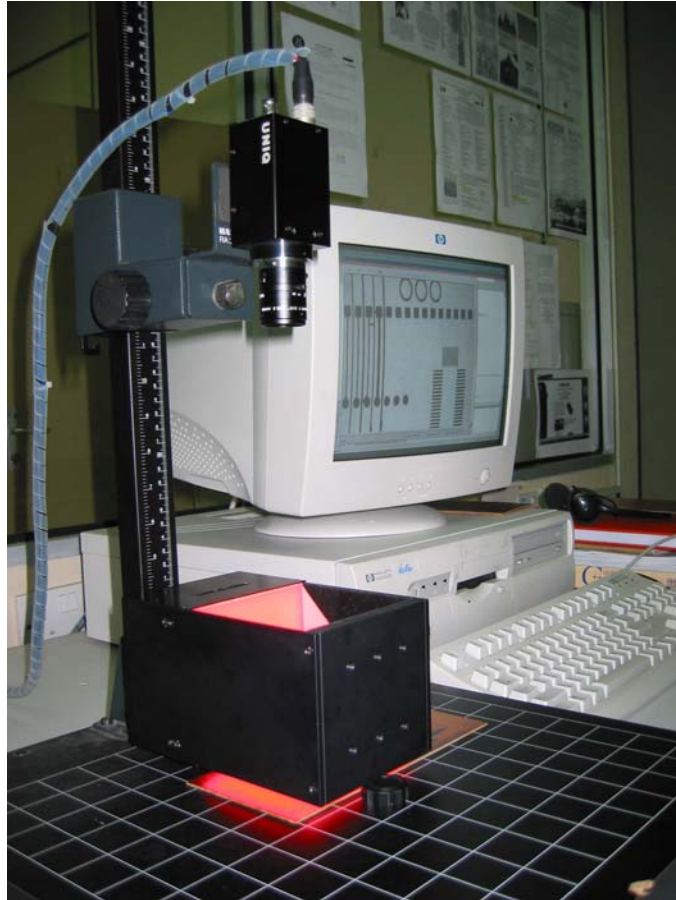


Figure 5.5 Overall setup for the inspection system

5.4 Recommendations

Even though this project has been completed successfully, it does not definitely mean that the PCB defect detection work is now over. In fact, this project has opened up many other doors of possible further research and experiments. One such area that is now being undertaken is in the area of defect classification i.e. identifying individual defect and classify them according to their class. Another possible area is in using multiple cameras so that larger area of PCB could be processed. This will then involve some coordination of cameras to be performed.

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