DESIGN AND DEVELOPMENT OF A STAND-ALONE MULTI-LEVEL INVERTER FOR PHOTOVOLTAIC (PV) APPLICATION

Report by:

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For

Research Vot No: 72342.

September 2003

ABSTRACT

Multilevel voltage source inverter (VSI) has been recognized to be very attractive in high voltage dc to ac conversion. It offers several advantages compared to the conventional two-level inverter, namely reduced switching losses and better harmonic performance. This work proposed a new switching strategy for a particular multilevel topology, known as the modular structured multilevel inverter (MSMI). The proposed scheme is based on symmetric regular sampled unipolar PWM technique. Unlike other techniques proposed by other researchers, this method uses multiple modulating waveform with a single carrier. Mathematical equations that define the PWM switching instants is derived. The derived equations are verified by computer simulation. To justify the merits of the proposed modulation scheme, prediction on the output voltage harmonics using Fourier analysis is carried out. An experimental five-level MSMI test-rig is built to implement the proposed algorithm. Using this set-up, it was found that the derived equations could be easily implemented by a low-cost fixed-point microcontroller. Several tests to quantify the performance of the inverter under the proposed modulation scheme is carried out. The results obtained from these tests agree well with theoretical prediction.

(*Keywords: inverter, power electronics, pulse-width modulation, multilevel*)

ABSTRAK

Penyongsang sumber voltan (VSI) bertahap diiktiraf amat sesuai digunakan dalam penukaran voltan tinggi DC ke AC. Ia memberikan beberapa kelebihan berbanding penyogsang dua tahap di mana kehilangan pensuisan dan harmonik dapat dikurangkan. Tesis ini mengusulkan satu strategi pensuisan untuk satu topologi penyongsang bertahap yang dikenali sebagai penyongsang bertahap struktur bermodul (MSMI). Skim pemodulatan ini adalah berasaskan teknik PWM satu kutub tersampel teratur simetri. Tidak seperti teknik yang diusulkan oleh penyelidik-penyelidik sebelum ini, kaedah ini menggunakan beberapa gelombang memodulat beserta isyarat pembawa tunggal. Hasilnya, satu persamaan matematik sesuai untuk pelaksanaan digital bagi skim tersebut diterbitkan. Persamaan yang diterbitkan itu ditentusahkan oleh simulasi komputer. Bagi menentukan kelebihan skim pemodulatan tersebut, telahan awal terhadap harmonik voltan keluaran mengunakan analisis Fourier telah dilakukan. Selanjutnya satu modul eksperimen untuk penyongsang lima-tahap struktur bermodul telah dibina untuk pengimplementasian algorithma yg diusulkan. Daripada ujikaji yang telah dijalankan, didapati bahawa persamaan yang diterbitkan dapat diiplementasikan secara digital dengan mudah menggunakan pengawal mikro berkos rendah. Beberapa ujian untuk mengenalpasti persembahan penyongsang menggunakan skim pemodulatan tersebut telah dilakukan. Didapati bahawa keputusan yang diperolehi disokong oleh teori.

Katakunci: penyongsang, elektronik kuasa, penyongsang berbilang tahap, pemodulatan lebar denyut

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CHAPTER I

INTRODUCTION

1.1 Overview

The past decade has witness the growing interest in alternative sources of energy [1-5]. The so-called renewable energy such as the sun, geothermal, biomass and wind can never be exhausted. They cause less emission and therefore stand out as a potentially viable source of clean and limitless energy. However these renewable sources energy—in particular the solar energy, requires rather sophisticated conversion techniques to make them usable to the end user. For example, the output of the photovoltaic (solar) panel is essentially dc; for it to be commercially viable, it needs to be converted to ac. This is necessary because the power utilisation is mostly in ac form. The technology to accomplish this conversion—known as inverter, is inevitably an integral part of the photovoltaic system.

Technology-wise, inverter can be divided into two main types; Voltage Source Inverters (VSI) and Current Source Inverters (CSI). Both types have their own advantages and disadvantages and are reported extensively in literatures [6-9]. However VSI is more popular compared to CSI, especially in renewable energy system [6,7]. Several research works [8-12] have concluded that the transformer-less inverter is very attractive in renewable energy application due to reduced weight and size. In principal, a two-level PWM inverter with high switching frequency can be adequately used, but for high power application the switching losses can be prohibitive [13].

A large body of literature over the past decade has testified multilevel inverter viability especially for high power application [14-17]. Multilevel inverter has become an effective and practical solution for reducing switching losses in high power application. Recently several multilevel topologies have become very popular in renewable energy sources applications [18-19]. It is well known that multilevel voltage source inverters offer several advantages compared to their conventional counterparts. By synthesizing the ac output terminal voltage from several levels of

dc voltages, staircase output waveform can be produced. This allows for higher output voltage and simultaneously lowers the switches voltage stress. In addition, multilevel inverter is known to have better harmonic profile and thus the requirement of output filter is reduced.

Generally the development of multilevel inverter system can be broadly divided into the two issues namely, power circuit topology and switching strategy. For circuit topology, three main types have been frequently cited in literature: (1) diode-clamped multilevel inverters (DCMI): (2) flying capacitor multilevel inverters (FCMI) and (3) modular structured multilevel inverters (MSMI). Abovementioned topologies have their specific advantages and disadvantages as detailed in [20-23]. The selection of appropriate topology depends on a particular application and the nature of the dc supply that feed the inverter.

The second aspect that defines the inverter performance is the switching strategy. This is closely related to the harmonic profile of the inverter output waveform. The simplest scheme is the square wave, which has the poorest harmonic performance. This is followed by quasi-square wave, which offers a marginal improvement compared to the square wave inverter. The most popular switching technique is the Pulse Width Modulation (PWM), which is currently being implemented in majority of the VSIs.

Historically, the development of PWM switching strategy was prompted by the natural sampled sinusoidal PWM technique introduced by Schonung and Stemmler in 1964 [25]. This analog technique is based on the physical comparison between a carrier signal and a pure sinusoidal modulating signal. Its digital version, i.e. the regular-sampling PWM was introduced by Bowes in 1975 [26]. It has simplified the PWM generation tremendously and has become the impetus for the proliferation of several important digital PWM techniques until the present day. Several currently popular PWM schemes are the Optimized PWM [26], Selective Harmonic Elimination PWM (SHEPWM) [27-28] and more recently the Space Vector PWM (SVPWM) [29-33].

Abovementioned modulation techniques were originally applied to the two-level inverter. However, it was discovered that by making some modifications they could also be suitably used for multilevel inverter. For multilevel sinusoidal PWM in particular, different methods of carrier arrangement namely Phase Opposition Disposition (POD), Phase Disposition (DP) and Alternatively in Phase Opposition Disposition (APOD) [20] have been suggested. All of these techniques employ multiple carriers with a single modulating waveform. Each method has its own unique spectra and specific applications [33-36]. In brief, the heart of any multilevel inverter is the selection of the power circuit topology and its associated switching strategy. The power circuit topology is dictated by a particular application and the nature of the dc supply that feed the inverter. The switching strategy will determine the harmonic performance of the output voltage waveform.

1.2 Objective of Research

As noted in the brief overview above, multilevel inverters have been used in power electronic applications for over a decade. Judging from the proliferation of literature in this subject, undoubtedly, research in this area is still very active. It triggers a lot of interest, particularly with the up-trend of the renewable energy resources.

Research efforts in this area have contributes toward the development of several PWM schemes suitable for multilevel inverter application. Fundamentally, the choice of the PWM scheme will influence the complexity and performance of the inverter system. In this work the research will be focused on developing a new switching algorithm for the modular structured multilevel inverter. It will be based on the popular regular sampling PWM. Mathematical derivation will be carried out to obtain switching instants that can be programmed using a C167 microcontroller. A harmonic analysis is carried out to justify the performance of the inverter under the proposed switching strategy. In order to validate the performance of the inverter, a low-power test-rig will be constructed. The performance of the inverter is analysed and compared with the result obtained from theory and simulation.

CHAPTER II

NOVEL TECHNIQUE FOR PWM WAVEFORM GENERATION FOR MULTILEVEL INVERTERS

2.1 Review of Conventional Voltage Source Inverter

Switch-mode dc-to-ac inverter is used in ac power supplies and ac motor drives with the objective to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. In single-phase or three-phase ac systems there are two common inverter topologies used. First is the half-bridge or a single leg inverter, which is the simplest topology, as shown in Figure 2.1. It is used to produce a two-level square-wave output waveform using two semiconductor switches S_1 and S_2. A center-tapped voltage source supply is needed; it may be possible to use a simple supply with two well-matched capacitors in series to provide the center tap. Another topology is known as the full-bridge inverter. It is used to synthesize a two-level or three-level square-wave output waveform but with double the amplitude compared to half-bridge. There are two inverter legs in a full-bridge topology as shown in Figure 2.2, namely leg *a* and leg *b*.

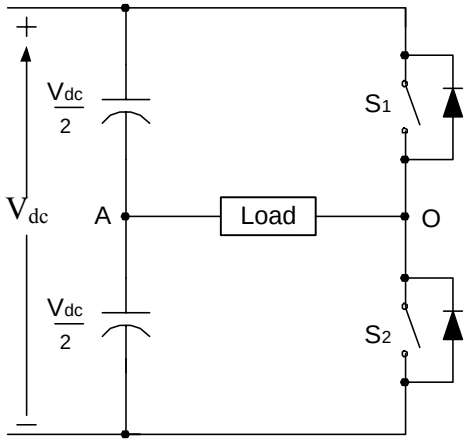


Figure 2.1: Half-bridge configuration.

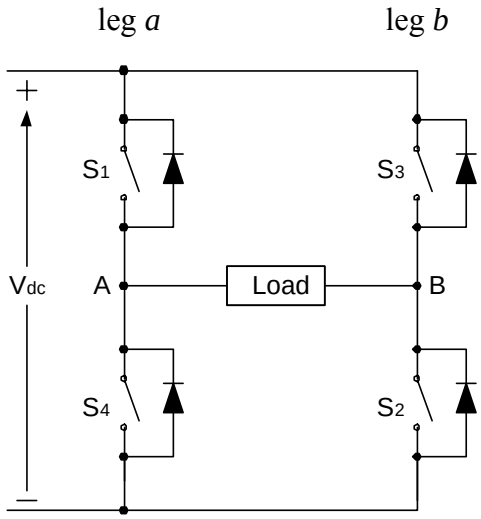


Figure 2.2: Full-bridge configuration.

For each inverter leg, the top and bottom switches have to be complementary to avoid shoot-through fault, i.e. if the top switch is closed (on), the bottom must be open (off), and vice-versa. Both switches, S_1 and S_2 for half-bridge inverter are never turned on at the same time. Similarly for full-bridge inverter, both S_1 and S_4 should not be closed at the same time, nor should S_2 and S_3. To ensure the switches not closed at the same time, each gating signal should pass through a protection mechanisme known as a "dead time" circuit before it is fed to the switches gate [46,47]. A two-level output waveform of half bridge and three-level output waveform of full bridge single-phase voltage source inverter are shown in Figure 2.3 and 2.4, respectively.

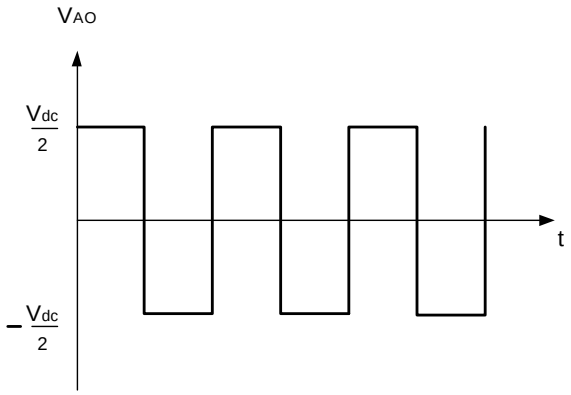


Figure 2.3: Two-level output waveform of half-bridge configuration.

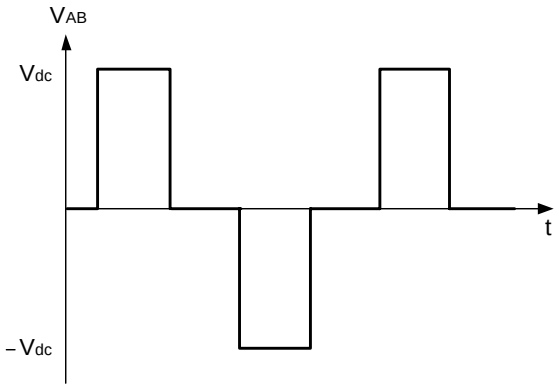


Figure 2.4: Three-level output waveform of full-bridge configuration.

2.2 Multilevel Inverters Topologies

Multilevel voltage source inverter (MVSI) is very attractive in high voltage and high power applications such as adjustable speed drives and electric utility applications. The development of MVSI began in the early 1980's when Nabae et al. [39] proposed a neutral-point clamped (NPC) PWM inverter. Since then several multilevel topologies have evolved. The general structure of the MVSI is to synthesize a sinusoidal voltage out of several levels of dc voltages [20]. The MVSI can therefore be described as a voltage synthesizer. The so-called multilevel starts from three levels. There are several advantages offered by the MVSI. In Voltage Source Inverter (VSI), the maximum voltage level output is determined by the voltage blocking capability of each device. By using a multilevel structure, the stress on each device can be reduced in proportional to the number of levels, thus the inverter can handle higher voltages [28]. As a result, an expensive and bulky step-up transformer can be avoided in various applications.

There are three main topologies of multilevel inverters as cited in literatures:

1) Diode-Clamped Multilevel Inverter (DCMI) [20-23].
2) Flying-Capacitor Multilevel Inverter (FCMI) [20,21].
3) Modular Structured Multilevel Inverters (MSMI) [20,23].

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels [20]. This topology is not very popular due to the need of large number high voltage rating diodes [20-23]. Furthermore, the voltage unbalance problem make this topology is unattractive to handle real power

flow control. The flying capacitor multilevel inverter, on the other hand, has the significant advantage that it eliminates the clamping diode problems present in the DCMI [20 However, FCMI has several technical difficulties that complicate its practical application for-high power converters. To maintain the charge balance in the capacitors, the dc-link capacitors need a controller, thus adding complexity to the control of the whole circuit. Furthermore, an excessive number of storage capacitors are required when the number of inverter levels is high. Higher level systems are more difficult to package and more expensive due to the bulky capacitors. Moreover, the switching losses will be high for real power transmission [20-21].

The cascaded multilevel inverter (MSMI) requires separate dc sources, and hence is well suited for various renewable energy sources such as photovoltaic, fuel cell and biomass. A single-phase N-level configuration of such inverter is shown in Figure 2.3. Each module consists of a separate dc source associated with a single-phase full-bridge inverter. The ac terminal voltage of each module is connected in series to form an output voltage, V_o. Figure 2.6 shows the synthesized voltage waveform of a seven-level Modular Structured Inverter with three separate dc sources. The output voltage is synthesized by the sum of each dc source from each module, i.e $V_{out} = E_1 + E_2 + E_3$. By different combinations of the four switches, S_{1M} through S_{4M}, each module can generate three different voltage outputs, +E, -E, and zero. The ac output of each module is connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. Note that the number of output phase voltage levels is defined in different way from those of two previous inverters. In this topology, the number of module (M), which is equal to the number of dc sources required, depends on the number of levels (N) of the MSMI. It is usually assumed that N is odd, as this would give an integer-valued M. The number of output phase voltage levels is defined by:

$$M=\frac{N-1}{2} \qquad (2.1)$$

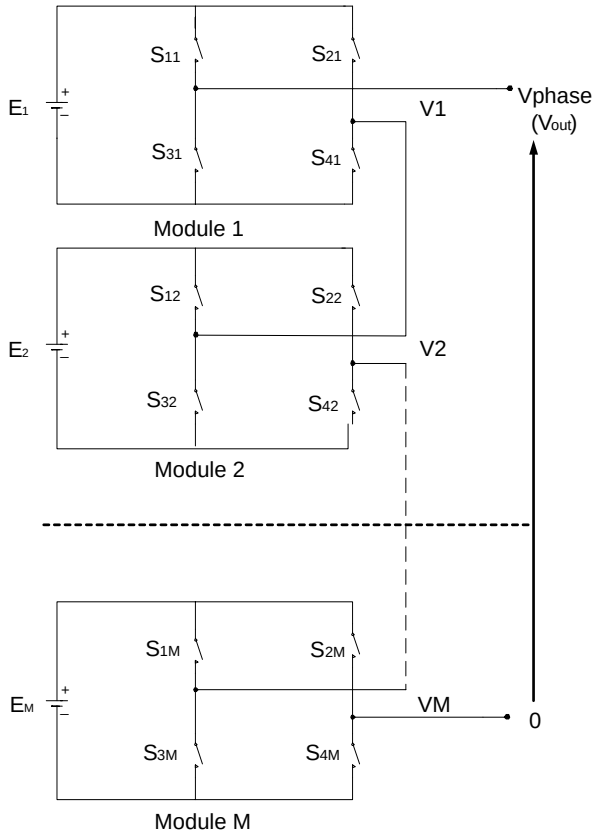


Figure 2.5: Single-phase structure of a MSMI

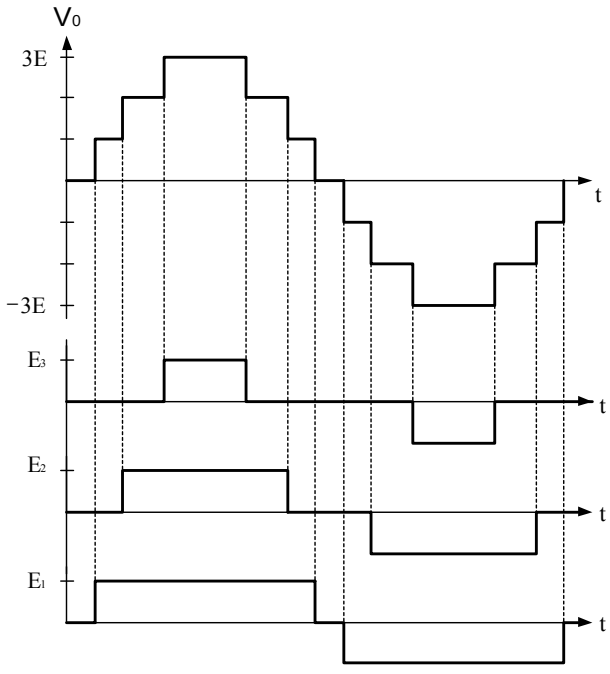


Figure 2.6: Voltage waveform of a seven-level MSMI.

There are many possible switch combinations that can synthesis stair case waveform for MSMI. The number of switch combinations is proportional with the system's level (N). The relationship between the number of switch combinations and the system's level is expressed by [34]:

Number of switch combinations = 2^{N-1}. (2.2)

For example, the number of switch combinations for seven-level inverter is 2^{7-1}, which is 64 different configurations. Hence, the flexibility in voltage synthesizing for this topology is more than DCMI and FCMI. Table 2.1 lists a possible combination of the voltage levels and their corresponding switch states.

Table 2.1: A possible switch combination for MSMI based seven-level inverter.

Load Voltage	+3E	+2E	+E	0	-E	-2E	-3E
S_{11}	1	1	1	1	0	0	0
S_{21}	0	0	0	1	1	1	1
S_{31}	0	0	0	0	1	1	1
S_{41}	1	1	1	0	0	0	0
S_{12}	1	1	1	1	0	0	0
S_{22}	0	0	1	1	0	1	1
S_{32}	0	0	0	0	1	1	1
S_{42}	1	1	0	0	1	0	0
S_{13}	1	1	1	1	0	0	0
S_{23}	0	1	1	1	0	0	1
S_{33}	0	0	0	0	1	1	1
S_{43}	1	0	0	0	1	1	0

As illustrated in Figure 2.5, this topology requires the least number of components among all multilevel converters to achieve the same voltage levels. In addition this topology can avoid extra clamping diodes or voltage balancing capacitors. Moreover modularized circuit layout and packaging is possible because each level has a standard structure. However, with the need of separate dc sources for real power conversions, the application of cascaded inverter can be somewhat limited.

2.3 PWM Modulation Techniques for MSMI

It is generally accepted that performance of an inverter, with any switching strategy is closely associated to the harmonic contents of its output voltage. Accordingly, power electronics researchers have proposed many novel control techniques to reduce and optimise the harmonic content in such waveforms. For multilevel inverter technology, there are several well-known PWM modulation techniques, which can be classified as follows: (1) selective harmonic elimination PWM (SHEPWM) [26,27]; (2) space vector PWM (SVPWM) [28-32]; and (3) sinusoidal PWM (SPWM) [33-38]. These multilevel modulation techniques are adapted from the well-established two-level PWM. Among the abovementioned techniques, the SPWM is the first and by far the most popular for traditional inverter [33]. Its popularity is partly due to its simplicity. The most common SPWM strategy for a two level output voltage is a comparison between sinusoidal with fundamental frequency modulating waveform against a high frequency carrier waveform. The switches turn on to the upper or the lower dc rail supply depending on whether the modulating waveform is greater or lower than the carrier waveform. By raising the carrier frequency, the output voltage harmonic can be moved to higher frequency, thus reducing the size of the output filters required to attenuate the harmonics.

A wide variety of SPWM strategies have been proposed based on this principle as described in [33-38]. With certain modification, this technique can be implemented in multilevel inverters.

2.3.1 The Proposed Modulation Scheme

The proposed modulation scheme for the MSMI is based on the classical unipolar PWM switching technique [46,47]. The main idea behind this method is to compare several modified sinusoidal modulation signals $s(k)$ with a single triangular carrier signal $c(k)$ as shown in Figure 2.7. These modified modulation signals have the same frequency (f_o) and amplitude (A_m). Since the modulation is symmetric, the sinusoidal modulation signals are sampled by the triangular carrier signal once in every carrier cycle. Intersection between the sampled modulation signals and the carrier signal defines the switching instant of the PWM pulses. In order to ensure quarter wave symmetry PWM output waveform, the starting point of the modulation signals ought to be phase shifted by half period of the carrier wave. The number of

modulation signals needed is equal to the number of modules in the MSMI [45]. Recall that the relationship between N and M for MSMI is described in equation (2.1), i.e.:

$$\mathrm{M}=\frac{\mathrm{N}-1}{2}$$

The carrier signal is a train of triangular waveform with frequency f_c and amplitude A_c. Equations (2.2) defines the modulation index m_i for N-level inverter with M number of modules:

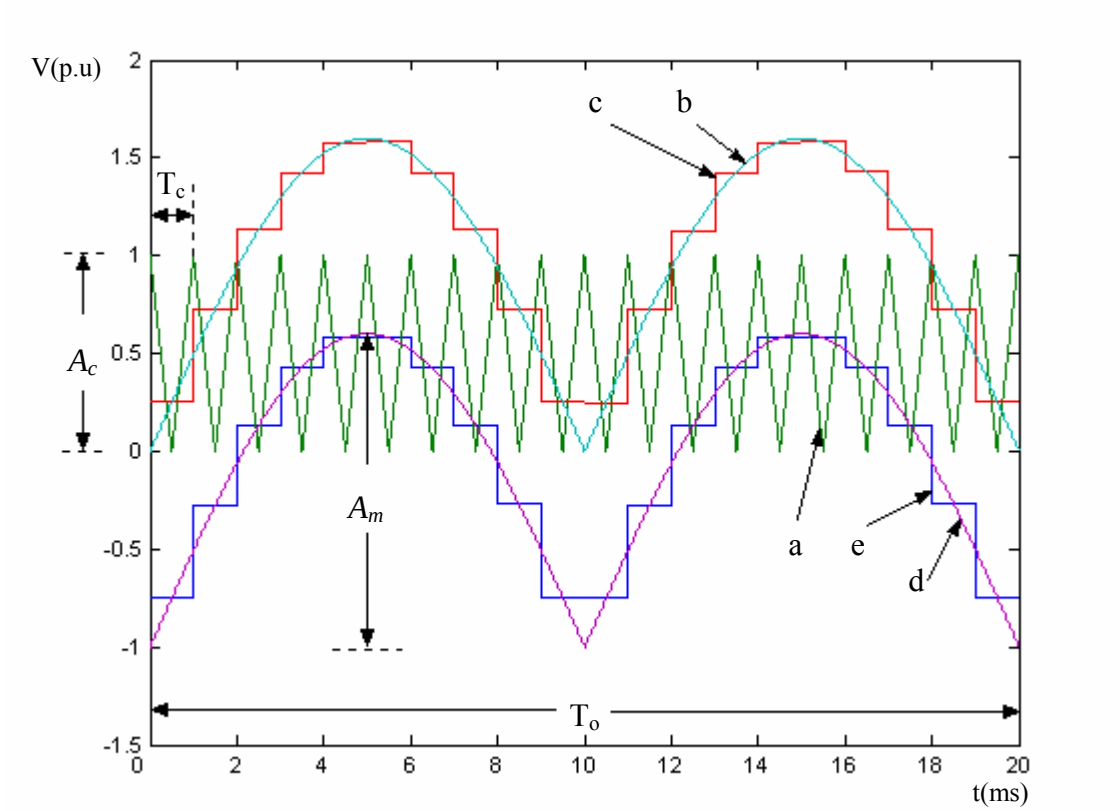
$$m_i = \frac{A_m}{\frac{(\mathrm{N}-1)}{2}A_c} = \frac{A_m}{\mathrm{M}A_c} \tag{2.2}$$

Therefore if A_c defined at a fixed p.u (1p.u), then m_i ranges between 0 and 1, while A_m ranges between 0 and M.

The definition of the modulation ratio m_f for multilevel inverter is similar to the conventional two-level output inverter, i.e.:

$$m_f = \frac{f_c}{f_o} \tag{2.3}$$

Where f_c is the frequency of the carrier signal and f_o is the frequency of sinusoidal modulation signals.

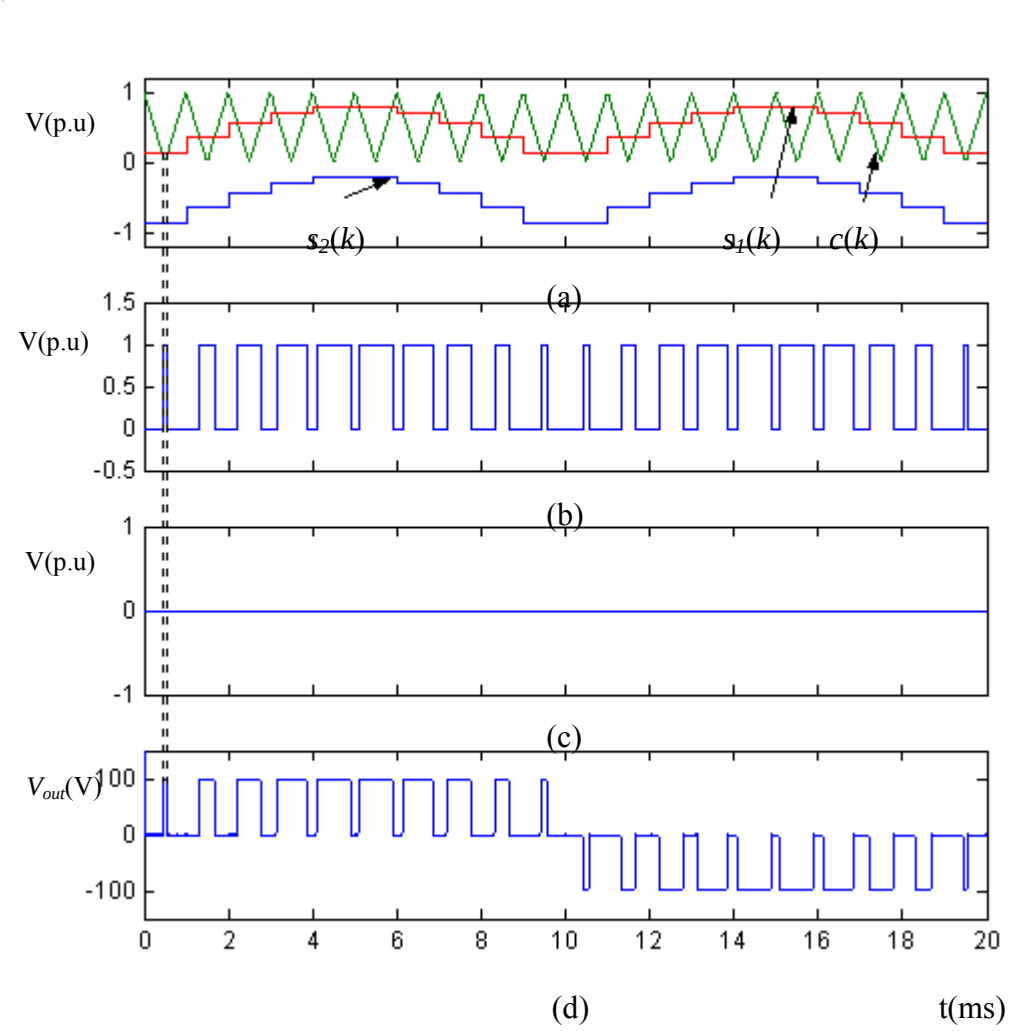


Legend

a. Carrier signal $c(k)$
b. Absolute sinusoidal modulation signal m_1 (t).
c. Modified sinusoidal modulation signal $s_1(k)$ of m_1 (t).
d. Shifted absolute sinusoidal modulation signal m_2 (t).
e. Modified sinusoidal modulation signal $s_2(k)$ of m_2 (t).

Figure 2.7: The modified sinusoidal modulation signals and a single carrier signal.

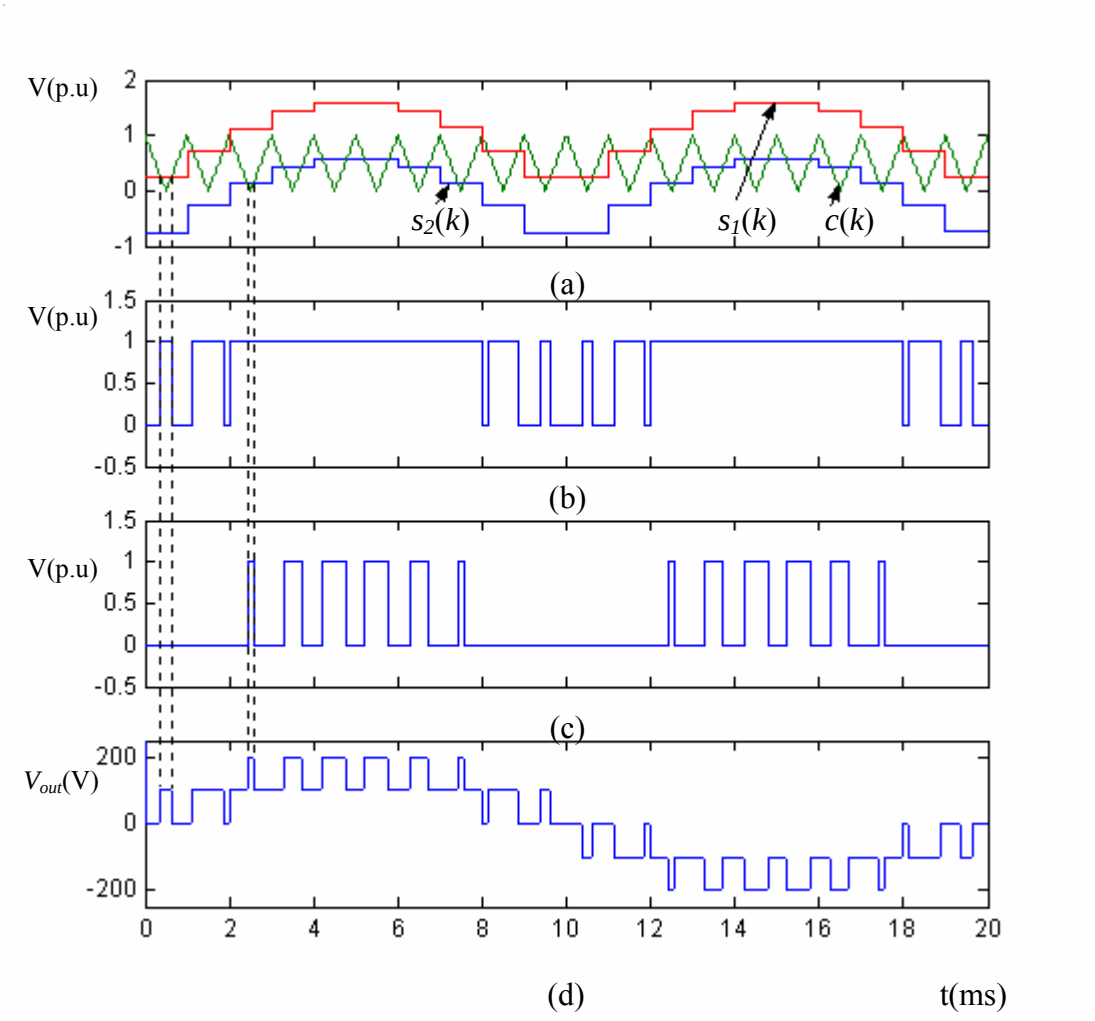
To illustrate the principle of the proposed scheme, a five-level inverter at $m_i = 0.4$ and $m_i = 0.8$ is shown in Figure 2.8 and 2.9 respectively. For clarity, m_f for both cases was arbitrary selected to 20. As mentioned above, the number of modulation signals for a five-level inverter is equal to the number of modules required. Thus two modulation signals namely $s_1(k)$ and $s_2(k)$ and single triangular carrier $c(k)$ are involved in this modulation process. Recall that signals $s_1(k)$ and $s_2(k)$ are modified modulation signal of $m_1(k)$ and $m_2(k)$, respectively. Signal $s_2(k)$ actually is $s_1(k)$ that shifted down by the amplitude of triangular carrier signals A_c.



Legend

(a) Modulation signals and carrier signal
(b) PWM pulses produced from comparison between $s_1(k)$ and $c(k)$, $V_1(k)$
(c) PWM pulses produced from comparison between $s_2(k)$ and $c(k)$, $V_2(k)$
(d) PWM output waveform

Figure 2.8: Principle of the proposed modulation scheme for $m_i = 0.4$, $m_f = 20$.



Legend

(a) Modulation signals and carrier signal
(b) PWM pulses produced from comparison between $s_1(k)$ and $c(k)$, $V_1(k)$
(c) PWM pulses produced from comparison between $s_2(k)$ and $c(k)$, $V_2(k)$
(d) PWM output waveform

Figure 2.9: Principle of the proposed modulation scheme for $m_i = 0.8$ $m_f = 20$.

The plots in Figures 2.8 and 2.9 show the PWM pulses and the inverter output waveform in the modulation process. Pulses $V_1(k)$ is generated from the comparison between $s_1(k)$ and $c(k)$, while $V_2(k)$ is from comparison between $s_2(k)$ and $c(k)$. The comparison is designed such that if $s_1(k)$ is greater than $c(k)$, a pulse-width $V_1(k)$ is generated. On the other hand, if $s_2(k)$ is greater than $c(k)$, $V_2(k)$ is generated. If there is no intersection, the $V_1(k)$ and $V_2(k)$ remain at 0. It can also be seen in Figure 2.8 that if $m_i \leq 0.5$, only $s_1(k)$ and carrier signal $c(k)$ is involved in the modulation

process. There is no intersection for $s_2(k)$. Therefore, the output pulse $V_2(k)$ is zero. The output voltage V_{out} is similar to the conventional three-level unipolar PWM case.

For $m_i > 0.5$, as depicted in Figure 2.9, both modulating signal $s_1(k)$ and $s_2(k)$ and carrier signal $c(k)$ are involved. In this case, two modulating signals intersect the carrier and therefore $V_1(k)$ and $V_2(k)$ are generated. Since there are two modulating signals intersect with the carrier, it can be expected that the equation of the switching angles to be defined is not as straight forward as for $m_i \leq 0.5$ case. It is also important to note that modulation ratio m_f, of the inverter must be selected to be even. This provision must be obeyed to ensure the output waveform obtained is quarter wave symmetry. With this assumption, the derivation for the switching angles equations is greatly simplified.

It will be shown in the next Section that using the proposed modulation scheme, simple trigonometric equations to define the switching instant of inverter switches can be obtained. The derived equations can be suitably programmed using microprocessor for an online PWM waveform generation.

2.3.2 Derivation of the Switching Angle Equations

It is desirable to obtain mathematical expressions that define the switching instants for the inverter switches. The motivation of such exercise is to derive simple equations that can be programmed using digital technique. The ultimate aim is to generate the PWM pulses on-line without having to do physical comparison of the carrier and modulating signals. The initial derivation is based on a modular structured five-level inverter. Then by extending the result of five-level inverter equations, a general equation for N-level MSMI can be accomplished.

The k^{th} rising edge is defined as the intersection of the negative slope carrier $c^-(k)$ and two set of modulating signals $s_1(k)$ and $s_2(k)$ as shown in Figure 2.10. The variable k represents a position of each modulated width pulses $V_1(k)$ and $V_2(k)$, initiated from $k = 1,2,3\ldots m_f$. Due to symmetrical nature of the proposed PWM scheme, the intersection between the positive slope carrier $c^+(k)$ and the modulating

signals is not required in the derivation. It can be deduced from the rising edge equation, i.e. the intersection between $\bar{c}(k)$ and $s_1(k)$ or $s_2(k)$.

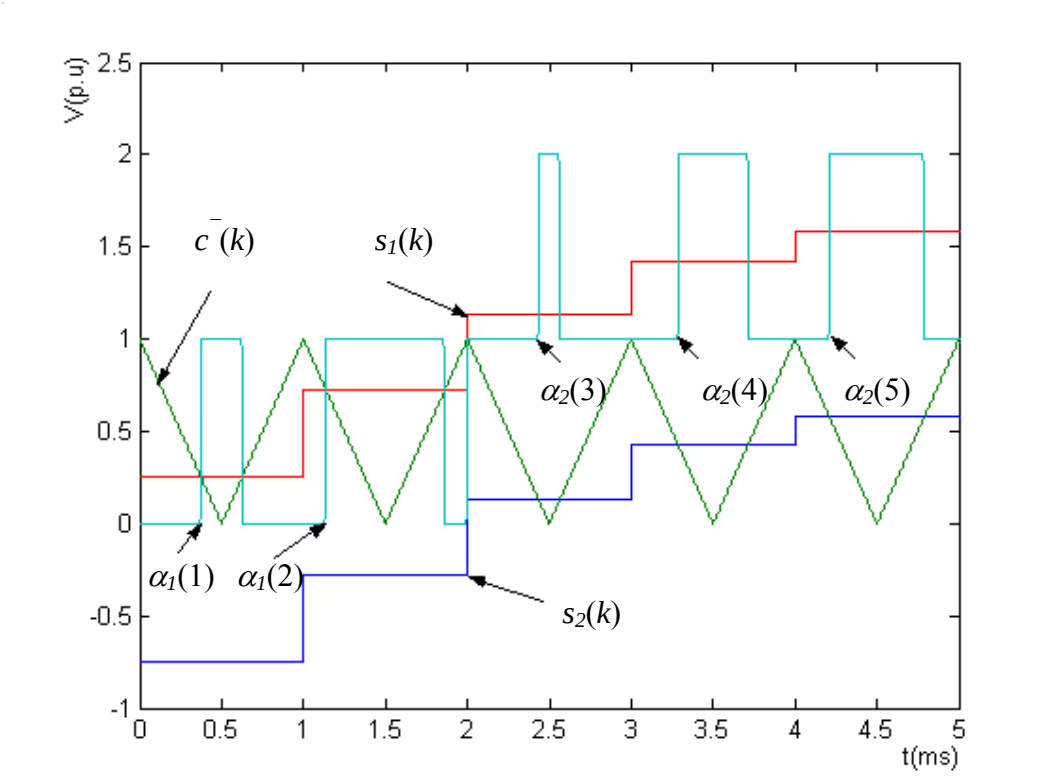


Figure 2.10: Intersection between single carrier and modulation signals in first quarter wave.

Figure 2.10 shows the single carrier and two set of sampled modulation signals in generating five-level inverter output voltage for $m_i = 0.8$, $m_f = 20$. The straight-line equation for the carrier wave is denoted by $\bar{c}(k)$ for the negative slope. It can be expressed as:

$$\bar{c}(k) = \left(\frac{-A_c}{\frac{T_c}{2}} \right) \alpha(k) + hA_c \qquad (2.4)$$

$k = 1, 2, 3....$

$h = 1, 3, 5....$

The relationship between T_c, f_c, f_o and m_f can be written as follows:

$$T_c = \frac{1}{f_c} \tag{2.5}$$

$$f_c = m_f f_o \tag{2.6}$$

Where T_c is a period of carrier signal, f_c is a carrier frequency and f_o is a modulating signal frequency.

The symmetric regular sampled modulation signals $s_{1k}(k)$ and $s_{2k}(k)$ can be expressed as:

$$s_1(k) = A_m \sin\left[\omega(i) + \frac{\pi}{m_f}\right] \tag{2.7}$$

$$s_2(k) = A_m \sin\left[\omega(i) + \frac{\pi}{m_f}\right] - A_c \tag{2.8}$$

$i = 0,1,2,3....$ when the modulation signal intersect with $c^-(k)$

The angular frequency ω, in (2.6) and (2.7) is represented by:

$$\begin{aligned}\omega &= 2\pi f_o \times \frac{T_o}{m_f} \\ &= \frac{2\pi}{m_f}\end{aligned} \tag{2.9}$$

From arithmetic regression equation,

$$T_n = a + (n-1)d \tag{2.10}$$

Where;

T_n = number at n^{th}

$a = T_1$ = first number.

d = increment/decrement of next number

n = 1,2,3….

Using the arithmetic regression in (2.10) and realizing that *k* is equal to *n*, thus relationship between *h* and *i* with *k* can be rewritten as:

$$\begin{aligned} h &= 1+(k-1)2 \\ \therefore h &= 2k-1 \\ i &= 0+(k-1)1 \\ \therefore i &= k-1 \end{aligned} \tag{2.11}$$

The k^{th} raising edge ($\alpha_1(k)$) of PWM signal $V_1(k)$ is produced by the intersection between $s_1(k)$ and $\bar{c}(k)$. This rising edge $\alpha_1(k)$ is represented by:

$$\left(\frac{-A_c}{\frac{T_c}{2}}\right)\alpha_1(k)+hA_c = A_m \sin\left(\omega(i)+\frac{\pi}{m_f}\right)$$

$$\begin{aligned} \alpha_1(k) &= \frac{T_c}{2}\left[h-\frac{A_m}{A_c}\sin\left(\omega(k-1)+\frac{\pi}{m_f}\right)\right] \\ &\quad \frac{T_c}{2}\left[(2k-1)-\frac{A_m}{A_c}\sin\left(\omega(k-1)+\frac{\pi}{m_f}\right)\right] \end{aligned} \tag{2.12}$$

Moreover, for intersection between $s_2(k)$ with $\bar{c}(k)$, every rising edge $\alpha_2(k)$ of PWM signal $V_2(k)$ can be expressed as:

$$\left(\frac{-A_c}{\frac{T_c}{2}}\right)\alpha_2(k)+hA_c = A_m \sin\left(\omega(i)+\frac{\pi}{m_f}\right)-A_c$$

$$\begin{aligned} \therefore \alpha_2(k) &= \frac{T_c}{2}\left[(h+1)-\frac{A_m}{A_c}\sin\left(\omega(k-1)+\frac{\pi}{m_f}\right)\right] \\ &= \frac{T_c}{2}\left[2k-\frac{A_m}{A_c}\sin\left(\omega(k-1)+\frac{\pi}{m_f}\right)\right] \end{aligned} \tag{2.13}$$

From observation of equation (2.12) and (2.13), it can be seen that in equation (2.12) the *h* is alone while in (2.13), the *h* is added with 1. This relationship shows these equations actually can be generalized to produce N-level inverter, where $\alpha_M(k)$ can be expressed as:

$$\therefore \alpha_M(k) = \frac{T_c}{2}\left[(h+\mathrm{M}-1) - \frac{A_m}{A_c}\sin\left(\omega(k-1)+\frac{\pi}{m_f}\right)\right]$$

$$= \frac{T_c}{2}\left[(2k+\mathrm{M}-2) - \frac{A_m}{A_c}\sin\left(\omega(k-1)+\frac{\pi}{m_f}\right)\right] \qquad (2.14)$$

Where M = 1,2,3…and relationship between M and N for modular structured multilevel inverter is expressed by:

$$\mathrm{M} = \frac{\mathrm{N}-1}{2} \qquad (2.1)$$

For example, to produce a nine-level output voltage using modular structured inverter, equation (2.14) can be used to generate $V_1(k)$, $V_2(k)$, $V_3(k)$ and $V_4(k)$. Where $V_1(k)$ is generated from $\alpha_1(k)$, $V_2(k)$ from $\alpha_2(k)$, $V_3(k)$ from $\alpha_3(k)$ and $V_4(k)$ from $\alpha_4(k)$ respectively, they are rewritten below as:

$$\alpha_1(k) = \frac{T_c}{2}\left[(2k-1) - \frac{A_m}{A_c}\sin\left(\omega(k-1)+\frac{\pi}{m_f}\right)\right] \qquad (215(a))$$

$$\alpha_2(k) = \frac{T_c}{2}\left[(2k) - \frac{A_m}{A_c}\sin\left(\omega(k-1)+\frac{\pi}{m_f}\right)\right] \qquad (2.15(b))$$

$$\alpha_3(k) = \frac{T_c}{2}\left[(2k+1) - \frac{A_m}{A_c}\sin\left(\omega(k-1)+\frac{\pi}{m_f}\right)\right] \qquad (2.15(c))$$

$$\alpha_4(k) = \frac{T_c}{2}\left[(2k+2) - \frac{A_m}{A_c}\sin\left(\omega(k-1)+\frac{\pi}{m_f}\right)\right] \qquad (2.15(d))$$

Using equation (2.1), the relationship between m_i with A_m and A_c for nine-level inverter is expressed by:

$$m_i = \frac{A_m}{4A_c} \tag{2.16}$$

CHAPTER III

DESIGN AND CONSTRUCTION OF A MSMI PROTOTYPE

3.1 Introduction

This chapter describes the design and construction of a 5-level MSMI prototype inverter test-rig to verify the proposed PWM scheme described in previous Chapter. Figure 3.1 (a) shows the photograph of overall prototype arrangement, while Figure 3.1 (b) shows MCB 167 microcontroller, driver circuit and five-level MSMI power circuit.

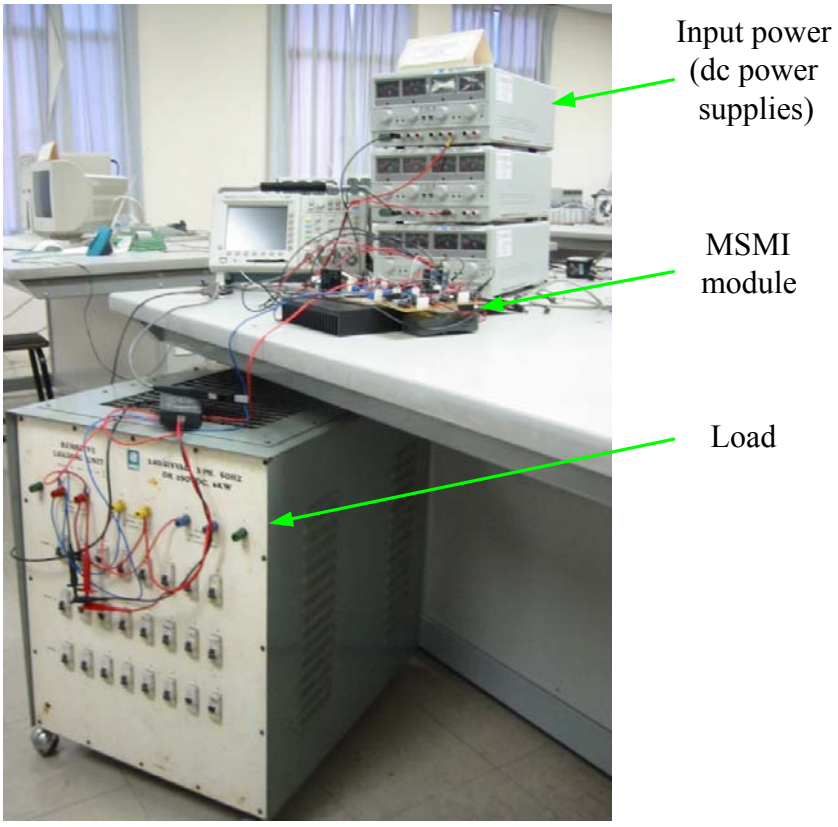


Figure 3.1 (a): Photograph of overall test-rig arrangement.

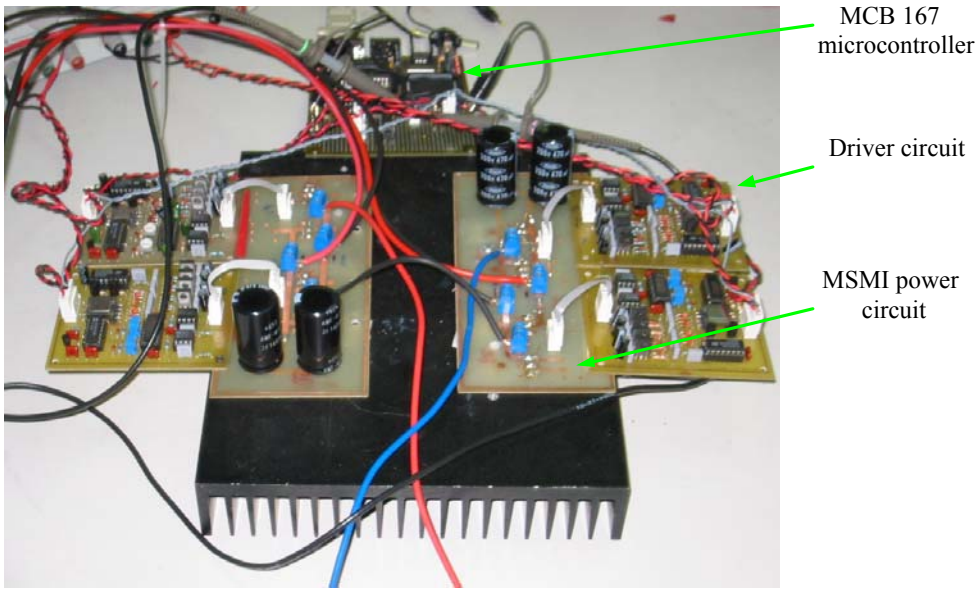


Figure 3.1 (b): Photograph of MCB-167 microcontroller, driver circuit and MSMI power circuit.

3.2 Siemens Microcontroller

The PWM signal generation is performed by SAB-C167CR-LM micocontroller from Siemens. The microcontroller is a fast instruction fixed-point microprosessor. Block diagram in Figure 3.2 desribes the main features of the chip. Integrated on-chip peripherals such as Serial Port, bi-directional Parallel Port, Timers, PWM module and Peripheral Interfaces units make the interfacing task much easier and with higher reliablity.

Some of the main features of SAB-C167CR-LM and its peripherals are summarized as follows [48]:

- The CPU is capabled of 100 ns minimum instruction cycle time, with most instruction executed in 1 cycle
- The external interrupt inputs are sampled every 50ns
- The CPU provides 56 separate interrupt nodes with 16 priority levels
- The CPU has two 16-channel Capture/Compare (CAPCOM) Units
- The CPU supports four independent high-speed Pulse Width Modulation signals with two independent time base

For analog signal measurement, a 16-channel 10-bit A/D converter with programmable conversion time has been integrated on the CPU.

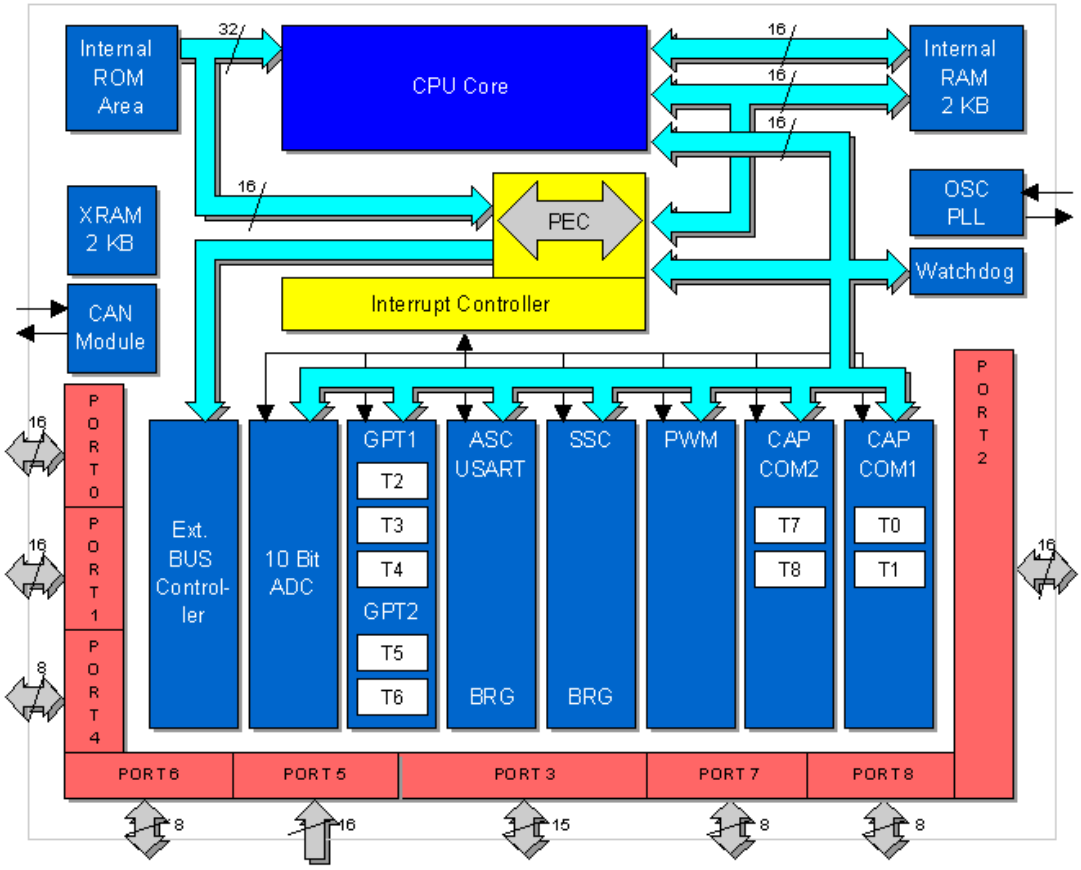


Figure 3.2: Block diagram of the SAB-C167CR-LM chip.

The MCB-167 microcontroller evaluation board shown in Figure 3.3 is used to develop, debug and execute SAB-C167CR application programs. The board, manufactured by Keil Electronics has two RAM chips, Toshiba TC551001BPL-70L each of 131 kilobyte in size. A wire wrap field is available for additional application hardware construction on-board.

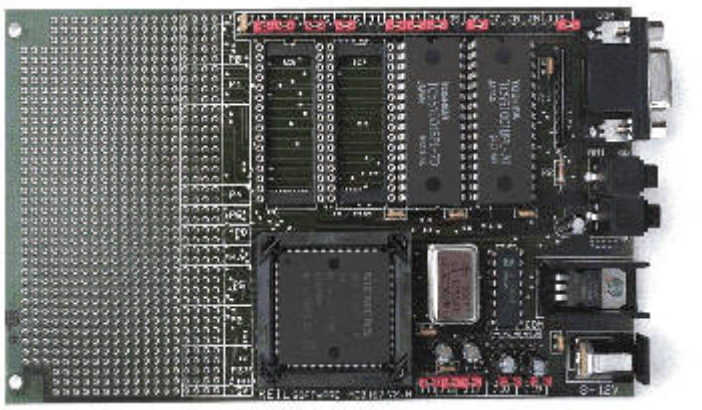


Figure 3.3: The MCB-167 microcontroller evaluation board.

For short programs, Keil μVision provides a restricted version of debugger with 8k-byte code size limit. For small size program, it can be loaded using Siemens Bootstrap Loader Tool. However if the bigger program is to be executed, the Keil C166 Cross Compiler is required. The Keil C166 is not a universal C compiler; in fact it is a dedicated 166/167 C compiler that generates extremely fast and compact code. The Keil C166 Compiler implements the ANSI standard for the C language.

3.3 Generation of PWM Waveform

To obtain a five-level output voltage as described in Chapter II, three signals need to be generated, namely:

1. Fundamental frequency square wave (in this case, 50 Hz),
2. PWM signal $V_1(k)$
3. PWM signal $V_2(k)$

These signals can be generated using on chip PWM module. The use of this module eliminates the requirement for complicated external timers.

3.3.1 PWM Module

The Pulse Width Modulation Module consists of 4 independent PWM channels. Each channel (shown in Figure 3.4) has a 16-bit up/down counter PTx, a 16-bit period register PPx, a 16-bit pulse width register PWx with a shadow latch, two comparators, and the necessary control logic. The operation of all four channels is controlled by two common control registers, PWMCON0 and PWMCON1. The interrupt control and status is handled by one interrupt control register PWMIC, which is also common for all channels.

The PWM Module of the C167CS allows the generation of up to 4 independent PWM signals. These PWM signals can be generated for a wide range of output frequencies, depending upon the CPU clock frequency (f_{CPU} = 20MHz), the selected counter resolution (f_{CPU} / 1 or f_{CPU} / 64), the operating mode (edge/center aligned) and the required PWM resolution (1-bit … 16-bit).

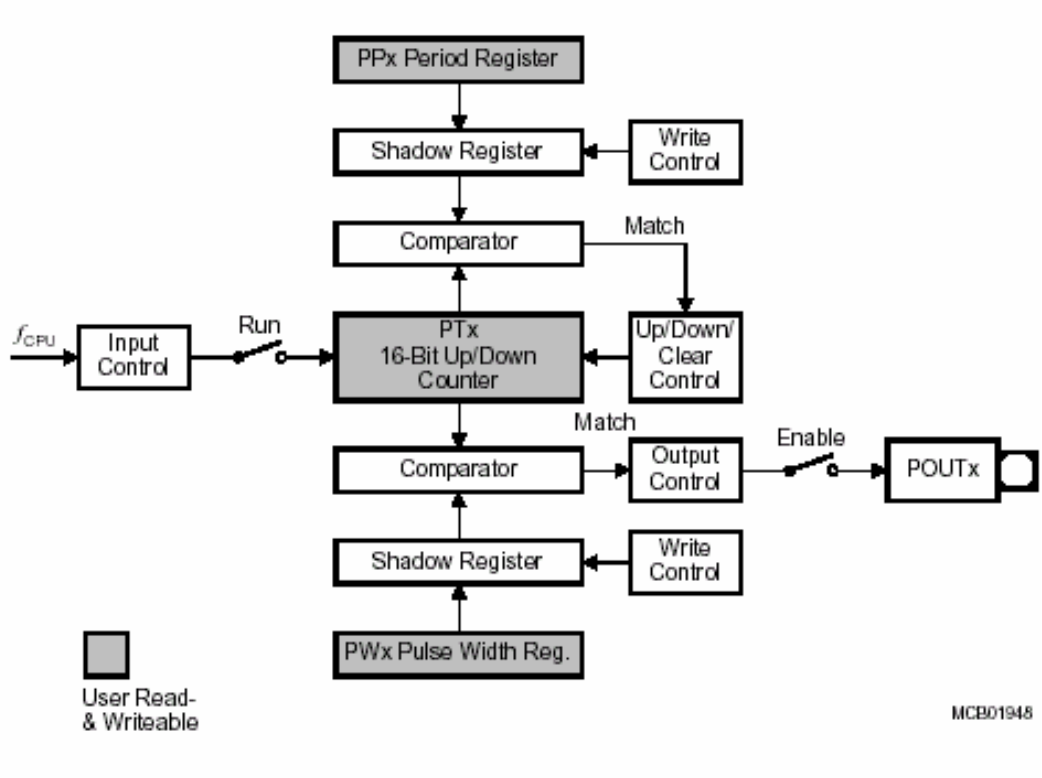


Figure 3.4: PWM Channel block diagram.

The PWM module in C167 provides four different operating modes, namely;

• Standard PWM generation (edge aligned PWM)

• Symmetrical PWM generation (center aligned PWM)

• Burst mode generation

• Single shot mode generation

In this work, the required three signals can be generated using two operating modes. Standard PWM is selected to generate fundamental frequency square wave, meanwhile Symmetrical PWM is dedicated to generate V_a and V_b.

3.3.2 Standard PWM Generation (Edge Aligned PWM)

Edge Aligned PWM is selected by clearing the respective bit PMx in register PWMCON1 to '0'. In this mode the timer PTx of the respective PWM channel is always counting up until it reaches the value in the associated period shadow register. Upon the next count pulse the timer is reset to 0000_H and continues counting up with subsequent count pulses. The PWM output signal is switched to high level when the timer contents are equal to or greater than the contents of the pulse width

shadow register. The signal is switched back to low level when the respective timer is reset to 0000_H, i.e. below the pulse width shadow register. The period of the resulting PWM signal is determined by the value of the respective PPx shadow register plus 1, counted in units of the timer resolution as given by the equation below:

$$PWM\_Period_{Mode0} = [PPx] + 1 \quad (3.1)$$

The duty cycle of the PWM output signal is controlled by the value in the respective pulse width shadow register. This mechanism allows the selection of duty cycles from 0% to 100% including the boundaries. For a value of 0000_H the output will remain at a high level, representing a duty cycle of 100%. For a value higher than the value in the period register the output will remain at a low level, which corresponds to a duty cycle of 0%.

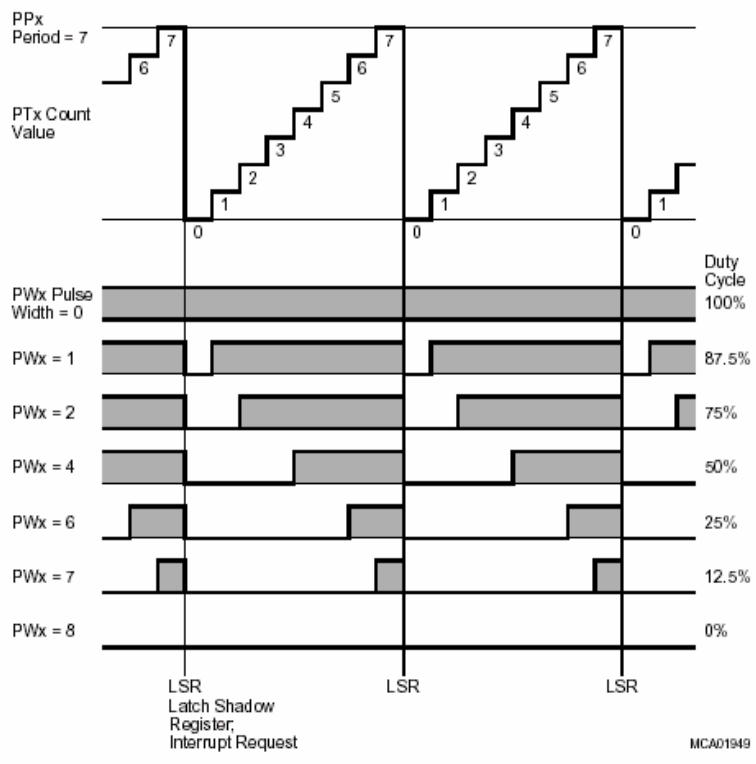


Figure 3.5: Operation and Output Waveform in Edge Aligned PWM.

Figure 3.5 illustrates the operation and output waveforms of a PWM channel in mode 0 for different values in the pulse width register. This mode is referred to as Edge

Aligned PWM, because the value in the pulse width (shadow) register only effects the positive edge of the output signal. The negative edge is always fixed and related to the clearing of the timer.

3.3.3 Symmetrical PWM Generation (Center Aligned PWM)

This mode is referred to as Center Aligned PWM, because the value in the pulse width (shadow) register effects both edges of the output signal symmetrically. Center Aligned PWM is selected by setting the respective bit PMx in register PWMCON1 to '1'. In this mode the timer PTx of the respective PWM channel is counting up until it reaches the value in the associated period shadow register. Upon the next count pulse the count direction is reversed and the timer starts counting down with subsequent count pulses until it reaches the value 0000_H. Upon the next count pulse the count direction is reversed again and the count cycle is repeated with the following count pulses.

The PWM output signal is switched to a high level when the timer contents are equal to or greater than the contents of the pulse width shadow register while the timer is counting up. The signal is switched back to a low level when the respective timer has counted down to a value below the contents of the pulse width shadow register. So in mode 1 this PWM value controls both edges of the output signal. Note that in Center Aligned PWM operation the period of the PWM signal is twice the period of the timer:

$$PWM\_PeriodMode1 = 2 \times ([PPx] + 1) \quad (3.2)$$

Figure 3.6 illustrates the operation and output waveforms of a PWM channel in mode 1 for different values in the pulse width register.

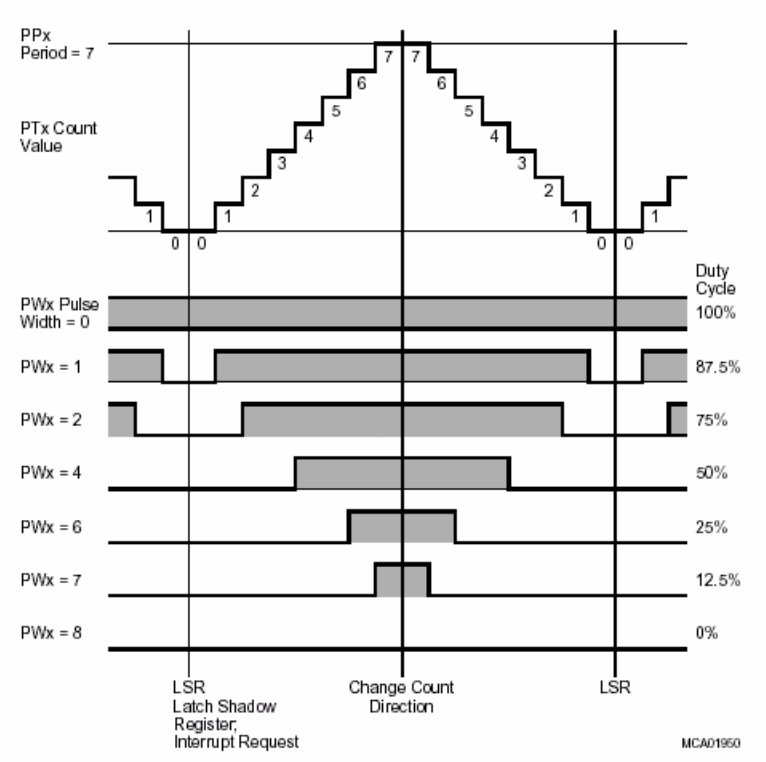


Figure 3.6: Operation and Output Waveform in Center Aligned PWM.

3.3.4 PEC (Peripheral Event Controller) Operation

For high frequency operation, extremely fast data transfer is required when a corresponding interrupt request occurs. Receiving interrupt signals from source pointer, PEC responses the request by moving a byte or word to the corresponding destination pointer within a single CPU cycle. Additionally it does not require saving and restoring the machine status. The C167 has 8 PEC channels which offers such fast interrupt data transfer capability. Each channel is controlled by the dedicated PEC channel Counter/Control register (PECCx) and a pair of pointers for source (SRCPx) and destination (DSTPx) of the transfer data.

Either a byte or word is moved during PEC service cycle, it can be controlled by Byte/Word Transfer bit BWT. This selection controls the transferred data size and the increment step for the modified pointer. The PEC Transfer Count Field, COUNT controls the action of a respective PEC channel, where the content of bit field COUNT at the time the request is activated and select the action. COUNT may allow a specified number of PEC transfers, unlimited transfer or no PEC services at all.

The PEC transfer COUNT allows to service a specified number of requests by the respective PEC channel, and then activate the interrupt services routine when it reaches 00_H. The interrupt services routine is associated with the priority level. After each PEC transfer the COUNT field is decremented and the request flag is cleared to indicate that the request has been serviced.

3.3.5 Generation of Square Wave Signal

In order to generate square wave signal, the Edge Aligned PWM operation mode is selected by clearing bit PMx in register PWMCON1 to '0' (Note that the available channel is 0,1,2 and 3, for this signal generation the selected channel is 3—thus PM3 is set to '0"). It is important to note that in generating PWM signal the selected channel must be the same for all registers. Thus the PWM Period Register (PPx) and the Pulse Width Register (PWx) are set to PP3 and PW3, respectively. Then the counter resolution is set to f_{CPU} / 64 by setting PTI3 in register PWMCON0 to '1'. This is compulsory in generating 50 Hz square wave because if the resolution is set to CPU clock (20MHz); the binary number of PP3 will be more than 16-bit, which is out of register limit. Where the new counter resolution to generate 50Hz square wave signal is set to f_{CPU} / 64 (312.5kHz).

PP3 is chosen to generate 50Hz square wave signal, which in clock-count, it can be written as:

$$\text{PP3} = \frac{312.5kHz}{50Hz} = 6250 \text{ clock-count} \qquad (3.3)$$

To generate 50Hz square wave signal, the Pulse Width Register (PWx) for this signal PW3, must be half of PP3, which is equal to 3125 clock-count.

3.3.6 Generation of $V_1(k)$ and $V_2(k)$ Signals

In order to generate $V_1(k)$ and $V_2(k)$ signals, Center Aligned PWM operation mode is selected by setting bit PMx in register PWMCON1 to '1'. Since the PWM module of the SAB-C167CR-LM offers four channels in generating PWM signals, which channel 3 is used in generating 50Hz square wave, other three channels namely; 0,1 and 2 are dedicated in generating $V_1(k)$ and $V_2(k)$. To generate PWM signals $V_1(k)$

and $V_2(k)$, channel 0 and 1 are chosen, respectively. While channel 2 is dedicated as input trigger for PECC6 in CAPCOM Units to generate PW1. This condition is required because only 1 interrupt is provided in PWM Module. This interrupt (PWMIC) is selected for channel 0 to generate $V_1(k)$. From above explanation, all registers dedicated in generating $V_1(k)$ and $V_2(k)$ can be expressed as:

PP0 = PP1= PP2 = *period_reg*,

Where period_register is presented by:

$$period\_reg = \frac{f_{CPU}}{f_o \times 2 \times m_f} = \frac{20MHz}{50 \times 2 \times m_f} = \frac{200000}{m_f} \quad (3.4)$$

Since the equation derived is in time domain, conversion to clock-count is compulsory. The conversion can be written as:

$$\text{PWx} = period\_reg - \left(period\_reg\left(2k-1\right) - E \times f_{CPU} \right) \quad (3.5)$$

Pulse Width Register (PWx) in equation (3.7) is $\alpha_M(k)$ in form of clock-count domain, while *E* represents the gating signal equations derived in Chapter III. Hence in generating signals $V_1(k)$ and $V_2(k)$, the Pulse Width Register PW0, PW1 and PW2 is written as:

$$\text{PW0} = period\_reg - \left\{ period\_reg\left(2k-1\right) - \left(\frac{T_C}{2} \left[(2k-1) - \frac{A_m}{A_C} \sin\left(\omega(k-1) + \frac{\pi}{m_f} \right) \right] \right) \times 20M \right\} \quad (3.6)$$

$$\text{PW1} = period\_reg - \left\{ period\_reg\left(2k-1\right) - \left(\frac{T_C}{2} \left[2k - \frac{A_m}{A_C} \sin\left(\omega(k-1) + \frac{\pi}{m_f} \right) \right] \right) \times 20M \right\} \quad (3.7)$$

$$\text{PW2} = \frac{period\_reg}{2} \quad (3.8)$$

3.4 Functional Block Diagram

The functional block diagram of the microcontroller ports, ex-or gate, IGBT gate drive and power circuit are shown in Figure 3.7. The PWM signals ($V_1(k)$ and $V_2(k)$) and 50 Hz squarewave are generated by the PWM module and latched out via C167 microcontroller parallel ports P7.0, P7.1 and P7.3, respectively. The fast external interrupt signal for P7.2, which operates as input trigger for P7.1 is activated via port P.2.9. The enable signals for IGBT gate drive are also supplied by microcontroller via ports P2.0 through P2.3.

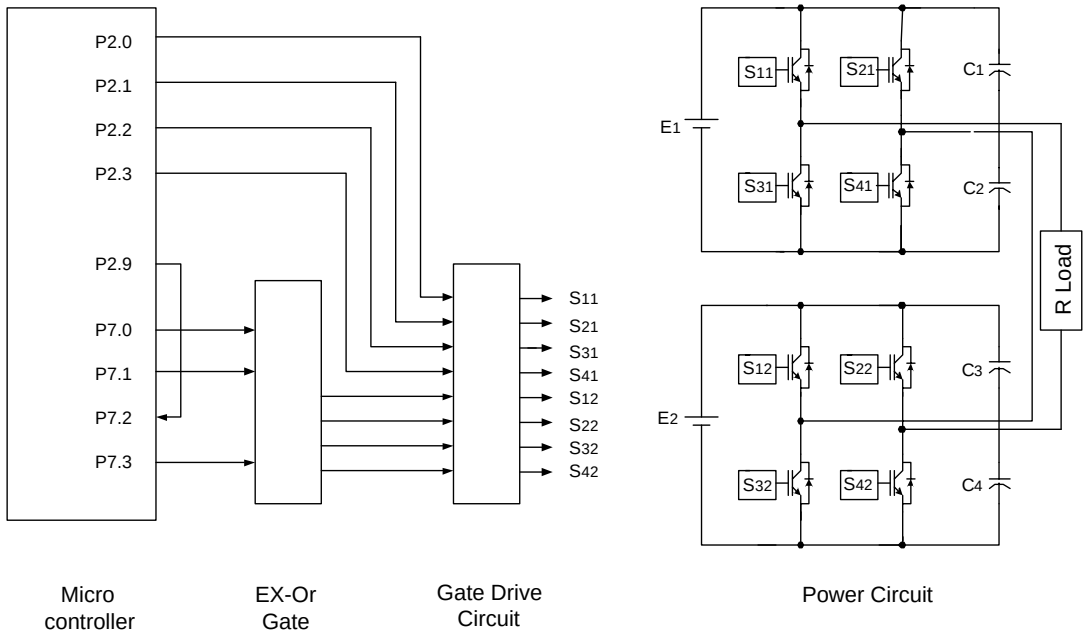


Figure 3.7: Functional Block Diagram

3.4.1 Ex-or Gate

The ex-or gate is required to generate gating signals for switches S_{12}/S_{32} and S_{22}/S_{42}. The speed of the ex-or gate must be sufficiently high to ensure delay between PWM output signals of ex-or gate and fundamental signal are not very significant. The CD74ACT86E is the most suitable TTL to do the task. It is a high speed Si-gate CMOS device manufactured by Texas instrument. The maximum rise and fall time for the IC is only 10ns, which is more than adequate to execute the task. It has four ex-or gates integrated in the IC with 2 inputs and 1 output for each gate. Only two signals are need to produce from the IC, hence only two gates are used in the process.

3.4.2 Gate Drive Circuit

An IGBT is a voltage-controlled device that needs a low firing signal to turn the device on and off. In this work each of the eight devices are switched using a gate drive circuit that designed in house [49]. Each gate-drive circuit requires 100mA and 12V as input to produce an isolated ±15V output signal.

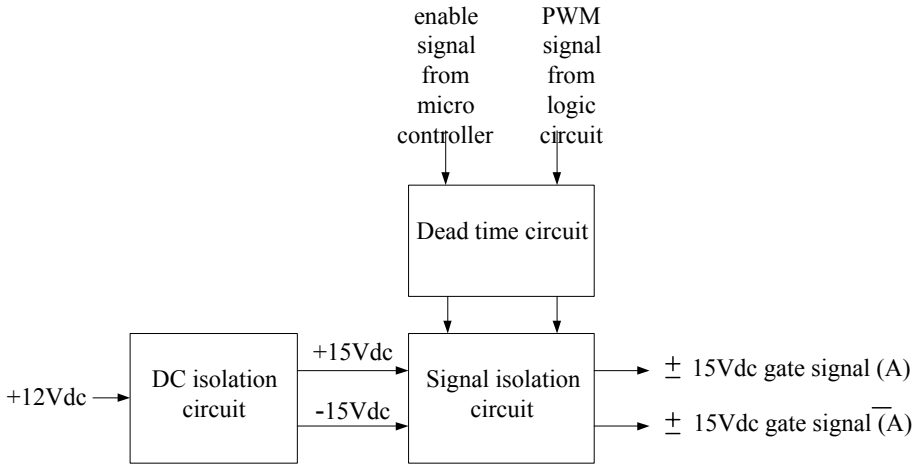


Figure 3.8: Block diagram of gate drive circuit.

The gate drive circuit can be separated into three parts as depicted in Figure 3.8. Dead time circuit is added to each gate signal for protection against shoot-through in the inverter leg. The dc power supply for top and bottom IGBT of the same leg need to be isolated. This is achieved by a high frequency transformer, which is employed in dc isolation circuit. The PWM signals from logic circuit also need to be isolated to protect the controller board from any incoming surge or high voltage signals from power circuit. This is accomplished by a pair of optocouplers, which integrated in signal isolation circuit.

The gate drive circuit provides a +15V and –15V of output voltage. This feature avoids the problem of Miller effect on the top switch when the bottom switch at the same leg suddenly turns on. For a modular structured five level inverter, four equivalent gate drive circuits is required to control eight IGBT switches.

3.4.3 Power Circuit

As illustrated in Figure 3.7, two modules of cascaded inverter power circuit are required for a five-level inverter. Both modules are connected in series and constructed from IGBT switches and dc link capacitors.

3.4.4 IGBT Switch

Power switches used for the inverter are type IRG430CKD IGBTs, manufactured by International Rectifier. They come in a single unit with an anti parallel diode as shown in Figure 3.9. Some of the important ratings of this particular IGBT are shown in Table 3.1.

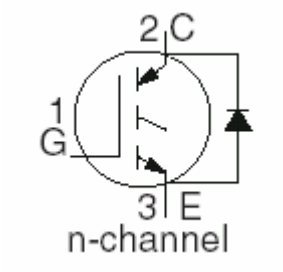


Figure 3.9: Structure of IGBT type IRG430CKD.

Table 3.1: Ratings and specifications of IGBT type IRG430CKD.

V_{CE} (V)	$V_{CE\ sat}$ (V)	$I_{C\ (cont\ at\ 25°C)}$ (A)	I_{CM} Pulsed (A)	t_r (ns)	t_f max. (ns)	$P_{D\ (at\ 25°C)}$ (W)
600	2.21	28	58	42	120	100

V_{CE} = collector-emitter voltage; $V_{CE\ sat}$ = collector-emitter saturated voltage; $I_{C\ (cont\ at\ 25°C)}$ = collector current (flowing continuously at 25°C); I_{CM} = maximum collector pulsed current; t_r = rise time; t_f = maximum fall time.

3.5 Flowchart of the program in generating PWM signals

The flowchart of the PWM generation program is shown in Figure 3.10. After power-up the microcontroller board, initialization of all variables and peripheral ports take place. The resolution for each PWM channel is configured in the PWM

timer. The desired modulation index, m_i and modulation ratio, m_f is chosen by setting the value in the program. By resetting the switch of the board the operation is stopped.

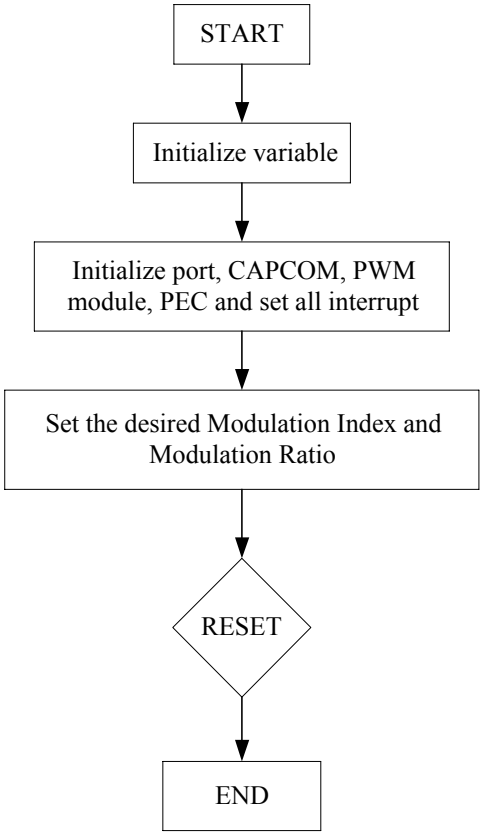


Figure 3.10: Flowchart for PWM generation program.

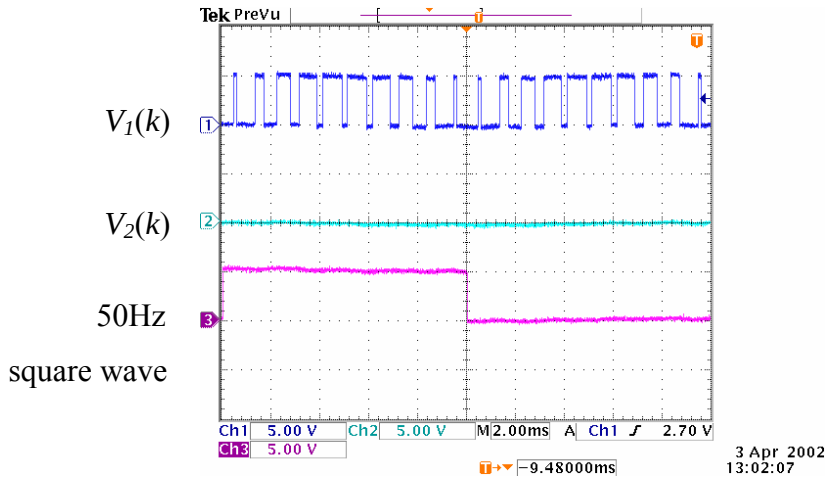
3.5.1 Setting-up MCB167 and main subroutines

This section is concerns about setting-up the MCB167 board and peripherals for the intended application. It involves the setting of the PWM Module, PWM Interrupt and Peripheral Event Controller. The subroutines in this section are briefly describes as follows:

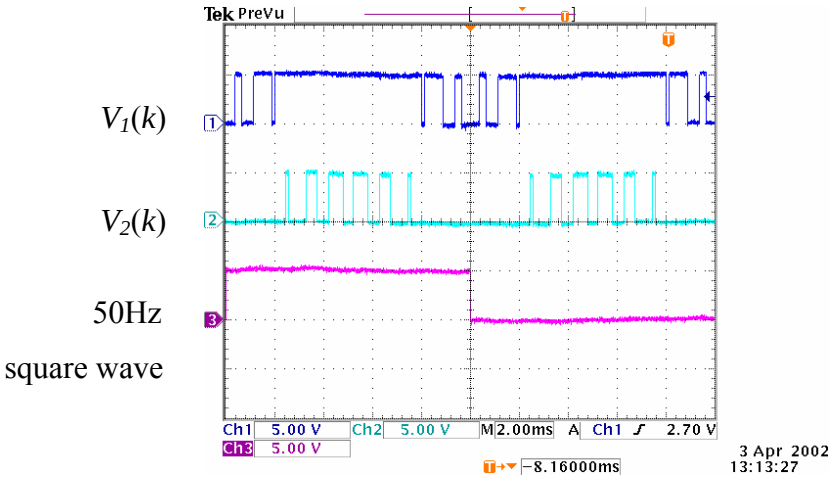
- PWM_init(): In PWM Module, 3 channel is set at CPU clock and symmetrical PWM generation (centered aligned), while 1 channel is set to CPU/64 clock and standard PWM generation (edge aligned).
- PWM_PEC_init(): Since only one interrupt is provided by PWM Module, this interrupt (PWMIC) is dedicated for channel 0.
- PEC_init(): The peripheral event controller is set to respond an interrupt request for PWM Module in channel 1 using channel 2 as input trigger.

3.6 Sample Waveforms

Output Waveforms From MCB167 Figure 3.11 (a) and 3.11 (b) shows the PWM waveforms generated from microcontroller MCB167 using the derived equation. In Figure 3.11 (a) the PWM signals $V_1(k)$, $V_2(k)$ and 50 Hz square waves for $m_i = 0.4$, $m_f = 20$ are depicted, while Figure 3.11 (b) show the same signals for $m_i = 0.8$, $m_f = 20$. The signals shown in the both figures are using time scale of 4ms/div and voltage scale of 5V/div. It can be observed that the signals generated from the microcontroller board are identical with the signals obtained in simulation work. Recall that PWM signal $V_2(k)$ only exist when m_i is greater than 0.3. For m_i less than 0.5, $V_2(k)$ is zero as evidently seen in both figures.



(a)

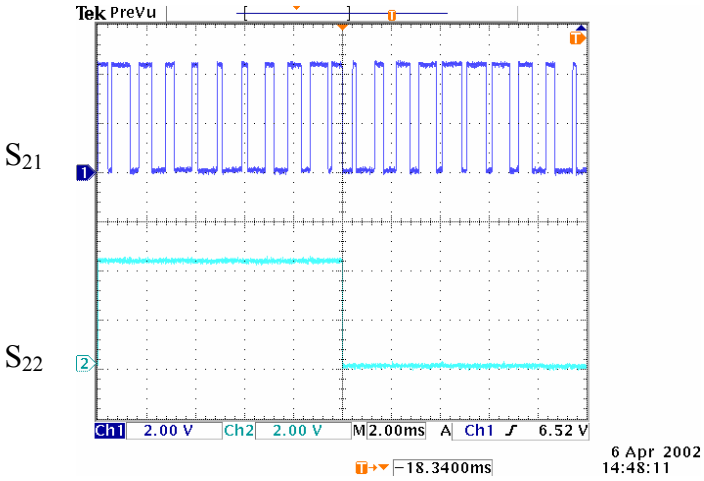


(b)

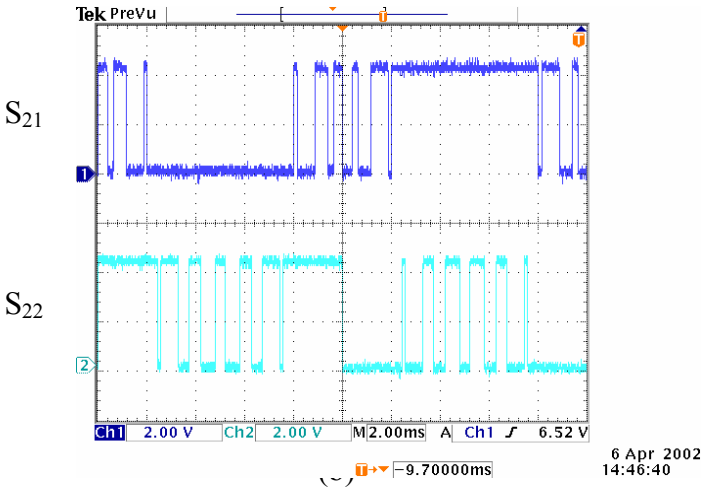
Vertical scale 5V/div. Horizontal scale 2ms/div.

Figure 3.11: PWM output signals from microcontroller port for (a) $m_a = 0.4$, $m_f = 20$ and (b) $m_i = 0.8$, $m_f = 20$.

As perviously mentioned, to obtain signals for S_{21} and S_{22}, signals $V_1(k)$ and $V_2(k)$ are ex-ored with the 50Hz square wave. Figure 3.12 (a) and 3.12 (b) represent the signals for gate drive S_{21} and S_{22} for $m_i = 0.4$, $m_f = 20$ and $m_i = 0.8$, $m_f = 20$, respectively.



(a)

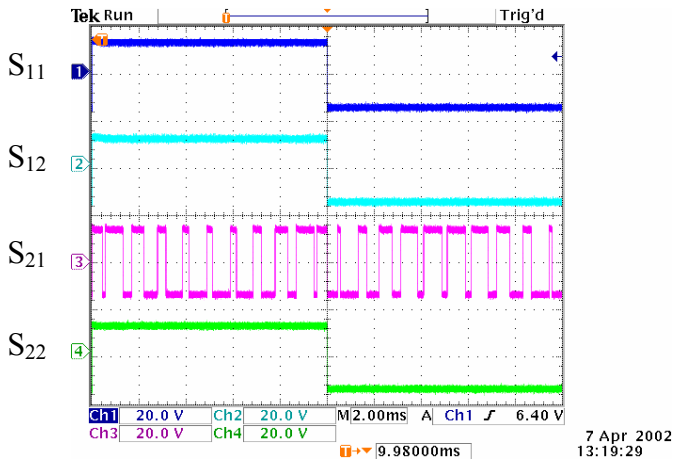


Vertical scale 5V/div. Horizontal scale 2ms/div.

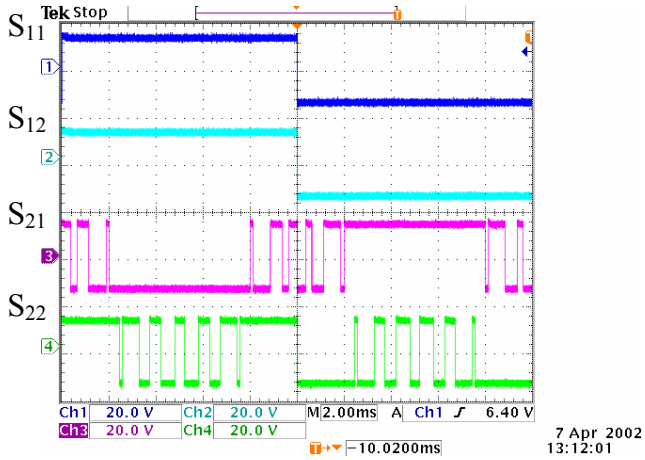
Figure 3.12: Signals for gate drive S_{21} and S_{22} (a) $m_i = 0.4$, $m_f = 20$ and (b) $m_i = 0.8$, $m_f = 20$.

Figure 3.13 (a) and 3.13 (b) represent the gate drive signals of S_{11}, S_{12}, S_{21} and S_{22} for $m_i = 0.4$, $m_f = 20$ and $m_i = 0.8$, $m_f = 20$, respectively. It can be seen that the waveforms of square wave and PWM signals (S_{21} and S_{22}) are identical with the output signal from microcontroller and digital circuit, respectively. However the

amplitude of these signals are increased from 0V and +5V to -15V and +15V to drive the IGBT.



(a)



(b)

Vertical scale 20V/div. Horizontal scale 2ms/div.

Figure 3.13: Signals of S_{11}, S_{12}, S_{21} and S_{22} for (a) $m_i = 0.4$, $m_f = 20$ and (b) $m_i = 0.8$, $m_f = 20$.

CHAPTER IV
RESULTS AND ANALYSES

4.1 Introduction

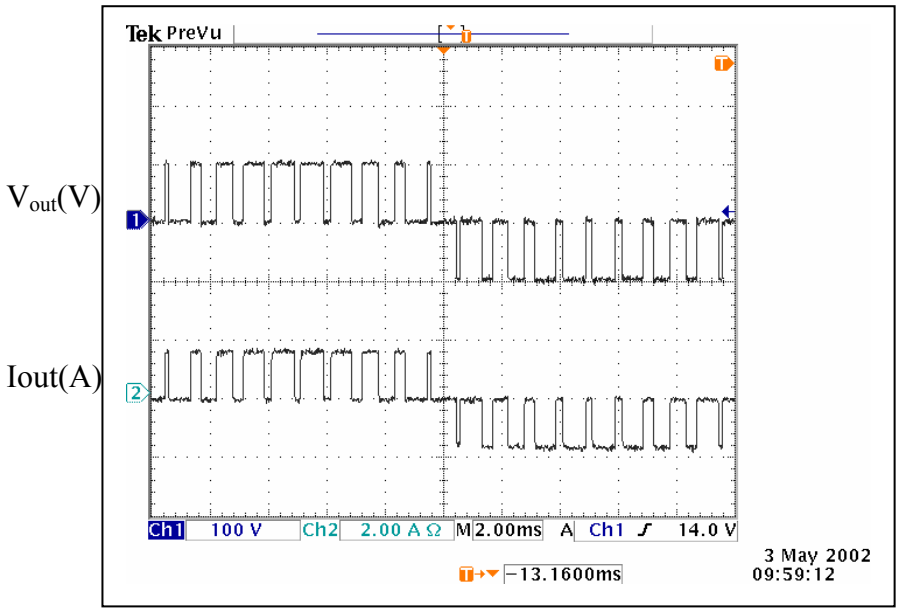
This chapter presents the practical results obtained from the MSMI prototype described in Chapter III. As a standard measure to evaluate the performance of inverter, analysis on the Total Harmonic Distortion (THD), Harmonic Loss Factor (HLF) and Second-order Distortion Factor (DF_2) for a five-level MSMI is carried out. The analysis includes theoretical and practical results of five-level MSMI in comparison to conventional two-level inverter. The variations and differences between those results are explained. Finally the effectiveness and performance of the proposed modulation scheme when employed to MSMI is evaluated.

4.3 Results

This section presents the selected voltage output and current output waveforms for the five-level MSMI obtained from experimental test-rig. These results are compared to the simulation. The inverter input voltages are fixed at 100V dc for each module and the inverter load is a purely resistive.

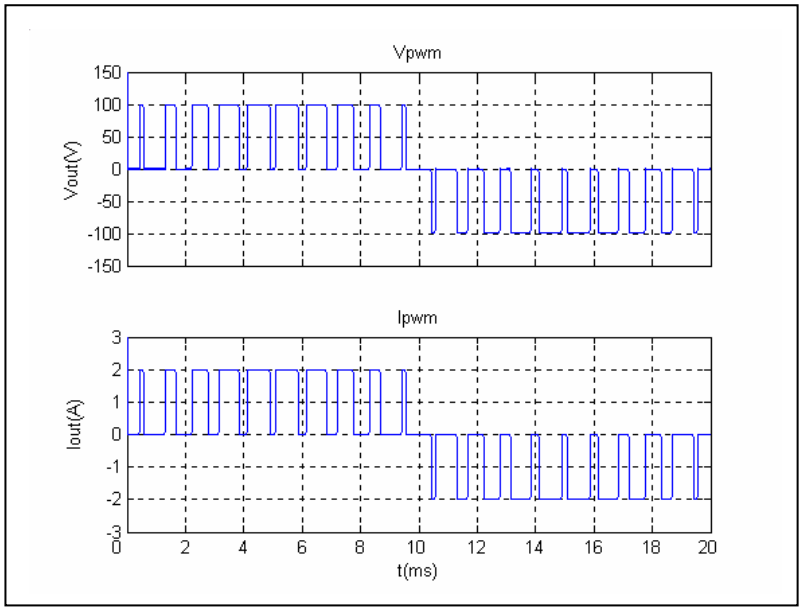
4.2.1 Inverter Output Voltage and Current

Figure 4.1 (a) shows the oscilogram of the output voltage and current of the inverter for $m_i = 0.4$ and $m_f = 20$. The figure shows that the practical result obtained from test-rig is in good agreement with the simulation result, which is shown in Figure 4.1 (b). The output voltage and output current for practical and simulation results is about $56V_{rms}$ and $1.13A_{rms}$. For the case of $m_i = 0.8$ and $m_f = 20$ shown in Figures 4.2 (a) and 4.2 (b), the consistency between the practical and simulation results holds. For this case, the output voltage and output current for practical and simulation results is about $112V_{rms}$ and $2.26A_{rms}$, which is doubled compared to the previous case. Since the measurement is made under pure resistance load, the current waveforms are in phase with the voltage waveform, which is clearly shown by these results.



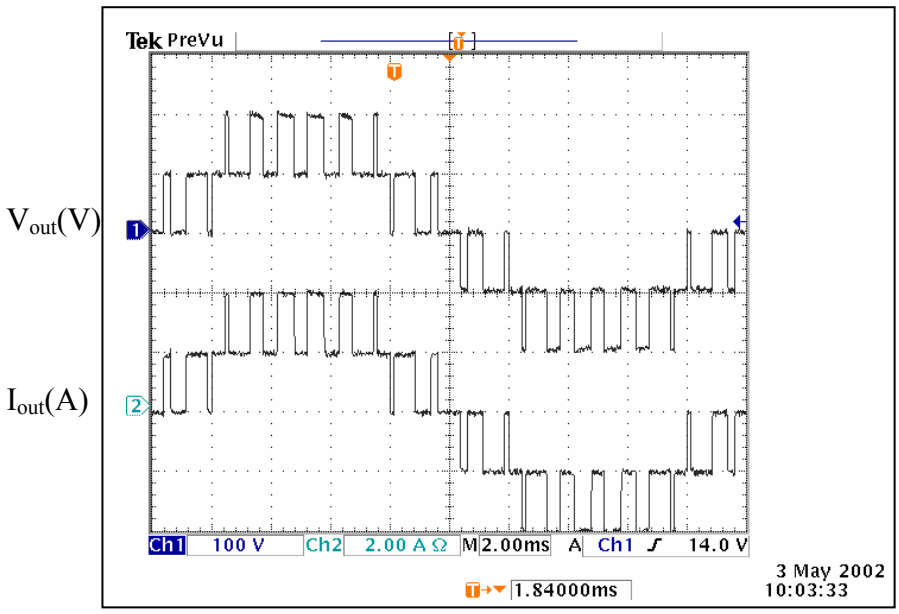
Top trace: V_{out}. Vertical scale 100V/div.
Bottom trace: I_{out}. Vertical scale 2A/div.
Horizontal scale 2ms/div.

Figure 4.1 (a): Practical result for $m_i = 0.4$; $m_f = 20$.



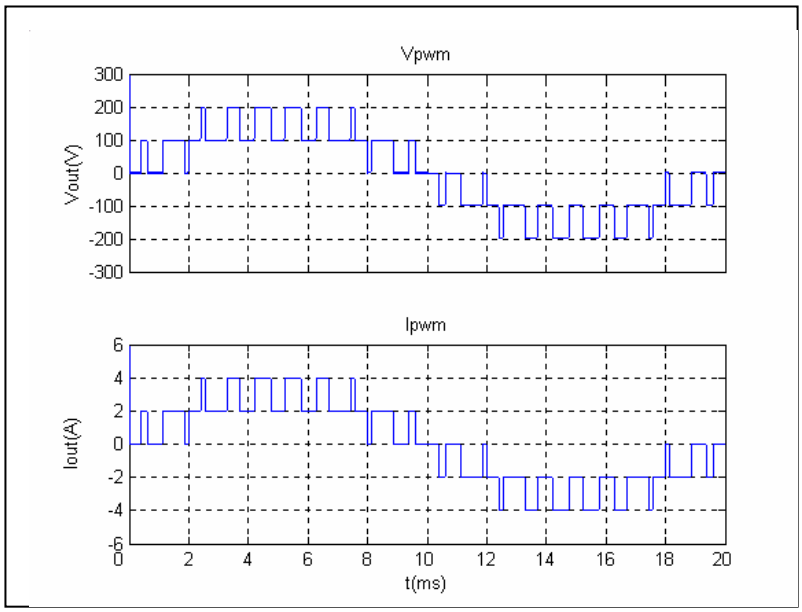
Top trace: V_{out}. Vertical scale 100V/div.
Bottom trace: I_{out}. Vertical scale 2A/div.
Horizontal scale 2ms/div.

Figure 4.1 (b): Theoretical result for $m_i = 0.4$; $m_f = 20$.



Top trace: V_{out}. Vertical scale 100V/div.
Bottom trace: I_{out}. Vertical scale 2A/div.
Horizontal scale 2ms/div.

Figure 4.2 (a): Practical result for $m_i = 0.8$; $m_f = 20$.



Top trace: V_{out}. Vertical scale 100V/div.
Bottom trace: I_{out}. Vertical scale 2A/div.
Horizontal scale 2ms/div.

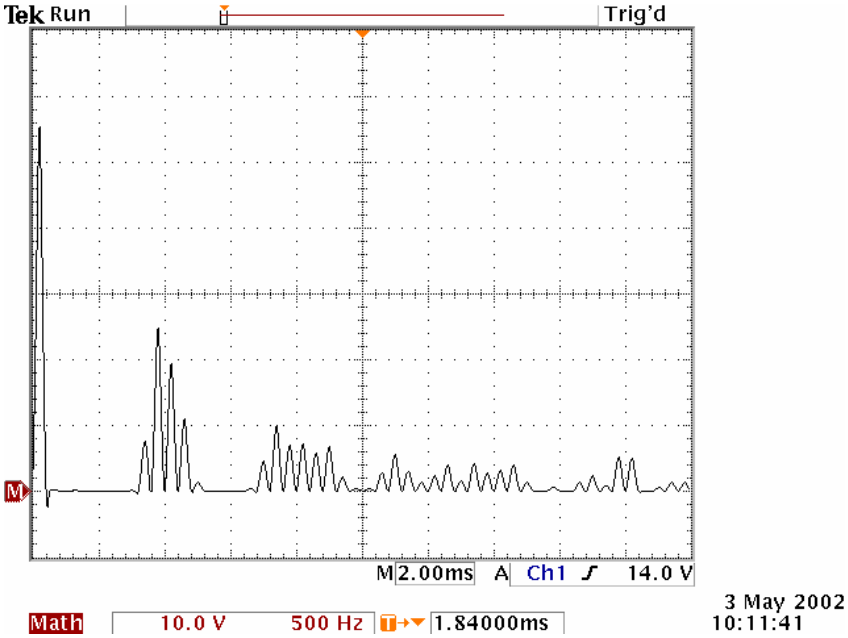
Figure 4.2 (b): Theoretical result for $m_i = 0.8$; $m_f = 20$.

4.2.2 Harmonic Spectrum

Performance of an inverter is determined by its harmonic content. This section presents the harmonic spectrum of a modular structured five-level inverter under different modulation indexes and ratios. Since the inverter has a pure resistive load, the harmonic spectrum for its output current is similar with the output voltage. Hence only harmonic spectrum of the latter is shown.

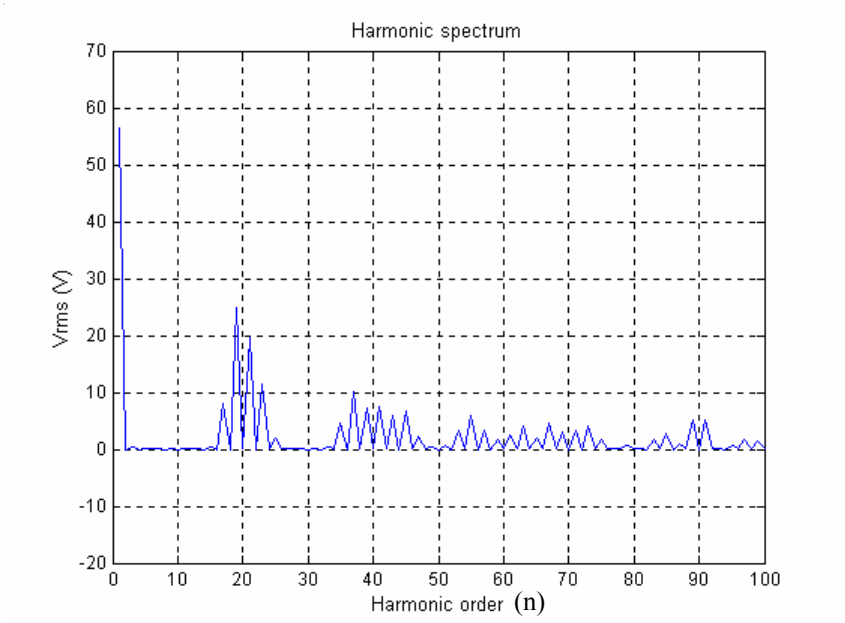
For the case of $m_f = 20$ and $m_i = 0.4$, the practical result of output voltage harmonic spectrum are shown in Figures 4.3 (a). The theoretical harmonic spectrum is calculated using the derived equations in Chapter IV. The equations, namely (4.18) and (4.32) for the case when $m_i \leq 0.5$ and $0.5 < m_i \leq 1$ respectively are subsequently programmed and plotted using MATLAB m-file. The theoretical spectrum for the similar case is shown in Figure 4.3 (b). By comparing Figures 4.3 (a) and 4.3 (b), it can be clearly observed that the harmonics incidences for $m_i \leq 0.5$ agree closely with theoretical predictions. The proposed modulation scheme produces only odd harmonic for even modulation ratio. Furthermore, harmonics at the carrier and the multiples of carrier frequency do not exist at all. These observations confirm the analysis, whereby it was concluded that for even modulation ratio, even harmonics are absent.

The figures indicate that the magnitude of fundamental harmonic is $53.8V_{rms}$ for practical result and $54.56V_{rms}$ for simulation result. The tabulated results shown in Table 4.1 indicate that the first significant harmonic is located at the 19^{th}. Practically, the magnitude of this harmonic is $24.8V_{rms}$, which is 44.44% of the normalized fundamental. Using simulation, the magnitude is $24.7733V_{rms}$ and the ratio is 43.8%, which proves the validity of the drived equations. To demonstrate the concurrence between simulated and theoretical results, the value of the first group of significant harmonic order is tabulated in Table 4.1. It can be concluded that the results obtained from test-rig i.e. in a good agreement with the theoretical predictions.



Vertical scale 10V/div.
Horizontal scale 500Hz/div.

Figure 4.3 (a): Practical harmonic spectrum of output voltage for $m_i = 0.4$; $m_f = 20$.



Vertical scale 10V/div.
Horizontal scale 500Hz/div.

Figure 4.3 (b): Theoretical harmonic spectrum of output voltage for $m_i = 0.4$; $m_f = 20$.

Table 4.1: Predicted and measured values of the first group of significant harmonic order for $m_i = 0.4$; $m_f = 20$.

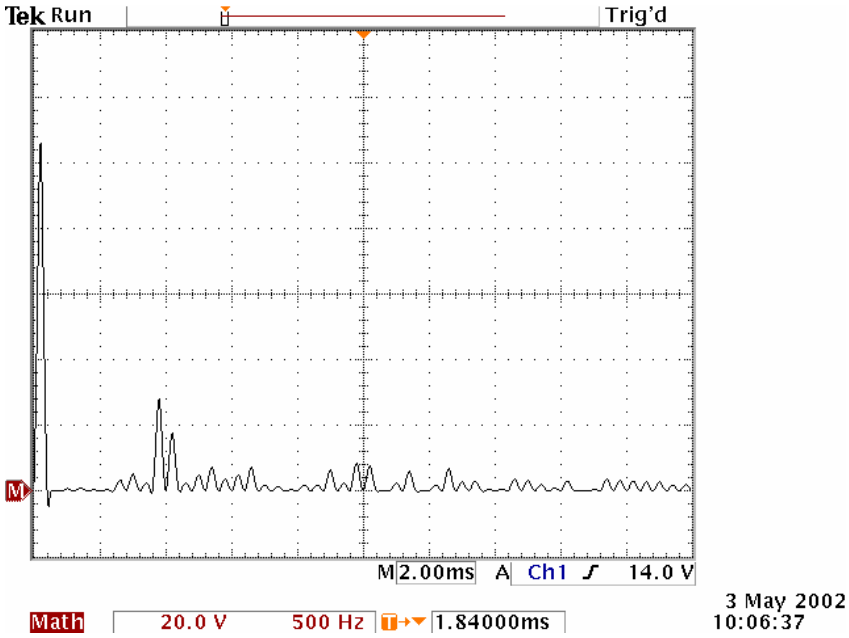
Number of Harmonic order	Frequency (Hz)	Magnitude of harmonic (V)	
		Simulation	Measured
17	850	8.0172	7.6
19	950	24.7733	24.8
21	1050	19.7115	19.8
23	1150	11.3250	11.4
25	1250	1.8777	1.6

Note: Simulation values are defined from the harmonic figures (after zoomed). Measured readings are taken directly from numerical values of harmonics given by Tektronix TDS3054 osiloscope

For the case of $m_f = 20$; $m_i = 0.8$, practical and theoretical results of the output voltage harmonic spectrum are illustrated in Figure 4.4 (a) and 4.4 (b), respectively. Again, it can be seen that as far as the harmonics incidences are concerned, the practical results agree with theory. The figures indicate that the magnitude of fundamental harmonic is $107V_{rms}$ for practical result and $113.12V_{rms}$ for simulation result The first significant harmonic is located at 19^{th} with magnitude of $24.9087V_{rms}$ or 23.79% of the normalized fundamental. From the test-rig, the same harmonic is $27.6V_{rms}$ or 23.79% of the fundamental. Recall that for five-level inverter, $m_i = 0.4$ is equivalent to $m_i = 0.8$ for a three-level inverter. As concluded by Agelidis [36], for an equivalent modulation index, the significant harmonic of a five-level is half compared to a three-level inverter.

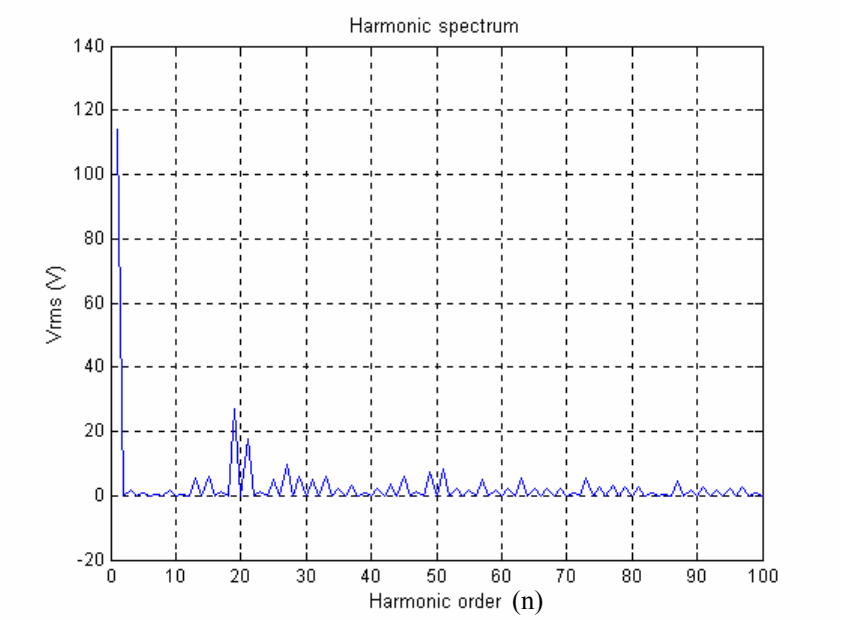
Table 4.2 tabulates the predicted and numerical results of the first group of significant harmonics. The comparison shows that for 13^{th} and 17^{th} harmonic order, the error is quite significant. The possible explanation for this would be the assumptions that were made when deriving the equation. In the mathematical formulation, inverter input voltage is assumed a pure dc voltage, but in practice there are ripples in dc voltages obtained from power supply. However, other harmonics especially the first significant one exhibits small error. In general, the simulation and

practical results can be considered close enough to validate the correctness of the mathematical analysis.



Vertical scale 20V/div.
Horizontal scale 500Hz/div.

Figure 4.4 (a): Practical harmonic spectrum of output voltage for $m_i = 0.8$; $m_f = 20$.



Vertical scale 20V/div.
Horizontal scale 500Hz/div.

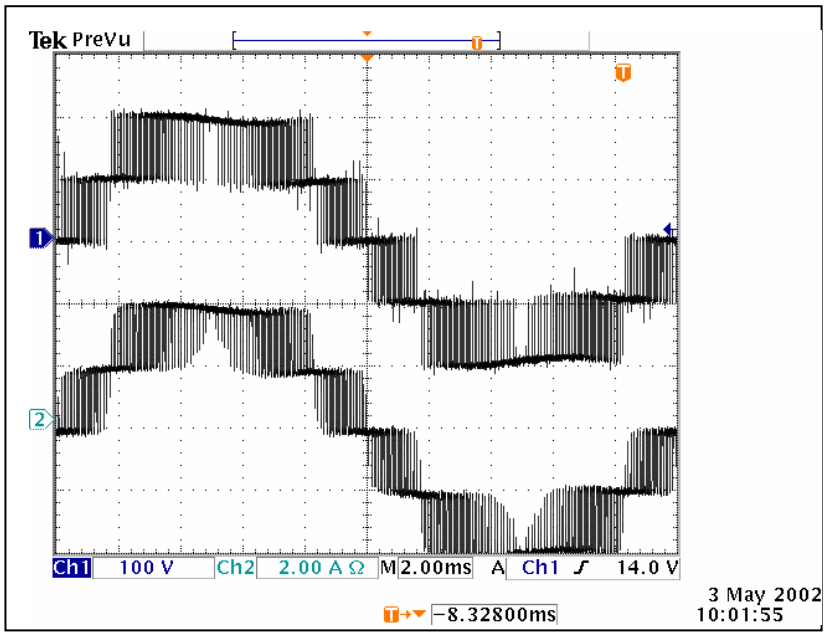
Figure 4.4 (b): Theoretical harmonic spectrum of output voltage for $m_i = 0.8$; $m_f = 20$.

Table 4.2: Predicted and measured values of the first group of significant harmonic order for $m_i = 0.8$; $m_f = 20$.

Number of Harmonic order	Frequency (Hz)	Amplitude of harmonic (V)	
		Simulation	Measured
13	650	3.5870	4.4
15	750	3.9801	3.6
17	850	1.1052	2.0
19	950	24.9087	27.6
21	1050	17.4743	18.0

4.2.3 Harmonics Performance at Higher Modulation Ratio

To evaluate the modulation scheme performance at higher frequency, test at modulation ratio equal to 200 is carried out. This ratio corresponds to switching frequency of 10 kHz. The practical and simulation results for this case when modulation index equals 1.0 is shown in Figure 4.5 (a) and 4.5 (b), respectively. It can be seen that at high switching frequency, the practical result in a good agreement with the simulation result. The rms output voltage and output current for practical and simulation results is about 112V and 2.26A The respective harmonic spectrum, as illustrated in Figure 4.6 (a) and 4.6 (b), are also consistent with each other.

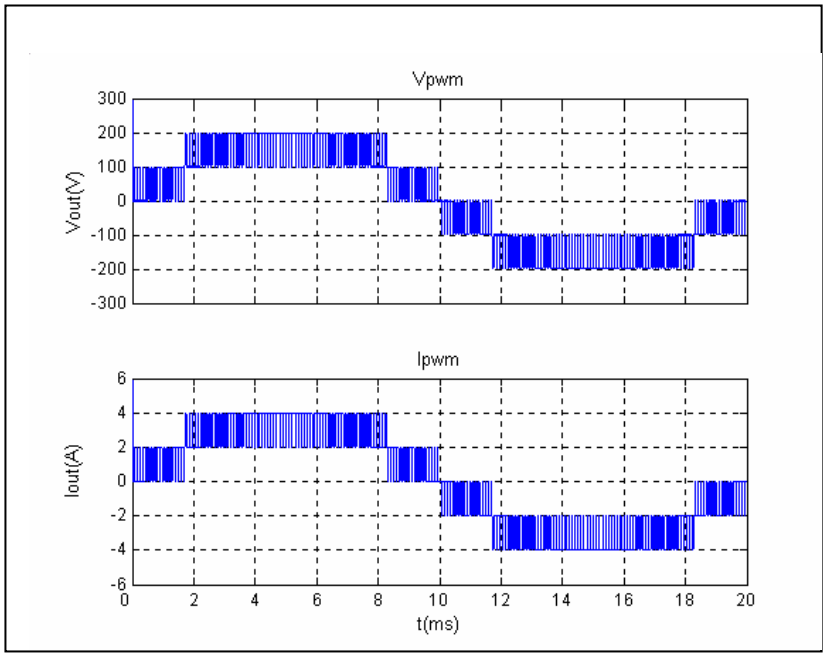


V_{out}(V)

I_{out}(A)

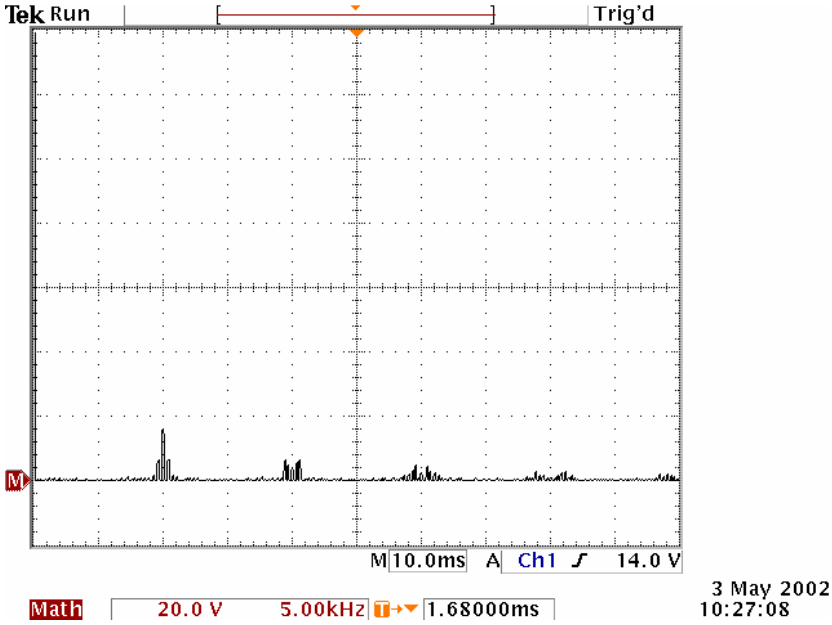
Top trace: V_{out}. Vertical scale 100V/div.
Bottom trace: I_{out}. Vertical scale 2A/div.
Horizontal scale 2ms/div.

Figure 4.5 (a): Practical result for $m_i = 1.0$ $m_f = 200$.



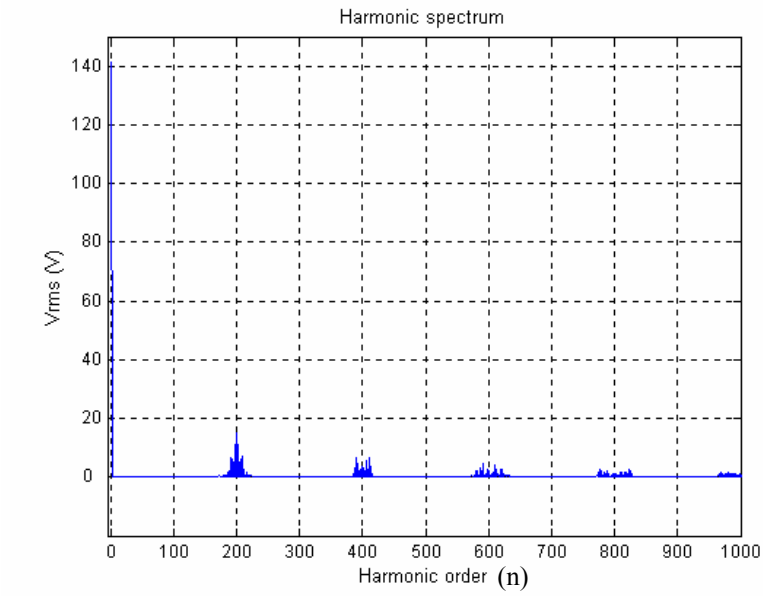
Top trace: Output voltage. Vertical scale 100V/div.
Bottom trace: Output current. Vertical scale 2A/div.
Horizontal scale 2ms/div.

Figure 4.5 (b): Simulation result for $m_i = 1.0$ $m_f = 200$.



Vertical scale 20V/div.
Horizontal scale 5kHz/div.

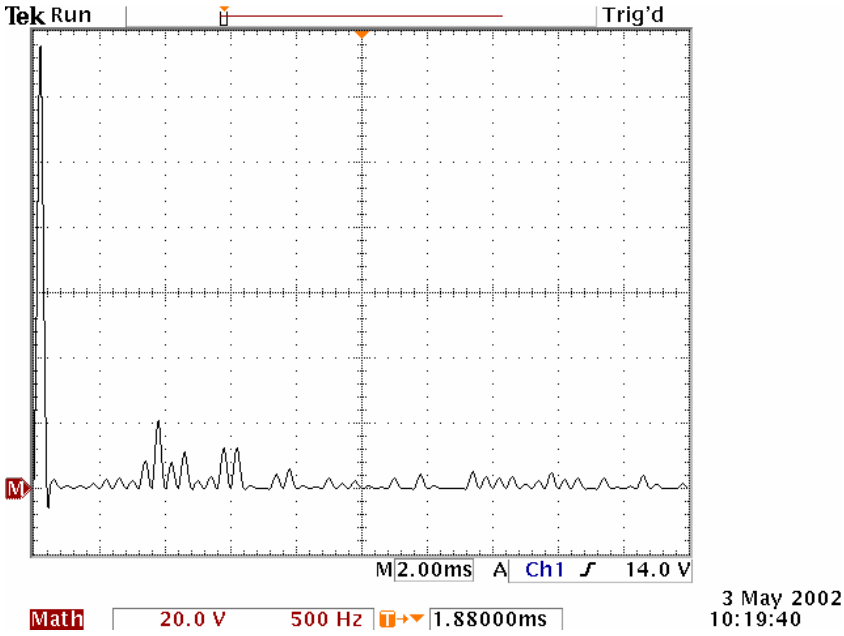
Figure 4.6 (a): Practical harmonic spectrum of output voltage for $m_i = 1.0$ and $m_f = 200$.



Vertical scale 20V/div.
Horizontal scale 5kHz/div.

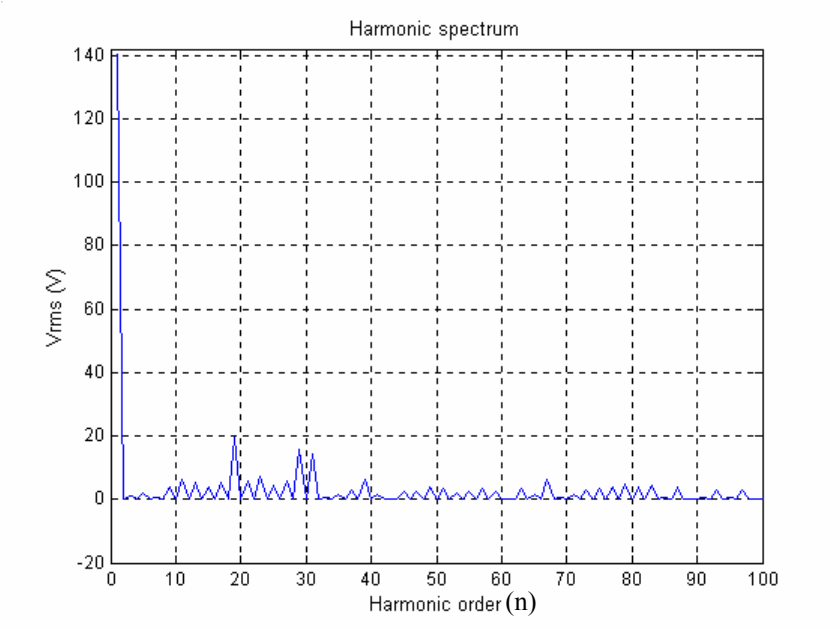
Figure 4.6 (b): Theoretical harmonic spectrum of output voltage for $m_i = 1.0$ and $m_f = 200$.

Figures 4.7 (a) and 4.7 (b) depict the spectra of the output voltages for $m_i = 1.0$ and $m_f = 20$. Comparing to the previous test, i.e $m_i = 1.0$ and $m_f = 200$, all the harmonics are shifted to higher frequencies in accordance to increase in the modulation ratio. This is consistent with the general PWM modulation theory. Numerically, it was found that first significant harmonic is slightly decreased when the modulation ratio is changed but the difference is relatively small. For this particular case, magnitude of the first significant harmonics are 13.81% and 10.74% compared to the fundamental harmonic for the $m_f = 20$ and $m_f = 200$, respectively. The increase of the former may be attributed to the overlaps that occur when the modulation ratio is insufficiently high.



Vertical scale 20V/div.
Horizontal scale 500Hz/div.

Figure 4.7 (a): Practical harmonic spectrum of output voltage for $m_i = 1.0$ and $m_f = 20$.



Vertical scale 20V/div.

Horizontal scale 500Hz/div.

Figure 4.7 (b): Theoretical harmonic spectrum of output voltage for $m_i = 1.0$ and $m_f = 20$.

4.3 Generalized of Harmonics Table for Five-level Inverter

The harmonics in the PWM inverter output voltage waveform appear as sidebands, clustered around the switching frequency and its multiples, i.e m_f, $2m_f$, $3m_f$ etc. This general pattern is true for all values of m_i in the range 0 through 1.0. Table 4.3 attemps to generalize the harmonic amplitudes with respect to the fundamental voltage for a five-level inverter. The table is created using the calculated values from equation (4.18) and (4.32).

As previously discussed, the amplitude of sidebands harmonic is somewhat larger when the inverter is switching at low frequency. The increase may be attributed to the overlaps that occur between the clusters when the modulation ratio is insufficiently high. From numerous trials, it was concluded that the minimum modulation ratio that guarantee no overlaps occurence is 30. Therefore, the table is sufficiently accurate for modulation ratio greater than 30. It can be observed that the amplitude of the fundamental component in the output voltage varies linearly with

m_i. It also can be seen that the numbers of sidebands at the first significant harmonic group (m_f), increased in proportional to m_i.

Table 4.3: Generalized harmonics of voltage output for large m_f in term of the normalized fundamental.

m_i	0.2	0.4	0.6	0.8	1.0
Fundamental	0.2	0.4	0.6	0.8	1.0
$m_f \pm 1$	0.1642	0.1632	0.1079	0.1542	0.0998
$m_f \pm 3$	0.0109	0.0656	0.0634	0.0145	0.0774
$m_f \pm 5$		0.0047	0.0624	0.0454	0.0010
$m_f \pm 7$			0.0076	0.0534	0.0425
$2m_f \pm 1$	0.0801	0.0523	0.0245	0.0049	0.0221
$2m_f \pm 3$	0.0339	0.0522	0.0425	0.0115	0.0185
$2m_f \pm 5$	0.0027	0.0445	0.0455	0.0375	0.0091
$2m_f \pm 7$			0.0442	0.0295	0.0358
$3m_f \pm 1$	0.0035	0.0163	0.0384	0.0155	0.0152
$3m_f \pm 3$	0.0442	0.0265	0.0182	0.0295	0.0035
$3m_f \pm 5$	0.0105	0.0338	0.0045	0.0145	0.0112
$3m_f \pm 7$		0.0286	0.0064	0.0179	0.0095
$4m_f \pm 1$	0.0262	0.0021	0.0161	0.0071	0.0075
$4m_f \pm 3$	0.0299	0.0055	0.0144	0.0085	0.0085
$4m_f \pm 5$	0.0204	0.0185	0.0088	0.0118	0.0022
$4m_f \pm 7$	0.0038	0.0157	0.0080	0.0138	0.0042

4.4 Performance Indexs for the Proposed Modulation Scheme

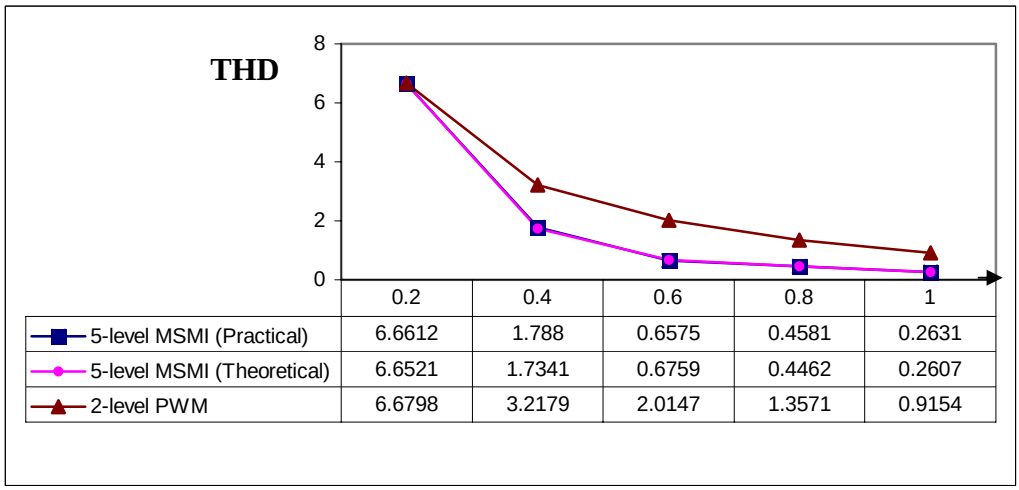
This section is dedicated to analyse the performance of five-level MSMI using the proposed modulation scheme. Analyses on Total Harmonic Distortion (THD), Harmonic Loss Factor (HLF) and Second Order Distortion Factor (DF_2) are carried out. Practical and theoretical performance indexes of five-level MSMI using the proposed modulation scheme are compared with conventional two-level SPWM inverter.

4.4.1 Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the most common power quality index to describe the quality of power electronic converter [49,50]. In general, all the output voltage of power electronic converters is not purely sinusoidal. The THD of the output voltage can be defined as:

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_h^2}}{V_1} \tag{4.1}$$

Where *n* denotes the harmonic order and 1 is the fundamental quantity. For inverter application, THD represents how close the ac output waveform with pure sinusoidal waveform. A high-quality inverter system should have low THD. Figure 4.8 shows the comparison of the THD between a five-level single-phase MSMI and a conventional two-level inverter configuration. The figure shows that for both cases, a poor THD are obtained when the inverter operated at low modulation index. This is to be expected because at $m_i \leq 0.5$, the MSMI essentially behaves like a conventional three-level inverter. A better THD is obtained when the inverter operated at higher modulation index. For example, at modulation index equals 1.0, it was found that THD for a MSMI inverter is very much better compared to a conventional two-level inverter.



	0.2	0.4	0.6	0.8	1
5-level MSMI (Practical)	6.6612	1.788	0.6575	0.4581	0.2631
5-level MSMI (Theoretical)	6.6521	1.7341	0.6759	0.4462	0.2607
2-level PWM	6.6798	3.2179	2.0147	1.3571	0.9154

Figure 4.8: Variation of THD for five-level MSMI and two-level SPWM inverter configuration.

Note: Data for two-level SPWM is obtained from Mohan et al [46].

It is also worthwhile to note that for the MSMI, the calculated value of THD using the derived equations for the harmonics agree closely with the data obtained from the test-rig. For both cases, the calculation for THD is done by considering only the first four harmonic clusters.

4.4.2 Harmonic Loss Factor (HLF)

Another important quality index of PWM technique is related to losses in inverter-fed ac drives. These losses represent harmonic copper loss and are quantified as harmonic loss factor (HLF) [26,51]. The harmonic equivalent circuit of an induction machine can be assumed to be its total leakage reactance at the harmonic frequency. Therefore harmonic current I_n is given by:

$$I_n = \frac{V_n}{2\pi n f L_e} \tag{4.2}$$

Where:

V_n harmonic voltage

L_e leakage inductance of the motor

N order of the harmonic

V_{L1} inverter output voltage (determine by modulation index)
In a variable speed ac drive it is necessary to main constant volt/hertz.

Therefore, the fundamental component of the inverter output voltage V_{L1} is proportional to the operating frequency f. Equation (4.2) can be rewritten taking L_e as the p.u quantity:

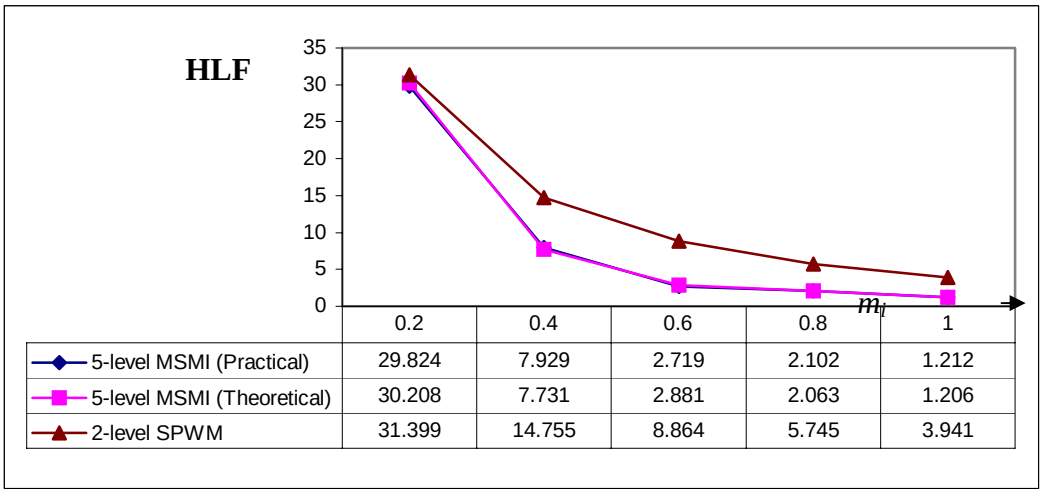
$$I_n \alpha \frac{V_n}{n V_{L1}} \tag{4.3}$$

The HLF, which is proportional to total rms harmonic current, can be defined as [26]:

$$\mathrm{HLF} = \frac{100}{V_{L1}} \sqrt{\sum_{n=5}^{\infty} \left[\frac{V_n}{n} \right]^2} \tag{4.4}$$

A good inverter-fed ac drive system should have a low HLF.

Figure 4.9 shows the variation of HLF for single-phase five-level MSMI and a conventional two-level inverter. The figure shows that for both inverter types, a poor HLF are obtained when the inverter operated at low modulation index. However, at higher modulation index, the HLF improve tremendously. For example, at m_i = 1.0, the HLF of the MSMI is reduced to about one third of the two-level inverter. The result is expected because in general, the HLF will follow the trend of THD.



	0.2	0.4	0.6	0.8	1
5-level MSMI (Practical)	29.824	7.929	2.719	2.102	1.212
5-level MSMI (Theoretical)	30.208	7.731	2.881	2.063	1.206
2-level SPWM	31.399	14.755	8.864	5.745	3.941

Figure 4.9: Variation of HLF for five-level MSMI and two-level SPWM inverter configuration.

Note: Data for two-level SPWM is obtained from Mohan et al [46].

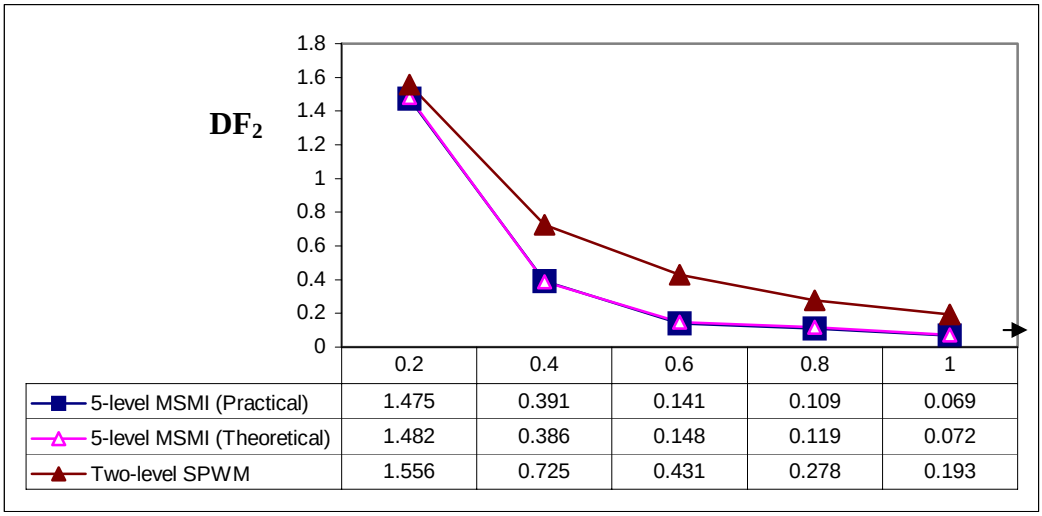
4.4.3 Second Order Distortion Factor (DF_2)

Inverter power supplies such as uninterruptible power supplies (UPS) employ an *L*-*C* filter between the inverter and the load. The main purpose of this filter is to provide harmonic attenuation, which is proportional to the square of the order (*n*) of the harmonic. A distortion factor that represents total harmonic content at the output of a second-order filter as can be described as [26]:

$$DF_2 = \frac{100}{V_{L1}}\sqrt{\sum_{n=5}^{\infty}\left[\frac{V_n}{n^2}\right]^2} \qquad (4.5)$$

For an inverter power supply a PWM scheme that results in minimum DF_2 is desirable.

Figure 4.10 illustrates the DF_2 variation for a single-phase five-level MSMI and a two-level conventional inverter. The figure demonstrates that the DF_2 for five-level MSMI and two-level inverter is about equal when the modulation index is low. However as the index increasing, the DF_2 for the MSMI reduces significantly compared to two-level inverter. At $m_i = 1.0$, it can be observed that DF_2 for MSMI is three times better than the two-level inverter.



	0.2	0.4	0.6	0.8	1
5-level MSMI (Practical)	1.475	0.391	0.141	0.109	0.069
5-level MSMI (Theoretical)	1.482	0.386	0.148	0.119	0.072
Two-level SPWM	1.556	0.725	0.431	0.278	0.193

Figure 4.10: Variation of DF_2 for five-level MSMI and two-level SPWM inverter configuration.

Note: Data for two-level SPWM is obtained from Mohan et al [46].

From the analyses for THD, HLF and DF_2 above, it can be concluded that the performance of MSMI as far better than the conventional two-level inverter. It should noted that for purpose of simplicity analysis was carried for one particular value of modulation ratio i.e $m_f = 40$. However, it was found that for other values of m_f (above 30), it trend does not change very much. This is in conformity with the conclusion described in [26]. It also important to note that the number of harmonics considered in all calculation above is only up to the fourth cluster.

CHAPTER V

SUMMARY, CONTRIBUTIONS AND SUGGESTION FOR FURTHER WORK

5.1 Summary of the Research

As a prelude to the report, a brief introduction on inverter that includes an overview of inverter power circuit topologies, switching strategies and modulation techniques has been presented. Several important multilevel inverter topologies namely Diode Clamped Multilevel Inverter (DCMI), Flying Capacitor Multilevel Inverter (FCMI) and Modular structured Multilevel Inverter (MSMI) basic structure have been described. Their merits and disadvantages have been discussed. The inverter topology selection basically depends on the application and the features of their dc sources. It was concluded that for application that requires separated dc sources such as renewable energy power inverter, MSMI is the most suitable choice. This topology does not suffer unbalance voltage problem and requires the least number of component compared to its rival.

Several multilevel switching techniques proposed by previous researcher are discussed. However only sinusoidal pulse width modulation (SPWM) is explained in detail since it is directly related to this work. This PWM technique is simple and it promises significant improvement to the harmonic distortion when applied to multilevel inverter. Using unipolar regular sampling, a new PWM modulation scheme for MSMI is proposed. It is based on the intersection of several modified modulating waveforms with a single carrier waveform.

In order to implement the switching technique into hardware, a 16-bit microcontroller (SIEMENS SAB-C167CR-LM) is chosen to generate the PWM pulses for a single-phase, five-level MSMI. Then a low-power test-rig has been constructed and the performance of the inverter with the proposed switching scheme is analyzed.

From the comparison between the practical and theoretical work, it can be concluded that the practical results are in close agreement with the theory. In harmonic analysis, it was found that only odd harmonic order is exists for the modulation scheme since the modulation ratio is limited to even number. The positions of the harmonics depend on the modulation ratio. All the harmonics are shifted to high frequencies when the modulation ratio increased. The amplitude of each harmonic depends on the modulation index, the better harmonic performance can be obtained when modulation index get closer to 1.0. It also found that for the same modulation index, the harmonics amplitude of five-level inverter is reduced to half compared to three-level inverter. Analyses on Total Harmonic Distortion (THD), Harmonic Loss Factor (HLF) and Second Order Distortion Factor (DF_2) conclude that the harmonic performance of modular structured five-level inverter using the proposed modulation scheme is superior compared to conventional two-level inverter.

5.2 Contributions

The aim of the research is to develop a digital PWM scheme for multilevel inverter suitable for photovoltaic application. The proposed modulation scheme is based on symmetric regular sampling SPWM technique using multiple modulating signals with a single carrier. This study has led to two important contributions. The derived equations based on the proposed modulation scheme were proven suitable for an online microprocessor PWM generation. It has been shown that the gating signals for a five-level inverter can be easily generated using a fixed-point (integer) microprocecessor. The second contribution is the analytical method to obtain the Fourier coefficients for a five-level MSMI using the proposed modulation scheme. The harmonic spetra that resulted from the analysis was proven to be within good agreement with experimental work carried out on a five-level MSMI test-rig.

From the theoretical and practical results, it can be seen that the harmonic spectrum produced from the proposed modulation scheme is very similar with Phase Opposition Disposition (POD) scheme proposed by previous researchers. This is because the end-results of both modulation techniques are quite similar although the approaches taken are significantly different. Traditional POD scheme uses a pure sinusoidal modulating signal modulated with several carrier signals, while the

proposed scheme is using a single carrier signal modulated with several modified sinusoidal modulating signals.

There are some significant advantages with the newly proposed modulation technique. The trigonometric equations to generate the switching angles prove to be quite simple and can easily implemented using a fix point microprocessor. It is also shown by simulation that the same equation could be used to generate gating signals for N-level inverter. Therefore, it is anticipated that the proposed modulation technique can be employed to N-level inverter without any difficulty.

5.3 Suggestion for Further Work

The proposed switching algorithm is tested only for purely resistive load in linear modulation. To test the full capability of the developed system, a reactive load such as R-L load test and inverter-fed ac drive test should also be performed. The test should carry out in both modulation range, i.e linear and over modulation.

A more sophisticated and high-resolution processor can be implemented on the inverter system. It is expected by using the floating-point processor such as DSP, the proposed swithing algorithm will produce more accurate results, especially at high modualtion ratio.

It is also possible the derived equations be used in multi-phase and higher-level inverter. The general equation should be extended to other multilevel inverter topologies such as Diode Clamped Multilevel Inverter (DCMI) and Flying Capacitor Multilevel Inverter (FCMI).

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