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Design and Implementation of a Single Input Fuzzy Logic Controller for Boost Converters

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Abstract

This paper describes the design and hardware implementation of a Single Input Fuzzy Logic Controller (SIFLC) to regulate the output voltage of a boost power converter. The proposed controller is derived from the signed distance method, which reduces a multi-input conventional Fuzzy Logic Controller (CFLC) to a single input FLC. This allows the rule table to be approximated to a one-dimensional piecewise linear control surface. A MATLAB simulation demonstrated that the performance of a boost converter is identical when subjected to the SIFLC or a CFLC. However, the SIFLC requires nearly an order of magnitude less time to execute its algorithm. Therefore the former can replace the latter with no significant degradation in performance. To validate the feasibility of the SIFLC, a 50W boost converter prototype is built. The SIFLC algorithm is implemented using an Altera FPGA. It was found that the SIFLC with asymmetrical membership functions exhibits an excellent response to load and input reference changes.

Key Words: Boost Converter, Field Programmable Gate Array (FPGA), Fuzzy Logic Controller (FLC), MATLAB, Power Electronics, Signed Distance Method, Single Input FLC

I. INTRODUCTION

Dc to dc boost converters are widely used in power electronics systems. Their application can be found in places ranging from the tiniest cell phones to high power train propulsion systems. Traditionally, the controller for a boost converter is based on classical linear methods such as frequency response and root locus/pole placement techniques. This approach is also known as the "model based" design. It relies heavily on a mathematical model of the converter for accurate control action. An important example of the classical control is the PI controller.

Despite the popularity and simplicity of model based controllers, achieving a high performance response is quite challenging. This is due to the fact that the small signal transfer function of the boost converter, which is the basis of the controller model, exhibits a right-half plane zero that is dependent on the load resistance, R [1], [2]. As a result, a converter can not perform satisfactorily when subjected to large load disturbances, i.e. large changes in R. Furthermore, sensitivity to changes in the system parameters, such as temperature variation and component aging, can be a major concern.

Recently, a new class of controllers which does not depend directly on the converter's model has been proposed. These are known as "non-model based' controllers. Among the most popular of these is the Fuzzy Logic Controller (FLC) [3]–[7]. It is robust, able to adapt well to non-linear variations and has excellent immunity to external disturbances [8]. The accuracy of a conventional FLC (CFLC) is determined by the number of inputs, its corresponding rule table and other fuzzy processes such as fuzzification, rule-based evaluation and defuzzification. Since the control variables are numerous, a speed/accuracy tradeoff is inevitable. The tuning of these parameters is a tedious task and hardware implementation often requires substantial computing resources [10]. Consequently, many researchers opt for a digital signal processor (DSP) for CFLC realization [8]. However, a DSP is costly and may not be justifiable in certain applications. Another way to reduce the computational burden of a CFLC is by reducing the number of rules inference. However, in doing so, the accuracy of its control action is impaired.

In this paper, the design and implementation of a Single Input Fuzzy Logic Controller (SIFLC) for boost converter regulation is proposed. It paves the way for fast FLC execution without compromising the accuracy of the control performance. The SIFLC is based on the "signed distance method" which reduces a multi-input CFLC into a single-input FLC. It effectively simplifies the rule table to a one dimensional array. This reduction allows for the SIFLC control surface to be approximated by a simple piecewise linear (PWL) function which results in a significant simplification of both the design and the parameter tuning.

Although the concept of a SIFLC was introduced by [11] some time ago, only a few researchers in the power converter field have exploited the advantages offered by this method.

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In [12] a SIFLC is combined with a PI controller to regulate the output voltage of a single phase inverter. The outcome showed a marked improvement when compared to a standard PI controller. The application of a SIFLC to control a boost converter was proposed in [13]. Unfortunately, its implementation is carried out using an analog technique, forcing it to inherit the disadvantages of an analog system such as noise, reference voltage sensitivity and component aging. In view of these shortcomings, the digital implementation of a SIFLC is preferable, which is why this work is carried out. The focus is on the digital implementation of a SIFLC to regulate a boost converter using a field programming gate array (FPGA).

This paper begins with a description of the concept of a SIFLC. This description includes the derivation of the reduced rule table using the signed distance method, and the construction of the PWL control surface. For completeness, a brief outline of the boost converter modeling is given. Then using MATLAB/Simulink, a CFLC and the proposed SIFLC are designed and applied to a converter to verify their equivalency. In the experimental section, the proposed SIFLC is implemented using an Altera EP2C35F672C6N FPGA. The performance of the SIFLC for both symmetrical and asymmetrical cases are compared and discussed.

II. Single Input Fuzzy Controller

A. The Signed Distance Method

A typical FLC has two controlled inputs, namely the error (e) and the change of error ($\dot{e}$). Its rule table can be designed based on the general behavior of the boost converter when subjected to a controller which can be summarized as follows:

- When the error signal is too far from the reference point and its derivative has too large a positive sign (in other words the output voltage is smaller than the reference) then duty cycle changes must occur very rapidly with a positive sign, i.e. the duty cycle increases dramatically, forcing an increment of the converter output voltage towards the reference value.
- When the error signal is near the reference point and its derivative has a small positive sign then duty cycle changes are also small.
- When the error signal and its derivative are zero, no changes in the duty cycle are required.

Similar observations are true when the error and the derivative of the error are negatives. Based on these known facts, a two dimensional phase-plane rule table, as shown in Table 1, can be constructed. Such a rule table is known as the FLC with the Toeplitz structure [11]. The main characteristic of this structure is that it has the same output membership in a diagonal direction. Additionally, each point on the particular diagonal line has a magnitude that is proportional to the distance from its main diagonal line L_Z.

In Table I, instead of using two-variable input sets $(e,\dot{e})$, it is possible to obtain the corresponding output, $\dot{u}_o$ using a single variable, d. The latter represents the absolute distance magnitude of the parallel diagonal lines from the main diagonal line L_Z. To derive d, let $Q(e_o,\dot{e}_o)$ be an intersection point of the main diagonal line and a line perpendicular to it

TABLE I
FLC Rule Table with Toeplitz Structure

e / $\dot{e}$	PB	PM	PS	Z	NS	NM	NB
NB	Z	NS	NM	NB	NB	NB	NB
NM	PS	Z	NS	NM	NB	NB	NB
NS	PM	PS	Z	NS	NM	NB	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PB	PB	PM	PS	Z	NS	NM
PM	PB	PB	PB	PM	PS	Z	NS
PB	PB	PB	PB	PB	PM	PS	Z

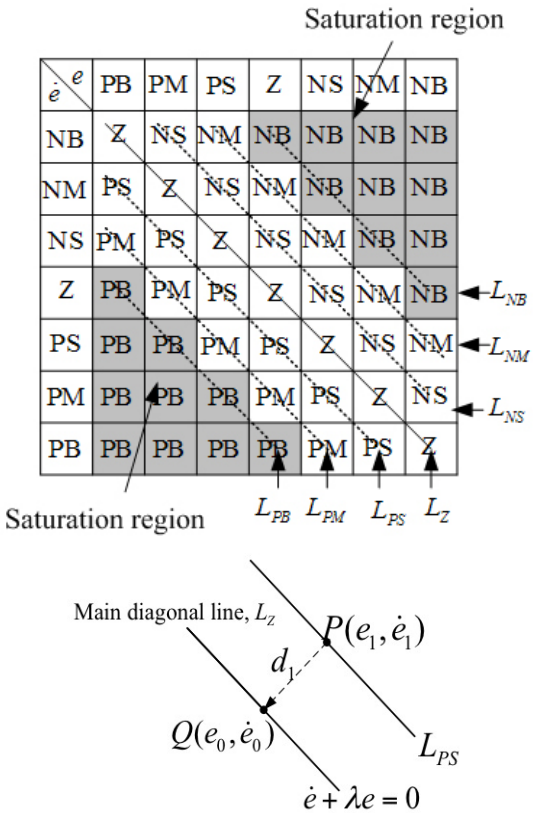


Fig. 1. Derivation of distance variable, d.

from a known operating point P. It can be noted that the main diagonal line can be represented as a straight line function, i.e.

$$\dot{e}+\lambda e=0. \tag{1}$$

The distance d from point $P(e_1,\dot{e}_1)$ to point $Q(e_0,\dot{e}_0)$, can be formulated as:

$$d=\frac{\dot{e}+\lambda e}{\sqrt{1+\lambda^2}}. \tag{2}$$

The derivation of d results in the one-dimensional rule table, depicted in Table II, in which L_{NL}, L_{NM}, L_{NS}, L_Z, L_{PS}, L_{PM} and L_{PL} are the diagonal lines of Table I. These diagonal lines correspond to the new input to Table II, while NL, NM, NS, Z, PS, PM and PL represent the output of the corresponding diagonal lines. The control action of using this table is now exclusively determined by a single input variable d. It is therefore appropriate to called it a Single Input FLC (SIFLC). The only constraint of this method is that it applies only to a FLC with a Toeplitz structure. Fortunately, it was found that most of rule tables used in power electronics converters are of such nature.

The structure of a SIFLC based on the signed distance method and its corresponding rule table can be translated as the block diagram in Fig. 2. The input to the Fuzzy block

TABLE II
The Reduced Rule Table

d	LNL	LNM	LNS	LZ	LPS	LPM	LPL
$\dot{u}_o$	NL	NM	NS	Z	PS	PM	PL

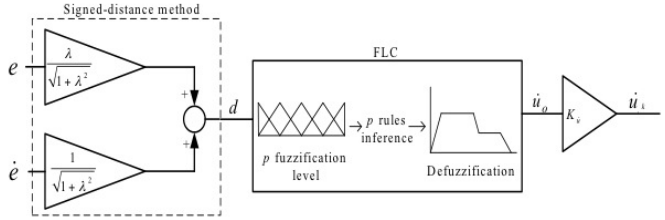


Fig. 2. SIFLC control structure.

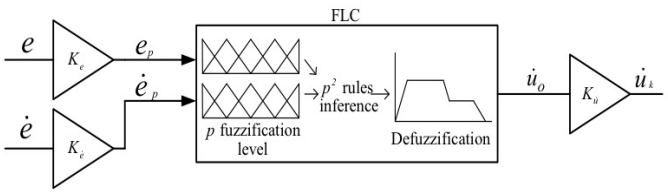


Fig. 3. Conventional FLC control structure.

is d, while its output is the change in the control output, $\dot{u}_o$. The final output is obtained by multiplying $\dot{u}_o$ with an output scaling factor, K_u. For comparison, the structure of a CFLC is shown in Fig. 2. It has two inputs to its Fuzzy block. The main feature of the SIFLC is a significant reduction in the number of rules. For a two input CFLC with a fuzzification level p, the number of rules to be inferred is p^2. An equivalent SIFLC requires only p rules.

B. SIFLC Control Surface

With the rule table reduced to a one-dimensional array, the control surface of the SIFLC can be approximated as a one- dimensional piecewise linear (PWL) function. This can be achieved with the following conditions: (a) the input membership function (MF) is triangular in shape (b) the output membership function is a singleton (c) the fuzzification and defuzzification processes use the Center of Gravity (CoG) method [13]. The main advantage of using a PWL function is that the control surface can be constructed using a simple look-up table that results in a much faster computation time.

Fig.4 shows an example of a PWL control surface which has a constant slope throughout the Universe of Discourse (UoD). This is called a SIFLC with a *symmetrical* MF. Such a surface is achieved when the triangular peaks of the input MF and the spacing in-between the singletons are equal. On the other hand, if the input and output MFs are arranged in unequal spaces, multiple PWL regions with linear lines of different slopes are created. This is shown in Fig. 5. It also introduces the break-point (BP), which is defined as the transition point between two piecewise linear slopes. This type is defined as a SIFLC with an *asymmetrical* MF. Alternatively, an asymmetrical type SIFLC can be constructed by changing the location of the singleton output MF. To obtain more piecewise linear regions on the control surface, more MFs are required, as depicted in Fig. 6. The additional asymmetric MFs result in more piecewise linear regions, with additional break-points being created.

By reducing the control surface to a PWL function, the control block of a SIFLC can be represented as in Fig. 7. The simplicity of the structure allows for very rapid computation

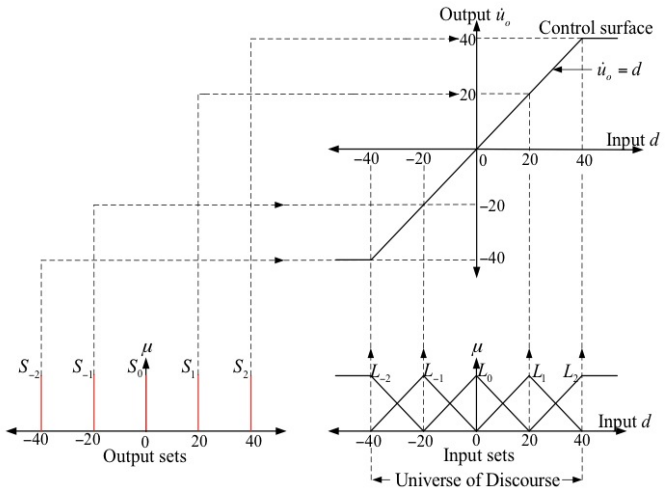


Fig. 4. PWL Control surface with symmetrical input and output membership functions.

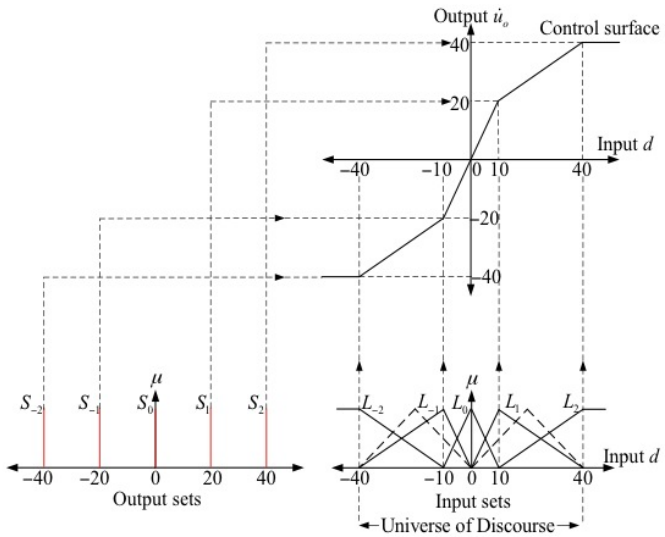


Fig. 5. PWL control surface with peak locations of the asymmetrical input MF.

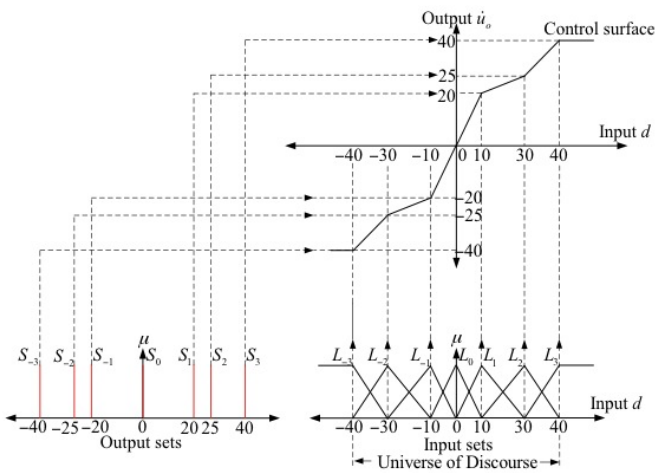


Fig. 6. PWL control surface with more piecewise linear regions using more input and output asymmetrical MFs.

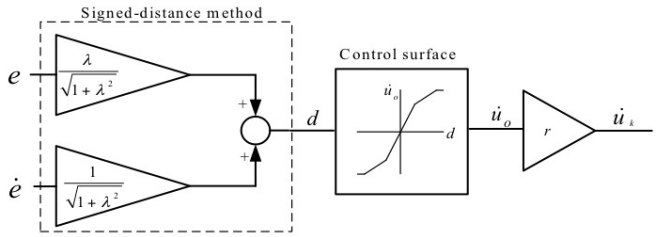


Fig. 7. SIFLC with PWL Control Surface.

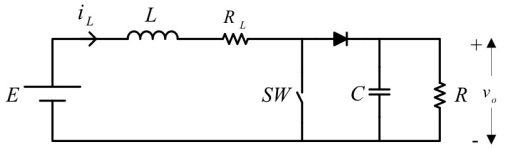


Fig. 8. Boost converter circuit.

because the fuzzification, rule inference and defuzzification processes are no longer required.

III. Boost DC-DC Converter

The circuit diagram of a boost converter is illustrated in Fig. 8. It has two states, i.e. when the SW is closed and opened. When the switch SW is in the "on" (closed) state, the current in the boost inductor (i_L) increases linearly and the diode is reverse biased. When SW is turned "off" (opened), the energy stored in the inductor is released through the diode to the output RC circuit. The converter is assumed to work in the continuous current mode where the inductor current is not allowed to reach zero.

To obtain an average model of the boost converter, i_L and the output voltage V_o are selected as state variables. If the SW is closed, the following expressions hold:

$$\frac{dv_o}{dt} = \frac{-v_o}{R \times C} \tag{3}$$

$$\frac{di_L}{dt} = \frac{E - i_L \times R_L}{L} \tag{4}$$

when SW is opened:

$$\frac{dv_o}{dt} = \frac{1}{C} \times \left(i_L - \frac{v_o}{R}\right) \tag{5}$$

$$\frac{di_L}{dt} = \frac{E - v_o - R_L \times i_L}{L}. \tag{6}$$

If the duty cycle is denoted by D and its period is T, the duration for the switch to be closed and opened are DT and $(1-D)T$, respectively. The average value of $\frac{dv_o}{dt}$ can be obtained by multiplying equations (3) and (5) with their respective closed and opened switch durations and then dividing the overall expression by T, i.e.:

$$\frac{dv_o}{dt} = \frac{D \times T \times \left(\frac{-v_o}{R \times C}\right) + (1-D) \times T \times \frac{1}{C} \times \left(i_L - \frac{v_o}{R}\right)}{T}. \tag{7}$$

Simplifying (7) yields:

$$\frac{dv_o}{dt} = (1-D) \times \frac{i_L}{C} - \frac{v_o}{R \times C}. \tag{8}$$

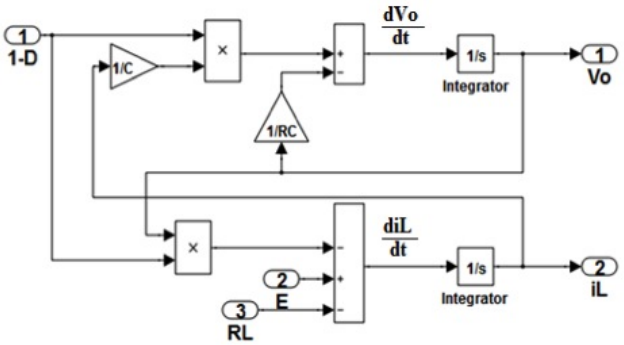


Fig. 9. Simulink model of boost converter.

Similar operations applied to $\frac{di_L}{dt}$ results in:

$$\frac{di_L}{dt} = \frac{E - R_L - v_o \times (1-D)}{L} \tag{9}$$

Eq. (8) and (9) complete the derivation of the average model of the boost converter. The implementation of the model in MATLAB/Simulink is shown in Fig. 9.

The average model is perturbed by a small signal perturbation around an operating point. For simplicity, the inductance winding resistance is neglected, i.e. $R_L = 0$. If $(\widetilde{d})$ is the perturbation in the duty cycle and $(\widetilde{v_o})$ is the resulting variation in the output voltage, the small signal model and transfer function of the converter can be obtained as [14]:

$$\frac{\widetilde{v_o}}{\widetilde{d}} = \frac{E}{(1-D)^2} \times \left(1 - \frac{L}{R} \times S\right) \times \frac{1}{L \times C \times \left(S^2 + \frac{S}{L \times C} + \frac{1}{L \times C}\right)} \tag{10}$$

The transfer function in (10) indicates the existence of a zero in the right-half plane. This zero affects the transient performance by limiting the control bandwidth, causing a slow transient response. The transfer function is also dependent on the steady state duty cycle value, i.e. D. Furthermore, it can be seen from the same equation that the zero and the poles values are load (R) dependent. As a result, different load value results in different poles and zero locations. Normally, the controller for a boost converter is designed based on a single (nominal) load value. Therefore, when a large load variation occurs (for example in a step load change), most model-based controllers are unable to satisfactorily cope with such changes. To minimize the effect of the load on the system, a load current sensing method has been proposed [15]. However, this solution requires an additional current sensor and a more complicated control algorithm.

IV. Equivalency of the between CFLC and SIFLC

A. Simulation Set-up

This simulation is dedicated to establish the equivalency of the CFLC and SIFLC, i.e. to show that the performances of both controllers are identical. Both symmetrical and asymmetrical cases will be investigated. The Simulink model of an averaged model boost converter with a CFLC is depicted in Fig.10. The values used for the boost converter are shown in Table III.

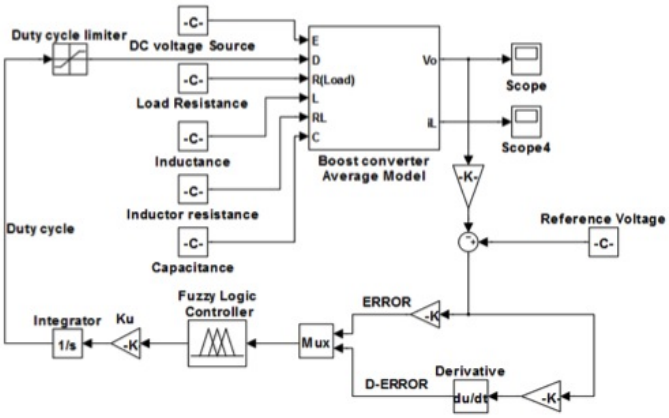


Fig. 10. Simulink simulation model for boost converter with CFLC.

TABLE III
VALUES AND PARAMETERS OF BOOST CONVERTER USED IN SIMULATION

Parameter/Component	Symbol	Value
Input Voltage	*vi*	10V
Output Voltage (nominal)	*vo*	20V
Nominal load	*R*	10 Ω
Switching frequency	*f*	100 KHz
Capacitor	*C*	100μF
Inductor	*L*	250μH
Inductor winding resistor	*RL*	0.1 Ω

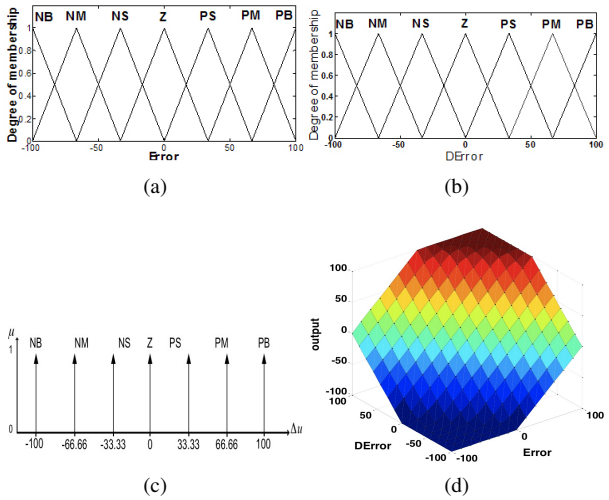
B. CFLC Simulation

Two inputs are applied to the CFLC, namely the error (Error) and the change of error (DError). The controlled parameter is the output voltage while the output of the controller is the change in D. Consequently, an integrator is introduced to generate D. Furthermore, a duty ratio limiter is required to limit $D < 0.8$. The purpose of this is to avoid converter instability [16]. The input and output of a CFLC with symmetrical MFs are illustrated in Fig. 11(a)-(c). It is a Sugeno-type with its input MFs equally spaced. The input MFs are 50% overlapping. To increase the computational speed, the singleton output MF is considered. The inference rules, shown in Table IV, are designed and optimized heuristically using the MATLAB Fuzzy Toolbox. The resulting three dimensional control surface is plotted in Fig. 11(d).

The CFLC in Fig. 11 has symmetrical distribution of its MFs. However, if the overlaps are made unequal, as illustrated in Fig. 12(a) and (b), a CFLC with asymmetric MFs will result. The output MF remains a singleton, which is similar to Fig. 11(c). The corresponding control surface of a CFLC with asymmetrical input MFs is depicted in Fig. 12(d).

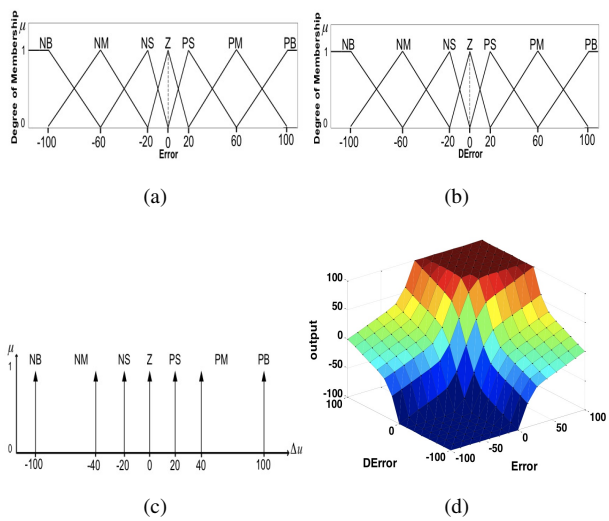
TABLE IV
RULE TABLE FOR SYMMETRICAL CFLC

ε \ e	PB	PM	PS	Z	NS	NM	NB
NB	0	-33	-66	-100	-100	-100	-100
NM	33	0	-33	-66	-100	-100	-100
NS	66	33	0	-33	-66	-100	-100
Z	100	66	33	0	-33	-66	-100
PS	100	100	66	33	0	-33	-66
PM	100	100	100	66	33	0	-33
PB	100	100	100	100	66	33	0



(a) (b) (c) (d)

Fig. 11. Symmetric CFLC. (a) Error MFs, (b) change of error MFs, (c) output MFs, (d) control surface for the given MFs.



(a) (b) (c) (d)

Fig. 12. Asymmetrical CLFC. (a) Error MFs. (b) Change of Error MFs. (c) Output MFs. (d) Control surface for the given MFs.

C. SIFLC Simulation

Fig. 13 shows a Simulink model of a boost converter with a SIFLC. The Fuzzy controller block is replaced by a simple PWL look up table. The SIFLC rule table in Table 4 corresponds directly to the CFLC with symmetrical MFs shown in Table 5. This is to ensure that fair comparisons can be made. The PWL control surface for this rule table is shown in Fig. 14(a). Note that this is the SIFLC with a symmetrical MF.

By manipulating the input MFs, i.e. by making them unequally spaced, the SIFLC with an asymmetrical MF is created, as shown in Fig 14(b). This control surface corresponds directly to the CFLC with asymmetrical MFs. It has three PWL sections with the highest slope for $0 < d < 10$. Then the slope is reduced after each subsequent breakpoint (BP1, BP2). Beyond UoD, i.e. $d > 100$, a saturation limit is imposed.

TABLE V
RULE TABLE FOR SYMMETRICAL SIFLC

Distance (d)	NB	NM	NS	Z	PS	PM	PB
Output, $\dot{u}_o$	-100	-66.67	-33.33	0	33.3	66.67	100

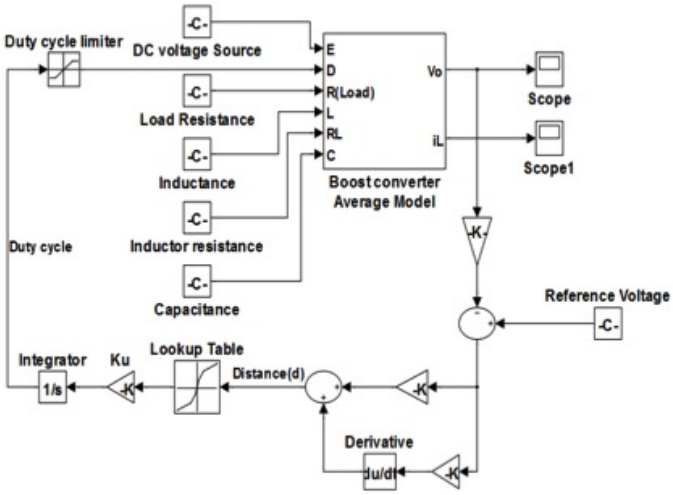
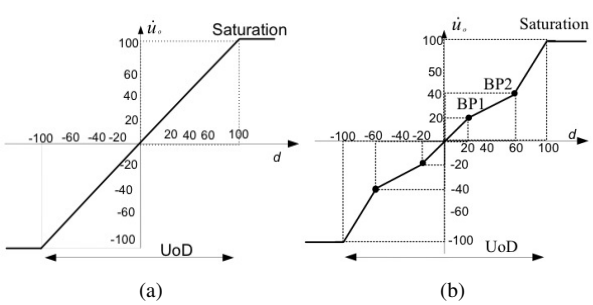


Fig. 13. Simulink simulation model for boost converter with SIFLC.

D. Verifying the Control Equivalency of the CFLC and SIFLC

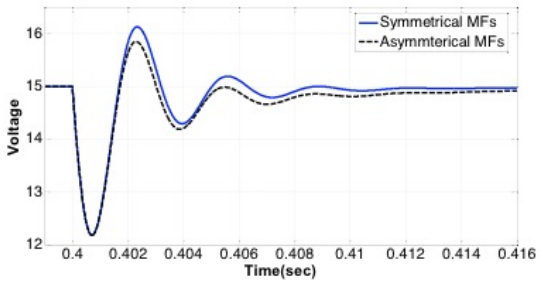
Next, simulations are carried out to show that the CFLC and SIFLC have identical control characteristics. Since the aim is to establish their equivalency, the designs need not to be optimized. Rather, the emphasis is to ensure that all of the parameters used in the CFLC and SIFLC match each other. These matching have been carried out in sections.

The controllers are evaluated using the most challenging disturbances, namely (a) a step change in the load and (b) a step change in the reference voltage. Fig. 15(a) and (b) show the responses of the CFLC and SIFLC for the step load changes, respectively. The load is stepped from 10 to 5 Ω at an output voltage of 15V. From the responses, it can be seen that, the performances of both controllers (for both asymmetrical and symmetrical MF cases) are hardly distinguishable. Fig. 15(c) depicts the absolute difference in voltage between the simulations using a CFLC and the SIFLC. The results indicate that the maximum discrepancy between the two approaches is 15mV, which is only 0.1% of the steady state voltage of 15V. Fig. 16(a) and (b) show the output voltage response of the converter when the input reference is stepped from 12.5 to 15V. The input voltage is fixed at 10V. From these two figures, it can be clearly seen that the control

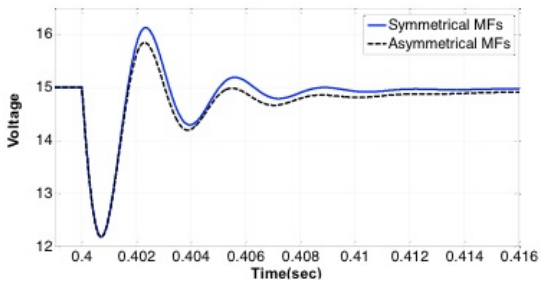


(a) (b)

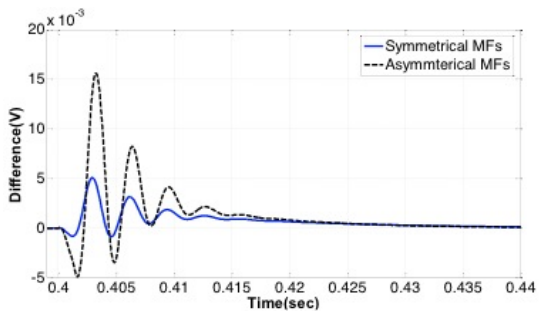
Fig. 14. PWL Control surface for SIFLC, (a) with symmetrical input MFs, (b) with asymmetrical input MFs.



(a)



(b)



(c)

Fig. 15. Voltage response for step change in load resistance from 10Ω to 5Ω when the input voltage $V_i = 10$V. (a) CFLC, (b) SIFLC, (c) voltage difference between SIFLC and CLFC.

response using a SIFLC is almost identical to that of a CFLC. Furthermore the maximum difference in voltage between the two methods, shown in Fig 16(c), is approximately 0.12%. From these observations, it can be concluded that even under very extreme disturbances, the SIFLC appears to be able to match the performance of a CFLC. These results suggest that a CFLC can be replaced with the SIFLC without a significant degradation in control ability.

E. Computational Time

Next, the execution times for the CFLC and SIFLC algorithms are compared. An appropriate benchmark is the total CPU run-time used by the Simulink program [17]. For each simulation run, the parameters and the Simulink simulation profiles for both controllers are kept equal. Ten sets of simulation are performed and the average execution times are shown in Fig. 17. For the CFLC with symmetrical MFs, the CPU run-time is 8.2 sec. In comparison, the SIFLC requires only 1.1sec, a reduction by a factor of eight. A similar trend is observed for the asymmetrical case. The run-times for the CFLC and SIFLC are 7.8 sec and 0.9 sec, respectively. These tests conclude that the SIFLC reduces the computation time by

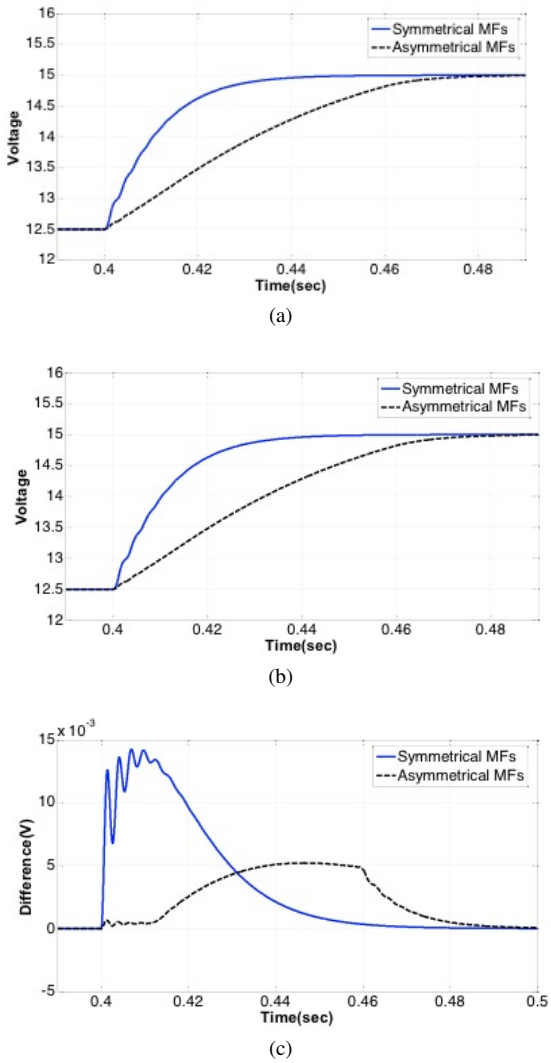


Fig. 16. Output voltage response for step change in reference voltage from 12.5 to 15V when input voltage $V_i = 10$V. (a) CFLC, (b) SIFLC, (c) absolute voltage difference between SIFLC and CLFC.

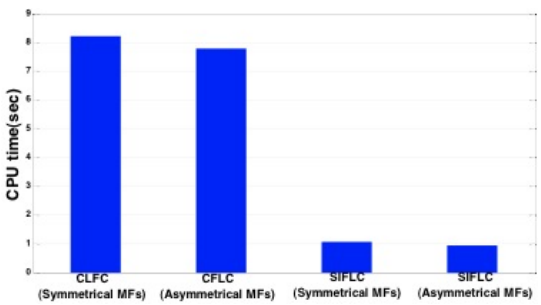


Fig. 17. CPU time consumed by CFLC and SIFLC.

order of magnitude with almost no difference in performance. This conclusion suggests that the SIFLC is preferable for hardware implementation because it can achieve a higher control bandwidth for a given switching frequency.

V. Experimental Results

A. Hardware Set-Up

In Section V, the equivalency of the CFLC and SIFLC has been demonstrated. Whilst the performances of both controllers are identical, the SIFLC has the advantages of a simpler and faster execution. On the other hand, the implementation of a CFLC is very complicated due the need to evaluate the rule table, as well as the fuzzification and deffuzzification processes. The task is more difficult when using a FPGA because it is less flexible when compared to other processors such as a DSP or a microcontroller. With these considerations, the SIFLC is only implemented in hardware. The boost converter specifications are as same as the simulation model specifications described in Section III. Both the symmetrical and asymmetrical MFs are implemented.

TABLE VI
EP2C35F672C6N FPGA RESOURCE UTILIZATION USING SIFLC

Elements	SIFLC usage	FPGA Capacity	% utilization
Logic Gates	408	33,216	1.2%
Total IO pins	4	475	1%
Total memory (Kbits)	213	484	44%

The SIFLC is realized using an Altera FPGA Educational board (DE2). The SIFLC is implemented in a single feedback loop structure, i.e. voltage control. In terms of functionality, the FPGA components can be divided into two types, namely sequential and combinational logics. The former comprises of analog to digital conversion (ADC), a differentiator and an integrator. These are time (clock) driven and are initiated when an enable signal is activated. The analog to digital conversion is implemented within the FPGA itself, i.e. without an external ADC chip. The remaining logics are combinational type, i.e. non-clock dependent. Timing-wise, they are always active. The control PWM pulse for the MOSFET is generated using a PWM block. It is based on a 200MHz clock, which means that the PWM pulse has a 5 ns resolution. Such a high resolution PWM is not achievable in a standard microprocessor or DSP. The main advantages of the high resolution PWM pulse is the reduced steady state error and the increased controller speed. The maximum frequency of the PWM pulse is 100 kHz.

Table VI shows the FPGA resource utilization using the proposed SIFLC scheme. The table indicates that the controller occupies a very small portion of the FPGA logic gates. Furthermore, the number of pins used is very few. These factors indicate that the SIFLC algorithm can be implemented on a much smaller and cheaper CPLD (*complex programmable logic device).*

B. Heuristic Tuning for the SIFLC PWL Control Surface

For the symmetrical SIFLC, the same PWL control surface used in the simulation, i.e. Fig. 14(a) is utilized. Note that a unity PWL slope is used throughout the UoD. This implies that no break point is introduced and therefore no tuning is required.

For the asymmetrical case, as a starting point, the same breakpoints that created the PWL functions in Fig 14(b) are utilized. However, to achieve optimum performance, the slopes of the PWL functions need to be tuned manually. The method of tuning is to adjust the slope of every section of the PWL function by means of setting the positions of the breakpoints. The objective is to achieve the best compromise in terms of the output voltage overshoot and the steady-state settling time.

In positioning the breakpoints, two main criteria are used: (1) a unity slope is considered between the origin and BP1 (2) a lower slope is set between BP1 and BP2 to slow down the effects of the step disturbance. Beyond BP2, the slope is automatically increased to reach the demanded saturation.

In contrast to the simulation, determining the optimum breakpoints in the hardware is not easy. The tuning needs to be done heuristically by trial and error.

C. Result: Comparison of Symmetrical and Asymmetrical MFs

Fig. 18 shows the response of the SIFILC when subjected to a step load change at an output voltage of 15V. The top oscillogram, i.e. Fig 18(a) depicts the symmetrical case while Fig 18(b) shows the asymmetrical case. The load was stepped from 10Ω to 5Ω, i.e. a 100% change. As can be clearly seen from these figures, the transient response of the asymmetrical case is significantly better than the symmetrical case. It has a lower overshoot and settles faster to the final steady-state value. The superiority of the asymmetrical case observed in the experiment appears to be consistent with simulation results. The apparently better hardware results can be attributed to the fact that during the experiment, the SIFLC parameters are tuned to achieve the best response. On the other hand, for the simulation shown in Section IV, the SIFLC design is not optimized.

Fig. 19 shows the response due to the input reference change. The input reference is periodically stepped from 12.5 to 15V and vice versa at 120 ms intervals. The load is fixed at 10Ω and the input is maintained at 10V. As can be seen from the expanded waveform of the output voltage (the bottom-most trace) the symmetrical case exhibits a faster response. When the input reference is stepped, it took 0.75 ms to stabilize to a new value. In contrast, the asymmetrical case requires approximately 2.5 ms. Again, this observation is consistent with the simulation shown in Section IV.

VI. Conclusion

In this paper, a SIFLC has been proposed to regulate boost converter output voltage. Simulation results of both the conventional FLC and the SIFLC show identical responses for the same disturbances. This equivalency suggests that the SIFLC can be utilized to replace a CFLC without a significant degradation in controller's performance. Furthermore, due to its much simpler structure, the SIFLC only requires about one tenth of the CPU execution time. To prove its effectiveness, the SIFLC is applied to control a 50W boost converter. The algorithm is implemented using an Altera FPGA. It was found that, in general, the SIFLC exhibits excellent responses to load and input reference changes.

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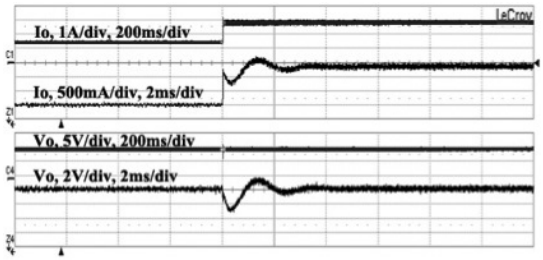
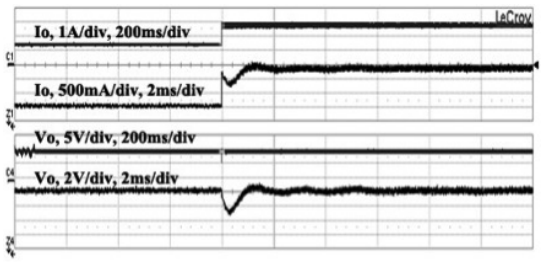
This work was supported by the Universiti Teknologi Malaysia under New Academic Staff (NAS) Fund (Vot. No. 77955).

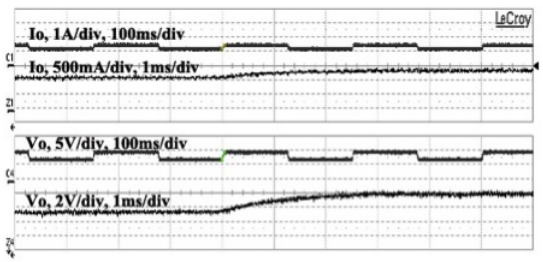


(a)

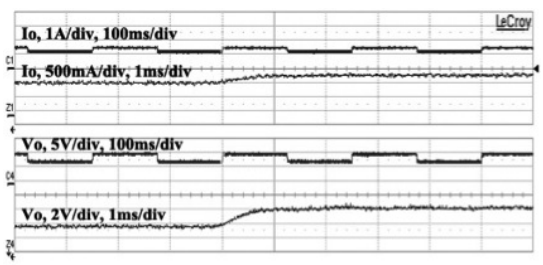


(b)

Fig. 18. Boost converter response using SIFLC in Vo=15v and load disturbance from 5Ω to 10Ω. (a) Using symmetrical MFs, (b) using asymmetrical MFs.



(a)



(b)

Fig. 19. Boost converter output voltage using SIFLC in 10Ω load and reference change from 12.5V to 15V. (a) Using asymmetrical MFs, (b) using symmetrical MFs.

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