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Impact of Device Parameter Variation on the Electrical Characteristic of N-type Junctionless Nanowire Transistor with High-k Dielectrics

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ABSTRACT

Metallurgical junction and thermal budget are serious constraints in scaling and performance of conventional metal-oxide-semiconductor field-effect transistor (MOSFET). To overcome this problem, junctionless nanowire field-effect transistor (JLNWFET) was introduced. In this paper, we investigate the impact of device parameter variation on the performance of n-type JLNWFET with high-k dielectrics. The electrical characteristic of JLNWFET and the inversion-mode transistor of different gate length (L_G) and nanowire diameter (d_{NW}) was compared and analyzed. Different high-k dielectrics were used to get an optimum device structure of JLNWFET. The device was simulated using SDE Tool of Sentaurus TCAD and the I-V characteristics were simulated using Sdevice Tools. Lombardi mobility model and Philips unified mobility model were applied to define its electric field and doping dependent mobility degradation. A thin-film heavily doped silicon nanowire with a gate electrode that controls the flow of current between the source and drain was used. The proposed JLNWFET exhibits high ON-state current (I_{ON}) due to the high doping concentration (N_D) of 1 x 10^{19} cm^{-3} which leads to the improved ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) of about 10% than the inversion-mode device for a L_G of 7 nm and the silicon d_{NW} of 6 nm. Electrical characteristics such are drain induced barrier lowering (DIBL) and subthreshold slope (SS) were extracted which leads to low leakage current as well as a high I_{ON}/I_{OFF} ratio. The performance was improved by introducing silicon dioxide (SiO_2) with high-k dielectric materials, hafnium oxide (HfO_2) and silicon nitrate (Si_3N_4). It was found that JLNWFET with HfO_2 exhibits better electrical characteristics and performance.

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1. INTRODUCTION

To speed up the performance of the microprocessor, the number of transistors must be double in every 18 months. To double the number of transistors means to reduce the size of transistor. As what being predicted by Moore's law, process technology tends to be scaled down continuously [1]. The scaling process allowed more transistors to be packed in a smaller chip area and hence enhance the functionality of silicon on chips (SoCs). MOSFET typically used in industries due to its small size, and can be fabricated in a single integrated circuit with millions of numbers. However, the scaling of conventional planar transistor has reached its limit which lead to increase in short channel effects (SCEs) and sensitivity to process variation [2]. SCEs are the main limitations in the scaling of MOSFET below 10nm [3]. SCEs comprises of Drain Induced Barrier

Lowering (DIBL), subthreshold slope (SS), limitation imposed on electron drift characteristics in the channel, increase in threshold voltage variation, reduction in I_{ON}/I_{OFF} ratio and increase of leakage current causing the scaling of conventional CMOS transistors in sub 10nm technologies almost impossible. This is due to the fact that reduction in I_{ON}/I_{OFF} ratio leads to device instability and hence limits subthreshold circuit design. Furthermore, increment in leakage current leads to the static power consumption increment[2].

In PN Junction transistor, the junction is formed when a piece of P-type silicon material and N-type piece of silicon are in contact. The majority carriers in N-type material are electrons, while holes are the majority carriers in P-type semiconductor. Some junction formed by two different semiconductors e.g. Schottky diode, heterojunction etc. Bipolar junction transistor contains two p-n junctions, JFET (junction field-effect transistor) has only one p–n junction and MOSFET contains a Schottky junction [4]. Junctionless transistor (JLFET) was introduced to replace the traditional junction transistor because of the challenges in scaling and complex thermal budget of the device [5]. Junctionless transistors can be described as variable resistors controlled by a gate electrode. JLNWFET is a very thin heavily doped semiconductor nanowire that has gate electrode that control the flow of current from source to drain [6]. The gate oxide thickness has gradually decreased so as to increase the gate capacitance as well as to drive the current to increase the device performance [7].Nanowire transistor has a uniform heavily doping concentration from source to drain. The channel also has the same doping concentration that can be fully depleted to turn the device off.High doping concentration and ultra-shallow junction are the main obstacles in improving scaling in MOSFETs [8]. Short channel effects such as Drain Induced Barrier Lowering (DIBL), subthreshold Swing (SS) and so on reduces the performance of the device [9]. Junctionless transistors, also known as gated resistor, have no junctions hence, no doping concentration gradients, simpler fabrication process, diminished DIBL and SS, and better electrical properties. Short channel effects are significantly reduced in Junctionless transistor [10]. The properties of the material of the gate and channel wires in conjunction with the nanoscale geometries in metal-gated junctionless FET (MJLFET) allows FET-like switching characteristics without the need for engineered source and drain junctions or lateral doping abruptness [11].

Previous work shows that Many researchers have contributed tremendously in identifying the challenges in scaling of conventional MOSFET. Junctionless FETs were proposed in order to overcome short channel and scaling challenges [12]. JLT exhibits excellent I_{ON}-I_{OFF} ratio, improved the scaling to the sub region, decreasing the short channel effects (SCE) and better electrical properties. SCEs can be mitigated by reducing the electrostatic integrity factor which depends on the geometry of the device and it is a measure of the way the electric field lines from drain influence the channel region thus causing the SCEs [13]. Low-sidewalls can improve the SCEs of the device significantly by reducing the fringing-induced barrier lowering for thick-gate insulators [14].

Multigate junctionless transistor (MuGJLT) was compared with MOSFET for a gate length of 10 – 30 nm has been conducted by Chi-Woo Lee et al.[9]. The electrical characteristics such as the DIBL, SS and threshold voltage (V_{TH}) of both MuGJLT and MOSFET were evaluated and analyzed. In this study, DIBL and SS of MuGJLT were significantly improving better than the conventional MOSFET for different L_G. The SS of the device with L_G 5nm is below 80mV/decade which is better than that of the MOSFET. This shows the potential of JLT for extremely short-channel applications. The I_{OFF} is determined entirely by the electrostatic control of the gate not by the leakage current of a reverse-biased diode. The drain current was high due to the high doping concentration of 8×10^{19} cm^{-3} and the cross-sectional area of the silicon wire is too small compare to the IM which used lightly doped channel in order to avoid pre-matured inversion at the corners [9].The electrical properties of junctionless nanowire transistor (JNT), inversion-mode transistor and accumulation-mode MOS devices for gate length 5nm were compared by J.P. Colinge et al.[15]. The variation of threshold voltage with physical parameters and intrinsic device performed was analyzed.

The drain current I_{DS} was significantly increased even for a gate length of 10 nm, but the leakage current is also high for V_{GS} = 0 V. This shows the leakage current is high in nanowire junctionless transistor having thickness oxide, t_{ox} of 2 nm. DIBL and SS were high for short L_G, but significant improved when the effective length, L_{eff} was high i.e. when L_G is 15 nm achieves a degraded SS of 78 mV/dec and DIBL of 95 mV/V [15]. The electrical characteristics of Nanowire JLFET and core shell JLFET were compared in [16]. I_{OFF} was improved by more than one order of magnitude when a high-k dielectric is used as a spacer in double gate junctionless transistor [17]. The leakage current has reduced due to parasitic bipolar junction transistor (BJT) action in the NWJLFET [18]. Core shell JLFET with the higher doping concentration has the lower leakage current is and therefore, exhibit higher I_{ON}/I_{OFF} ratio. Although a core doping of 1×10^{19} cm^{-3} depletes the shell region at core shell interface, but the depletion is not sufficient to volume depletion. Electron channel still exists in the channel region. Highly doped p+ core of 1×10^{20} cm^{-3} should be use in order to achieve total volume depletion [16]. The I_{OFF} may be increases when the channel length in the NWJLFET due to the improved gain of the parasitic bipolar junction transistor (BJT) when the base width reduced [19, 20]. The parasitic BJT action causes the I_{OFF} to increased, hence I_{ON}/I_{OFF} ratio decreases [21].

In this paper, JLNWFET device and the inversion mode FETs of the same device parameters was designed and their performances were compared and analyzed. JLNWFET device of different dielectric materials (low-k and high-k) was also designed and their electrical characteristics were compared and analyzed. The electrical properties such as threshold voltage (V_{th}), on-off current ratio (I_{ON}/I_{OFF}), subthreshold swing (SS), and drain induced barrier lowering (DIBL) were extracted from the I-V curves. Finally, their overall electrical characteristics were compared and validated with the literature review.

2. RESEARCH METHOD

The simulation was carried out using Sentaurus TCAD software. The device structure was simulated by using SDE Tool and I-V curve was extracted by using Sdevice Tool. Lombardi mobility model and Philips unified mobility model were embedded to consider field- and doping-dependent mobility degradation. Shockley–Read–Hall (SRH) is the dominant generation and recombination process in silicon and other indirect energy band gap materials. It can also dominate in direct band gap materials under conditions of very low carrier densities or very low level injection. Auger recombination model and Fermi–Dirac statistics were also used. The L_G of the devices was varied between 7 – 120nm and d_{NW} was varied from 6 – 10 nm were designed and simulated. SiO_2 and high-k dielectric materials such as HfO_2 and Si_3N_4 devices of different L_G and d_{NW} were also designed and simulated to obtained electrical characteristics. High-k dielectric was used in the JLNWFET device structure to optimize the electrical characteristics and reduce the SCEs. The electrical characteristics such as V_{TH}, ON-state current, OFF-state current, DIBL, SS and the ON-state to OFF-state current ratio of the devices were analyzed. The parameters and dimension of the device are shown in Table 1 for both the JLNWFET and Inversion-Mode device. The table shows the dimensions of the parameters used in designing the two devices of different L_G and d_{NW}. The device parameters of JLNWFET is the same with that of [22] for further validation. Both devices JLNWFET and Inversion-Mode NWFET are fixed to have same device parameters.

Table 1. JLNWFET and Inversion-mode device parameters

Parameter	JLNWFET	Inversion-mode
Structure	n-type cylinderical	n-type cylindrical
S/D doping	$10^{19}cm^{-3}$	$10^{17}cm^{-3}$
Channel doping	$10^{19}cm^{-3}$	$2 \times 10^{20}cm^{-3}$
Nanowire diameter (d_{NW})	6-10nm	6-10nm
Oxide thickness (t_{ox})	1nm	1nm
Oxide material used	SiO_2, HfO_2, Si_3N_4	SiO_2
Gate workfunction (ϕ_m)	4.8eV	4.8eV
Gate length (L_G)	7-120nm	7-120nm
Length of S/D (LSD)	10nm	10nm
Length of S/D contact (LSDC)	10nm	10nm

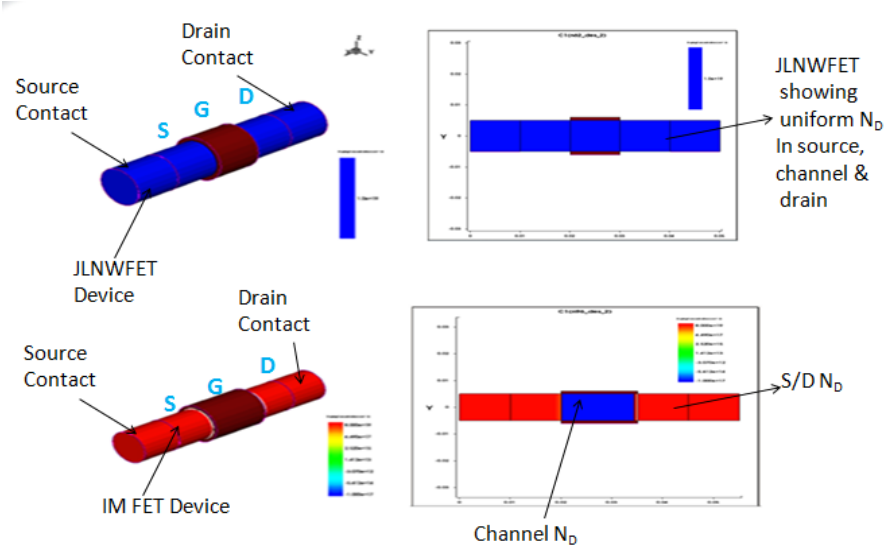

Figure 1. 3D and horizontal cross-sectional view of JLNWFET (top) and Inversion-mode (bottom) devices

The 3D and horizontal cross-sectional diagram of JLNWFET and the inversion-mode device was shown in Figure 1. It shows that JLNWFET has uniform N_D from source to drain while the inversion-mode device, channel doping is different to the doping in the source and drain junctions.

3. RESULTS AND DISCUSSION

The result of the research was obtained and dicussed in three forms:

3.1. Impact of variation of L_G on electrical characteristics of JLNWFET and Inversion mode FET

JLNWFET and the inversion-mode devices were simulated at both linear and saturation regions which are V_{DS} of 0.05 V and 1 V respectively. The N^+ region is heavily doped with concentration of 1 x 10^{19} cm^{-3} in order to get high ON-state current to flow between the source and the drain. A small cross section of the channel was used to ensure full depletion of the heavily doped channel resulting in low leakage current as shown in Figure 2. However, when Lg decreases, the leakage current increases. This is due to the short channel effects. Figure 2 shows the I-V curve of JLNWFET of for different L_G. It was found that the device with L_G = 120 nm has minimum I_{OFF} while the device with smaller gate length, L_G = 7 nm has higher I_{OFF}. This prove that as the I_{OFF} decreases with an increase of L_G. Figure 2 shows that JLNWFET with L_G = 7 nm has lower V_{TH} while device with L_G = 120 nm has higher V_{TH}. This shows that as the L_G increases, the V_{TH} also increases and vice versa.

Figure 3 shows theSubthreshold slope and DIBL with L_G variation for both devices. Subthreshold slope and DIBL in JLNWFET shows great improvement than the inversion-mode device as shown in Figure 3. Both the SS and DIBL were limited to 69.98 mV/dec and 54.73 mV/V respectively for L_G of 7 nm, compared to the inversion-mode device which has 90.13 mV/dec and 112.15 mV/V respectively for the same L_G. However, as the gate length LG increases with constant dNW, the SS and DIBL reduced to the minimum level. For L_G of 120 nm, the SS and DIBL of JLNWFET device are 47.77 mV/dec and 69.98 mV/V respectively. Our aim is not only to minimize SCEs but also to improve the scaling in order to obtain the most optimum device structures with optimized electrical characteristics.

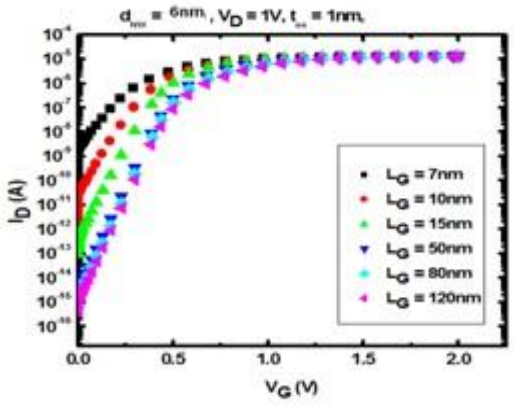

Figure 2. I-V characteristics of JLNWFET for different L_G for V_D= 1 V (in log scale)

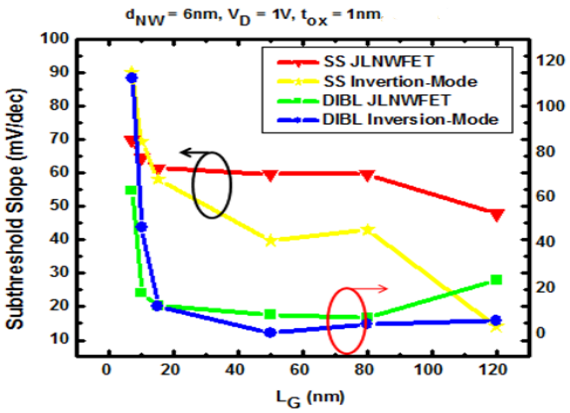

Figure 3. SS and DIBL of JLNWFET and inversion-mode devices for different L_G for V_D= 1 V

High doping concentration, N_D and small nanowire cross sectional area increases the ON-state current in nanowire junctionless transistor [23]. Metal gate work function and small cross-section area of the nanowire are to ensure full depletion of the heavily doped channel resulting in low leakage current [24]. Figure 4 shows JLNWFET and the Inversion-mode FET demonstrates almost equal ON-state current. For device with L_G of 7 nm, JLNWFET and the inversion-mode FET have I_{ON} of 3.77 x 10^{-6} A and 1.23 x 10^{-5} A respectively. However, as the L_G increases the I_{ON} decreases. The OFF-state shows significant improvement in JLNWFET over the inversion-mode for gate length less or equal to 10nm. For L_G of 7 nm, I_{OFF} is 8.68 x 10^{-14} A and 2.50 x 10^{-12} A for NW JLFET and inversion-mode device respectively. As the L_G increases, the I_{OFF} of both devices improves further. JLNWFET has better I_{ON}/I_{OFF} ratio for L_G below 10 nm. For L_G of 7 nm, JLNWFET and inversion-mode have I_{ON}/I_{OFF} ratio of 4.34 x $10^7$and 4.92 x 10^6.

The results obtained were tabulated and compared as in the Table 2 for both JLNWFET and the inversion-mode devices.

Table 2. Electrical propoerties of JLNWFET and Inversion-Mode for different L_G with constant d_{NW} of 6nm for $V_D = V_G = 1$ V

DEVICE	L_G (NM)	V_{TH} (V)	SS (MV/DEC)	DIBL (MV/V)	I_{ON} (A)	I_{OFF} (A)	I_{ON} / I_{OFF}
JLNWFET	7	0.454	69.98	54.73	3.77×10^{-6}	8.68×10^{-14}	4.34×10^{7}
	10	0.503	64.71	24.10	3.70×10^{-6}	3.98×10^{-15}	9.29×10^{8}
	15	0.530	61.39	20.21	3.62×10^{-6}	3.75×10^{-16}	9.65×10^{9}
	50	0.584	59.53	17.58	3.11×10^{-6}	2.94×10^{-17}	1.06×10^{11}
	80	0.606	59.64	16.84	2.75×10^{-6}	1.75×10^{-17}	1.57×10^{11}
	120	0.622	47.77	27.89	2.34×10^{-6}	1.11×10^{-17}	2.11×10^{11}
INVERSION-MODE	7	0.443	90.13	112.95	1.23×10^{-5}	2.50×10^{-12}	4.29×10^{6}
	10	0.554	69.29	47.26	1.07×10^{-5}	2.39×10^{-15}	4.48×10^{6}
	15	0.604	58.15	12.42	1.02×10^{-5}	3.94×10^{-17}	2.59×10^{11}
	50	0.648	39.71	8.29	7.50×10^{-6}	4.87×10^{-18}	1.54×10^{12}
	80	0.656	42.97	4.32	6.21×10^{-6}	2.79×10^{-18}	2.23×10^{12}
	120	0.666	14.06	5.89	5.12×10^{-6}	2.59×10^{-18}	1.98×10^{12}

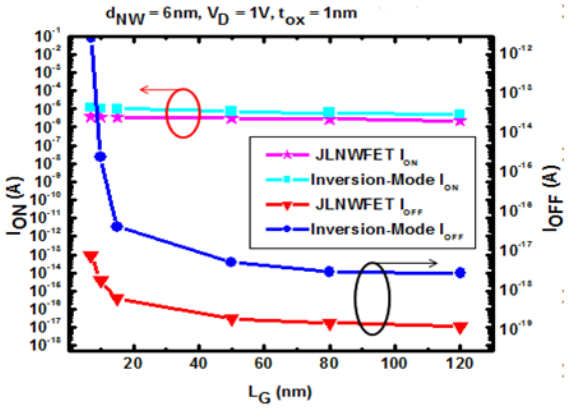

Figure 4. I_{ON} and I_{OFF} of JLNWFET and inversion-mode device for different L_G for $V_D = 1$ V

3.2. Impact of variation of d_{NW} on electrical characteristics of JLNWFET and Inversion mode FET

JLNWFET and the inversion-mode devices were simulated using different d_{NW} of 6, 8, and 10 nm using a constant L_G of V_D of 1 V. For d_{NW} of 6 nm, JLNWFET and inversion-mode has V_{TH} of 0.454 V and 0.443 V respectively. However, as the diameter increases, the threshold voltage decreases for both the two devices because, the V_{TH} depends on the doping concentration, gate oxide thickness, nanowire width and silicon thickness film [25]. The DIBL and the SS shows significant improvement in JLNWFET than in the inversion-mode device as shown in Figure 5. For d_{NW} of 6 nm, the SS and DIBL of JLNWFET and inversion mode are 69.98 mV/dec and 54.74 mV/V respectively as against the inversion-mode FET of 90.13 mV/dec and 112.15 mV/V respectively. Nevertheless, as the d_{NW} increases both the SS and DIBL increases further

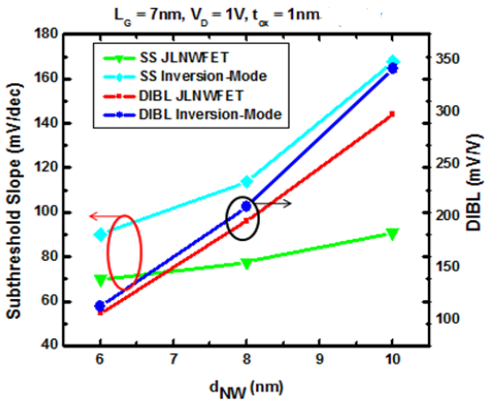

Figure 5. DIBL and SS of JLNWFET and inversion-mode device for different d_{NW} for V_D of 1 V.

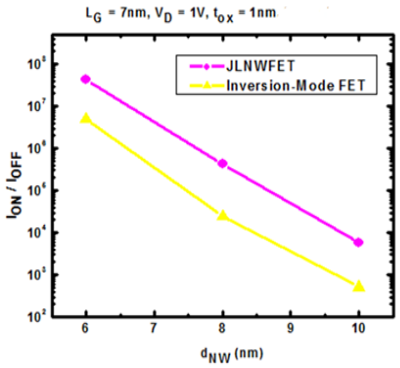

Figure 6. I_{ON}/ I_{OFF} of NW JLFET and inversion-mode device for different d_{NW} for V_D of 1 V

Small d_{NW} and high doping and concentration reduce the series resistance for the flow of current in nanowire, hence increasing the ON-state current of the junctioless transistor [16]. Metal gate material was used in order to reduce the gate resistance. Small cross section of the channel allows the gate to deplete the heavily doped channel entirely and obtain a very low leakage current (I_{OFF}) [9].Figure 6 shows the JLNWFET exhibits higher ON-state to OFF-state current ratio than the inversion-mode device. For d_{NW} of 6nm, I_{ON}/I_{OFF} of JLNWFET and inversion-mode were found to be 4.34 x 10^7 and 4.92 x 10^6 respectively. Nevertheless, as the d_{NW} increases the I_{ON}/I_{OFF} of both the two devices decreases. This proves that, high doping concentration and small cross-sectional area of nanowire improve the performance of the device. The results of the variation of nanowire diameter (d_{NW}) for L_G of 7 nm of both JLNWFET and the inversion-mode devices were obtained and tabulated in Table 3.

Table 3. Electrical Characteristics of JLNWFET and Inversion-Mode for constant L_G of 7 nm with different d_{NW} for $V_D = V_G = 1$ V

DEVICE	D_{NW} (nm)	V_{TH} (V)	SS (mV/dec)	DIBL (mV/V)	I_{ON} (A)	I_{OFF} (A)	I_{ON} / I_{OFF}
JLNWFET	6	0.454	69.98	54.73	3.77 x 10^{-6}	8.68 x 10^{-14}	4.34 x 10^7
	8	0.320	77.59	96.11	6.64 x 10^{-6}	1.56 x 10^{-11}	4.26 x 10^5
	10	0.168	90.91	143.89	1.03 x 10^{-5}	1.84 x 10^{-9}	5.60 x 10^3
INVERSION-MODE	6	0.443	90.13	112.95	1.23 x 10^{-5}	2.50 x 10^{-12}	4.29 x 10^6
	8	0.269	113.75	209.16	1.90 x 10^{-5}	7.84 x 10^{-10}	2.44 x 10^4
	10	0.046	167.50	341.89	2.73 x 10^{-5}	5.32 x 10^{-8}	5.12 x 10^2

3.3. Effects of different dielectric materials of the electrical characteristic of JLNWFET

`To optimize the device, JLNWFETs was designed and simulated with different dielectric materials; HfO_2, Si_3N_4 and SiO2 of different L_G as in [26]. The remaining parameters and dimensions are the same as in Table 1. The electrical characteristics of the devices was obtained using Sdevice of Sentaurus TCAD, analyzed and compared.

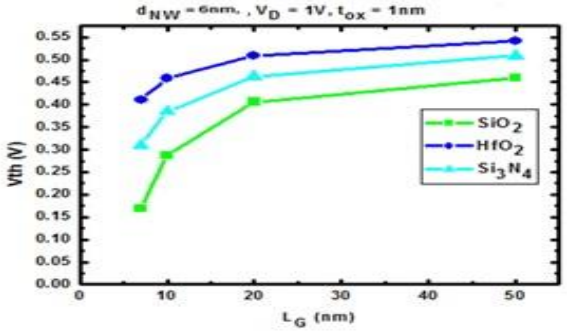

Figure 7. V_{TH} of JLNWFETs for different dielectric materials for V_D of 1 V

Figure 7shows the V_{TH} of the JLNWFET of the three different oxide materials for different L_G was shown. It was found out that SiO_2 demonstrates lower V_{TH} of all L_G. For L_G of 7 nm, threshold voltage of the JLNWFET with SiO_2, HfO_2 and Si_3N_4 are 0.169 V compared to 0.410 V and 0.310 V of respectively. As the L_G increases V_{TH} also increases in all the three devices as shown.

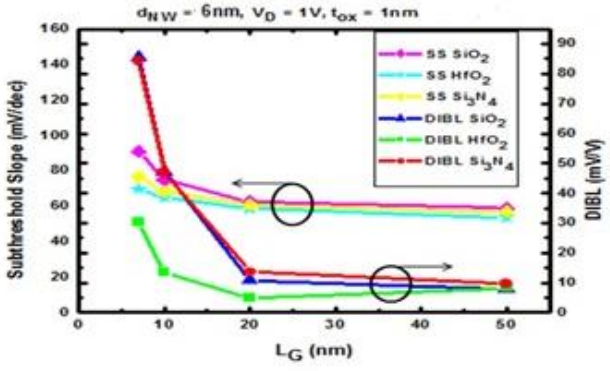

Figure 8. Effect of different dielectric materials on SS and DIBL of JLNWFET for different L_G

Junctionless transistors are expected to have a very low DIBL and SS effects due to the absent of junction. When L_G is small, high-*k* dielectrics can help to minimize this DIBL effect very effectively. The theoretical limit of SS is 60 mV/decade [26]. In Figure 8, it was found out that HfO_2 exhibits better SS and DIBL among the three gate oxides. For L_G of 10nm, the SS and DIBL of HfO_2, SiO_2 and Si_3N_4 are 64.70 mV/dec and 22.74 mV/V, 74.92 mV/dec and 79.68 mV/V and 68.49 mV/dec and 46.95 mV/V respectively. JLNWFET demonstrates lower I_{OFF} when the L_G is large. For L_G of 50 nm, the I_{OFF} of SiO_2, HfO_2 and Si_3N_4 are 3.81 x 10^{-15} A, 1.14 x 10^{-16} A and 4.92 x 10^{-16} A respectively. For device with L_G 7 nm, the OFF-state currents are high i.e. 1.84 x 10^{-9} A, 2.66 x 10^{-13} A and 1.76 x 10^{-11} A for SiO_2, HfO_2 and Si_3N_4 respectively. HfO_2 reveals better OFF-state current than the other two dielectric materials.

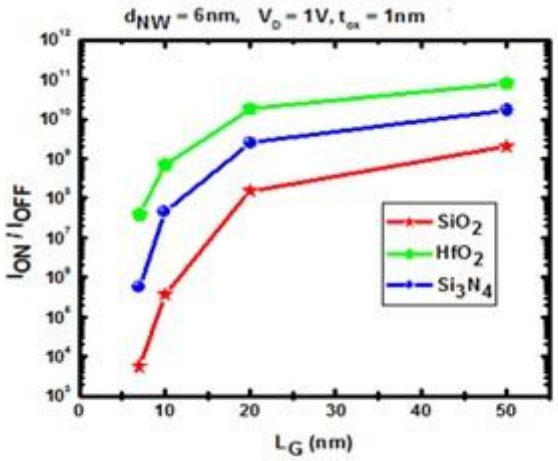

Figure 9. Effect of different dielectric materials on I_{ON}/I_{OFF} of JLNWFET of different L_G for V_D of 1 V

Due to the higher I_{ON} and lower I_{OFF}, HfO_2 exhibits higher ON-state to OFF-state current ratio as shown in Figure 9. For devices with L_G 10 nm, I_{ON}/I_{OFF} of SiO_2, HfO_2 and Si_3N_4 was found to be 3.70 x 105, 6.96 x 108 and 4.43 x 107 respectively. The I_{ON}/I_{OFF} increases when the gate length increases. The I_{ON}/I_{OFF} of SiO_2, HfO_2 and Si_3N_4 when L_G is 50 nm are 2.04 x 109, 7.88 x 1010 and 1.68 x 1010 respectively. The results obtained were tabulated and compared in the Table 4 for the devices with three different dielectric materials.

Table 4. Electrical Characteristics of JLNWFET for constant d_{NW} of 6nm with different L_G for V_D of 1 V

DEVICE	GATE OXIDE	L_G (nm)	V_{TH} (V)	SS (mV/dec)	DIBL (mV/V)	I_{ON} (A)	I_{OFF} (A)	I_{ON} / I_{OFF}
JLNWFET	SiO_2	7	0.169	90.91	143.89	1.03 x 10^{-5}	1.84 x 10^{-9}	5.60 x 10^{3}
		10	0.287	74.92	79.68	1.00 x 10^{-5}	2.70 x 10^{-11}	3.70 x 10^{5}
		20	0.320	62.45	18.21	9.38 x 10^{-6}	6.09 x 10^{-14}	1.54 x 10^{8}
		50	0.168	58.95	13.16	7.74 x 10^{-6}	3.81 x 10^{-15}	2.04 x 10^{9}
	HfO_2	7	0.410	69.67	51.16	1.04 x 10^{-5}	2.66 x 10^{-13}	3.91 x 10^{7}
		10	0.459	64.70	22.74	1.03 x 10^{-5}	1.48 x 10^{-14}	6.96 x 10^{8}
		20	0.508	58.76	8.21	9.89 x 10^{-6}	5.49 x 10^{-16}	1.80 x 10^{10}
		50	0.542	53.72	13.79	8.98 x 10^{-6}	1.14 x 10^{-16}	7.88 x 10^{10}
	Si_3N_4	7	0.310	76.71	84.32	1.03 x 10^{-5}	1.76 x 10^{-11}	5.85 x 10^{5}
		10	0.385	68.49	46.95	1.01 x 10^{-5}	2.28 x 10^{-13}	4.43 x 10^{7}
		20	0.463	60.69	13.58	9.59 x 10^{-6}	3.86 x 10^{-15}	2.48 x 10^{9}
		50	0.509	56.89	9.58	8.29 x 10^{-6}	4.92 x 10^{-16}	1.68 x 10^{10}

Table 5. Performance validation of proposed work and other works

Electrical Properties	L_G = 7 nm		L_G = 20 nm		
	[27]	**This Work**	**[27]**	**[27]**	**This Work**
SS (mV/dec)	68.5	54.73	61.68	110	62.45
DIBL (mV/V)	17.3	69.98	30	140	18.21
I_{ON}(A)	N/A	N/A	7 x 10^{-6}	N/A	9.38 x 10^{-6}
I_{ON}/I_{OFF}	10^6	10^7	10^7	10^5	10^8

The highlighted result (in red box) in Table 4 shows the electrical characteristics of HfO_2. It was found out that HfO_2 exhibits significant characteristics than SiO_2 and Si_3N_4. It can be observed that for L_G of 7 nm, HfO_2 has achieved I_{ON}/I_{OFF} of 10^7 compared to SiO_2 and Si_3N_4 of 10^3 and 10^5 respectively. SS and DIBL were highly improved to 64.70 mV/dec. and 22.74 mV/V respectively for L_G of 7nm in HfO_2 than the other two materials. This shows that the proposed JLNWFET with HfO_2 is the optimum alternative to improve the scaling and the performance of the device as well as to suppress the SCEs.The electrical properties of this proposed work was compared with the other works in [4, 8, 11] for L_G of 7 nm and 20 nm as in Table 5. For the case of 7nm gate length, it was observed that SS of this proposed work is improved by 20% with 54.7 mV/dec as compared to 68.5 mV/dec. I_{ON}/I_{OFF} is also improved by tenfold as compared to [4]. For the case of 20 nm gate length, it was observed that but the DIBL is greatly improved by about 39% with 18.21 mV/V as compared to [8] which is 30 mV/V. Moreover, for the case of 20 nm gate length, it was observed that SS, DIBL and I_{ON}/I_{OFF} are greatly improved if compared to [11].

4. CONCLUSION

JLNWFET and inversion-mode devices have been successfully designed for different gate lengths and nanowire diameters. The electrical characteristics of the two devices was compared and analyzed. The electrical characteristics and performance of JLNWFET of three different dielectric materials (low-k and high-k) have been investigated, compared and analyzed. This work discovered that JLNWFET exhibits significant improvement in electrical characteristics than the inversion-mode device especially for gate length less or equal to 10 nm. SCEs such as DIBL and SS are considerably reduced in JLNWFET devices. Although, the JLNWFET with long L_G demonstrated higher I_{ON}/I_{OFF} and the most optimum SCEs. Our aim is not only to improve performance and SCEs, but also to get the most optimum device's physical parameter. For the same L_G and d_{NW}, JLNWFET proved to have better electrical characteristics than the inversion-mode device. JLNWFET with HfO_2dielectric demonstrated better SCEs and excellent electrical characteristics than JLNWFET with Si_3N_4 and SiO_2 dielectrics for L_G shorter than 35 nm. JLNWFET with Si_3N_4 exhibits better electrical characteristics and SCEs than HfO_2 and SiO_2 for gate length longer than 35 nm. To achieve better performance, JLNWFET of L_G 10 nm or below is highly recommended. Heavily doped concentration and small nanowire diameter (d_{NW}) of 10 nm or below produced higher ON-state current. Metal gate material was used to reduce gate resistance. To achieve volume depletion, the cross-sectional area of the channel must be small enough in order to deplete the highly doped channel entirely. In both the JLNWFET and the inversion-mode devices, as the ON-state current increases, the OFF-state current also increases which leads to small improvement in the I_{ON}/I_{OFF} ratio.

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