Analysis and Design of a Bidirectional Cycloconverter-Type High Frequency Link Inverter with Natural Commutated Phase Angle Control

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Abstract

In this paper a cycloconverter-type high frequency transformer link inverter with a reduced switch count is analyzed and designed. The proposed topology consists of an H-bridge inverter at the transformer's primary side and a cycloconverter with three bidirectional switches at the secondary. All of the switches of the cycloconverter operate in non-resonant zero voltage and zero current switching modes. To overcome a high voltage surge problem resulting from the transformer leakage inductance, phase angle control based on natural commutation is employed. The effectiveness of the proposed inverter is verified by constructing s 750W prototype. Experimentally, the inverter is able to supply a near sinusoidal output voltage with a total harmonic distortion of less than 1%. For comparison, a PSpice simulation of the inverter is also carried out. It was found that the experimental results are in very close agreement with the simulation.

Key Words: Cycloconverter, High frequency link inverter, PSpice, PWM, Voltage surge

I. INTRODUCTION

The transformer isolated voltage source inverter is the main building block of uninterruptable power supplies, aerospace ac power supplies, photovoltaic, wind, fuel cell and other renewable energy conversion systems [1]. A conventional inverter with a line frequency isolation transformer is shown in Fig.1. The H-bridge inverter utilises the pulse width modulation (PWM) scheme to synthesise a sinusoidal voltage. The modulated waveform is low pass filtered to obtain a fundamental sinusoidal voltage which is then stepped-up/down and isolated from the supply using a line frequency (50/60Hz) transformer. Although the topology is simple and inherently allows for bidirectional power flow, the line frequency transformer is very heavy and bulky. With the constant rise in material cost such as copper and steel, a transformer can easily be the most expensive part of an inverter.

Despite the high switching frequency of modern power switches, the transformer size for a conventional inverter remains large because its current is not alternating at high frequencies. To reduce the weight, size and cost, high frequency (HF) transformer link inverters have been proposed [2]. The size reduction is mainly due to the utilization of a ferrite transformer operated in the kHz range. HF link
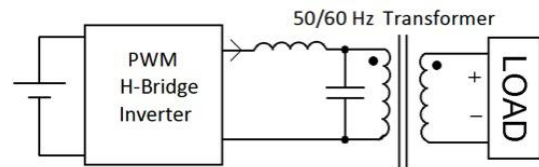
Fig. 1. Conventional line frequency inverter.

inverters can be classified into the resonant and non-resonant types. Resonant HF link inverters combine proper converter topologies and switching strategies to soften the abrupt switching edges of switching device waveforms [3], [4]. There are basically three main categories of resonant converters: load-resonant, resonant-switch and resonant-link converters. They are discussed extensively elsewhere [5]–[8].

Non-resonant HF link inverters utilize conventional "hard-switching" PWM. Two well-known topologies are the "dc-dc" and the "cycloconverter" types. The dc-dc topology cascades a dc–dc forward converter with a PWM inverter. This configuration actually has three power conversion stages: dc–ac in the forward converter primary, ac–dc in the rectification for the dc bus, and dc–ac in the inverter. In a practical circuit, it consists of a PWM H-bridge inverter at the primary side, a high frequency transformer, a rectifier and a polarity-reversing bridge after the secondary [9], [10]. The cascaded conversion would appear to be redundant, since it adds a dc bus that requires an intermediate filtering. As a result, the efficiency is reduced, due to power losses during the forward conduction of the rectifier's switches. Another drawback is that the H-

bridge requires a PWM modulated signal, which makes the transformer design less efficient [8].

To reduce the number of conversion stages, while keeping the desirable HF transformer link, the "cycloconverter type" inverter has been proposed [11]–[17]. This type of inverter appears to be more attractive because it utilizes fewer switches. It shall be the main focus of this work and will be discussed in detail in the following section.

Regardless of the type used, HF link inverters suffer from two major problems, namely (1) a large voltage surge at the transformer secondary and (2) a high switching loss. The voltage surge is due to the fast turn off of the switches that leads to a large transient energy being released by the leakage inductance. Depending on the size of the leakage inductance and the rate of change of the current turn-off, there is a possibility that the surge will exceed the absolute voltage rating of the switch, resulting in permanent damage. In general, surge reduction is achieved by using some kind of voltage clamper or snubber circuit. The high power loss is directly related to the large number of switches (transistors and diodes) that are normally required for HF link topologies. To improve the efficiency, an inverter is forced to switch under zero current switching (ZCS) or/and zero voltage switching (ZVS).

In [18], the voltage surge at the cycloconverter stage is reduced using a voltage clamper. However, the topology and its switching method are complicated; therefore the practical use of this converter is difficult. A variation of this topology, the dc-clamped type switch mode rectifier, was proposed to simplify the control strategy. The circuit utilizes a lossy *RCD* snubber network to limit the secondary voltage spike [21], resulting in a degradation of the efficiency. Alternatively, the authors in [22] proposed a regenerative snubber for a dc-dc type HF link inverter but it requires additional power circuitry with a very complex switching scheme. A flyback-type HF link inverter that inherently operates under the ZCS turn-on condition is described in [23]. By introducing energy regenerative snubber circuits, the ZVS turn-off condition is also accomplished. This circuit has good efficiency but it requires complicated snubber circuits. It is important to note that the flyback type inverter operate in the discontinuous current mode, which results in high current stress and also higher conduction losses. Another interesting method to control voltage surges is proposed by [24] and [25]. This topology consists of a phase-angle controlled cycloconverter that utilized the natural commutation concept. The cycloconverter operates in ZCS and ZVS modes, both at the H-bridge and the cycloconverter stages. The combination of two soft-switching power stages realizes totally the soft-switched HF link converter. Despite these advantages, this topology requires a large number of switches; 12 transistors and 12 diodes altogether.

This paper proposes an improved cycloconverter type HF link inverter. The main contribution of the work is a circuit that utilises fewer switches when compared to other topologies that have similar capabilities and functions [20]–[25]. Furthermore, by using a suitable PWM switching strategy, it is possible to operate two of the diodes and transistors (known as a freewheeling switch) at low frequencies. These improvements decreases the overall power losses and improve the efficiency. To reduce the voltage surge problem, the cycloconverter stage is switched using a phase angle control based on natural commutation. The magnetic energy stored in the leakage inductance at the switching instant is released using the "commutation overlap" phenomena. Thus there is no need for additional surge suppressing circuits. Although the concept of switching overlap is not new, it has not been applied to topologies other than the one proposed in [25].

This paper begins by describing the power circuit topology, followed by an analysis of the commutation phenomena. The two proposed switching schemes, namely the asymmetric bipolar PWM and the edge aligned unipolar PWM, are then described in detail. To verify the theoretical analysis, a 750W laboratory prototype inverter is designed and constructed. The correctness of the results obtained from the experimental hardware are further verified by PSpice simulation.

II. CYCLOCONVERTER TOPOLOGY

A. Conventional ac-ac Cycloconverter

The ac-ac cycloconverter is a natural commutated type converter that is able to control the power flow between the ac supply and the load without an intermediate conversion link [18]. Fig. 2 shows a conventional single–phase cycloconverter. In its basic form, it is essentially a pair of controlled rectifiers connected in inverse-parallel. Consider a case when an output voltage with a frequency that is one forth the input frequency is required. The cycloconverter employs a phase control technique to control the sine wave input voltage. Converter-P operates for the first two cycles of input voltage to rectify the input voltage; therefore, it synthesizes four positive half cycles. In the next two cycles, converter-N operates, and the output voltage is negative. The output frequency can be simply varied by changing the operating period of the converters.

B. Cycloconverter Type HF Link Inverter

The generalized topology of a cycloconverter type HF Link Inverter is shown in Fig. 3. At the primary side, the dc source is chopped to form a high frequency square wave train with a simple 50:50 duty cycle ratio. Then using a control method similar to those in the ac–ac cycloconverters mentioned earlier, a sinusoidal PWM waveform is generated at the output. In this approach, the power conversion is more direct than in the dc-dc type because only two stages are required. Moreover, this topology inherently supports bidirectional power flow and is suitable for power conditioning systems that double as active filters [19].

The simplest way to obtain a sinusoidal PWM waveform at the output of the cycloconverter is to utilize a phase angle control scheme, as depicted in Fig. 4. The cycloconverter itself modulates the incoming square wave to become a bipolar sinusoidal PWM waveform. By using an appropriate switching sequence, it is also possible to generate a unipolar SPWM using this method.
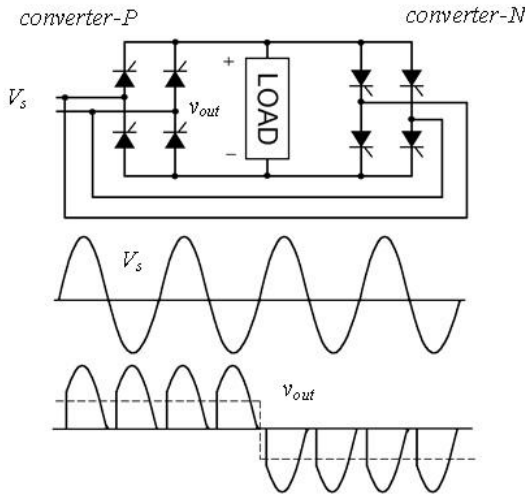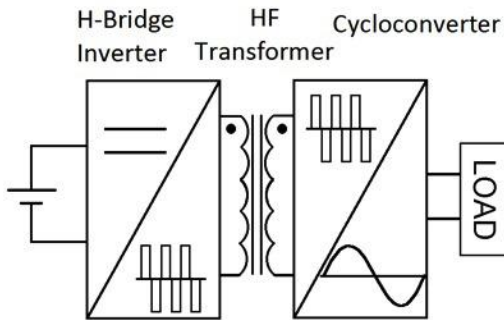
Fig. 2. Single-phase cycloconverter.

Fig. 3. HF link inverter –" cycloconverter" type.

III. THE PROPOSED HF LINK INVERTER

The power circuit of the proposed HF-link inverter is shown in Fig. 5. It consists of an H-bridge inverter, a centre-tapped HF transformer and a cycloconverter stage. Like other topologies, an L-C low pass filter is place at the output to filter the switching harmonics. The H-bridge inverter converts the input dc voltage into a high frequency square wave voltage. When MOSFETs *M1* and *M2* are turned on, V_s appears across the transformer primary. When *M3* and *M4* are turned on, the transformer primary voltage is reversed to $-V_s$. The voltage across the transformer primary is a high frequency symmetrical square waveform (50% duty cycle).

The cycloconverter converts a high frequency square wave into a sinusoidal PWM waveform. Effectively, it is a combination of a controlled centre-tapped bidirectional rectifier and a buck converter. "Powering" switches *SX* and *SY* rectify and regulate the voltage across the transformer secondary while the "freewheeling" switch *SZ* provides the freewheeling path when the powering switch is turned off. Each bidirectional switch consists of a pair of diodes and a pair of transistors. There is no connection between the transistor drain terminals. This configuration enables full control of the current flow directions. Transistors and diodes labeled as group "+" (e.g. *MX+*, *DX+*, etc) are turned on when the load current is positive while the group "–" (e.g. *MX-*, *DXs-*, etc) are turned on when load current (i_{out}) is negative. Transistors of the same bidirectional switch are never turned on at the same instant. The freewheeling switch *SZ* is turned on alternately with the
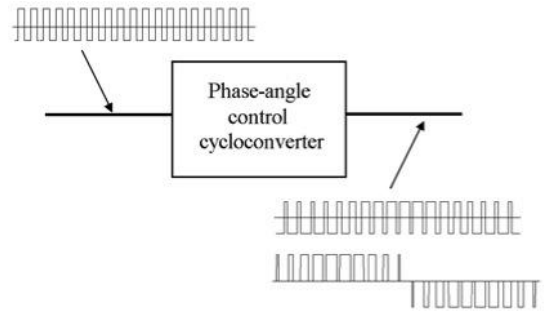

Fig. 4. HF link cycloconverter with phase-angle control. The Fig. shows the waveform before and after the cycloconverter stage.
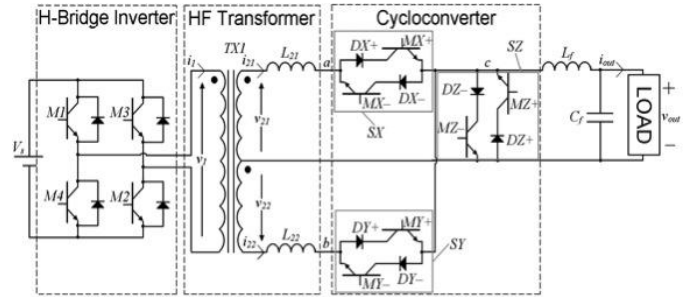

Fig. 5. The proposed cycloconverter type HF link inverter.

powering switches.

The powering switches allow power to flow between the source and the load and vice versa. When the switch *SX* is turned on, the output voltage follows the transformer secondary voltage v_{21}. When switch *SY* is turned on, the output voltage follows the transformer secondary voltage v_{22}. Note that throughout these discussions, the transformer secondary voltages are referred to, with a transformer centre-tapped terminal as a common node. By controlling the duty cycle of the powering switches, an output voltage with various sinusoidal PWM pulse-widths can be generated. Both unipolar and bipolar sinusoidal PWM are possible.

The freewheeling switch *SZ* provides a freewheeling path for the load current when the powering switches are turned off. During freewheeling, no current flows through the powering switches, the transformer or the bridge inverter. The output voltage is drawn to zero. Hence, the conduction loss is reduced during freewheeling intervals. By using unipolar sinusoidal PWM control, a longer freewheeling period can be achieved.

A. Commutation Technique

Forced commutation refers to a current that is forced to zero by turning off the device or by diverting it to another circuitry. On the other hand, if the current of a power device is drawn to zero due to the natural behavior of the source voltage, it is called natural commutation.

1) Commutation on the H-Bridge: A simplified power circuit to illustrate the forced commutation on the H-bridge is shown in Fig. 6. The capacitors C_1, C_2, C_3, and C_4 represent the transistor output capacitances. It is assumed that the transistor leakage inductances are negligible in this analysis. Since the overlapped switching technique is applied, the transformer primary current I_1 lags the transformer primary voltage v_1. It can be assumed that the transformer current remains constant
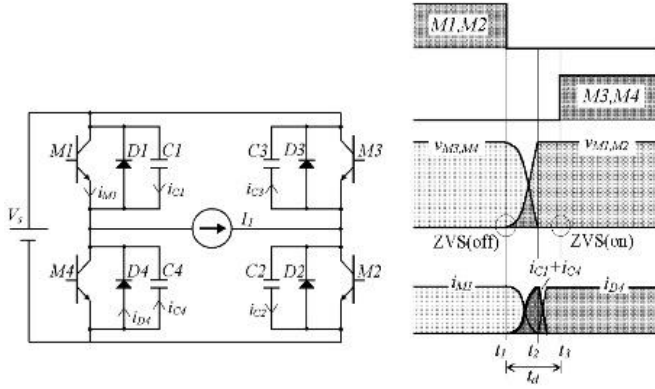
Fig. 6. Forced commutation at H-bridge.

Fig. 7. Forced commutation at the cycloconverter stage.

throughout the transition period. In order to avoid a current shoot-through fault, a dead time t_d is provided between the turn-on time of the incoming and outgoing transistors.

Initially, let both the output voltage and the current be positive. Transistors $M1$ and $M2$ are turned on and the current flows through these transistors. At time t_1, all of the transistors are turned off. The drain current of $M1$ and $M2$ is forced to zero, while C_1 and C_2 are charging, and C_3 and C_4 are discharging. At t_2, the output capacitances are fully charged and discharged, the voltages of the incoming transistors v_{M3} and v_{M4} drop to zero while the voltages of the outgoing transistors v_{M1} and v_{M2} rise to V_s. The transformer primary voltage v_1 is reversed. The anti-parallel diodes $D3$ and $D4$ are turned on and the output current flows back to the voltage source through these diodes. At t_3, the transistors $M3$ and $M4$ turn on under the ZVS condition. Consider only the commutation at the switching leg with the transistors $M1$ and $M4$:

$$i_{M1} + i_{D4} + i_{C1} + i_{C4} = I_1. \tag{1}$$

When the forced commutation process occurs, $D4$ is not conducting. Since $I1$ is constant:

$$\frac{di_{M1}}{dt} + \frac{di_{C1}}{dt} + \frac{di_{C4}}{dt} = 0. \tag{2}$$

Assume that all of the transistors are identical, and have an equal output capacitance, $C_1 = C_2 = C_3 = C_4 = C_{out}$:

$$\frac{di_{M1}}{dt} = -\left(\frac{di_{C1}}{dt} + \frac{di_{C4}}{dt}\right) = -2\frac{di_{Cout}}{dt}. \tag{3}$$

If it is assumed that the charging process is relatively linear:

$$i_{Cout} = C_{out}\frac{dv_{Cout}}{dt}. \tag{4}$$

where $\Delta t = t_2 - t_1$. Therefore:

$$I_1 = 2 \times C_{out}\left(\frac{V_s}{t_2 - t_1}\right) + i_{M1}. \tag{5}$$

From Equation (3), it is clear that the mechanism of forced commutation is mainly determined by the transistor output capacitance, C_{out}. Equation (5) indicates that in order to operate the inverter transistors under the ZVS condition, the load current i_{out} must be large enough to draw a sufficient I_1. Also, the dead time between the transistor turn on time must be longer than Δt to allow for complete voltage transition. The
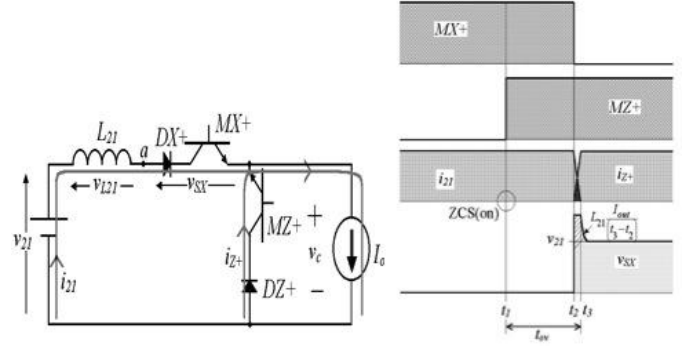
output voltage transition from negative to positive is identical to that previously discussed, as long as the transformer current is lagging. Note that the passive snubber capacitor can be connected in parallel with each transistor to obtain a better control of the forced commutation process. Since the switching transition from $M3$, $M4$ to $M1$, $M2$ is identical to the abovementioned operation, all of the transistors in the bridge inverter stage are also operating under the ZVS condition.

2) Commutation on the Cycloconverter Stage: Natural commutation at the cycloconverter stage enables soft-switching operation and therefore, voltage surge and power loss reductions. However, gate turn-off devices like MOSFETs and IGBTs inherently operate in forced commutation. For the transistors to operate at natural commutation, the turn-on time for the transistors in the cycloconverter stage is overlapped, as explained below.

The cycloconverter stage circuit can be simplified to perform an analysis of the forced commutation, as shown in Fig. 7. The transformer secondary voltage is assumed to be constant. It is modeled as a voltage source in series with an inductor that represents the transformer leakage inductance. Since sinusoidal PWM control is applied, the load can be replaced with a constant current source, and the output voltage is labelled as v_c. Furthermore, the switches that remain turned off are assumed not participated in the operation. Since the overlapped switching technique is applied, during the switching transition between the powering switch and the freewheeling switch, the transistor turn-on time overlaps. The overlap interval is denoted as t_{ov}.

Assume that the input voltage and the load current are positive and that the incoming switch is SZ. Prior to time t_1, $MX+$ is turned on, and the power is transferred from the transformer to the load through this transistor. The load current is constant, so there is no voltage drop across the leakage inductance and v_c is equal to the input voltage magnitude. When $MZ+$ turns on at time t_1, $DZ+$ is reversed biased and it prevents the commutation process. At t_2, $MX+$ is turned off and v_c is drawn to zero to allow the load current to forced commutate from $MX+$ to $MZ+$. The commutation process ceases at t_3 when no more current flows through the transformer. The following equations describe how the leakage inductance causes a voltage surge across SX:

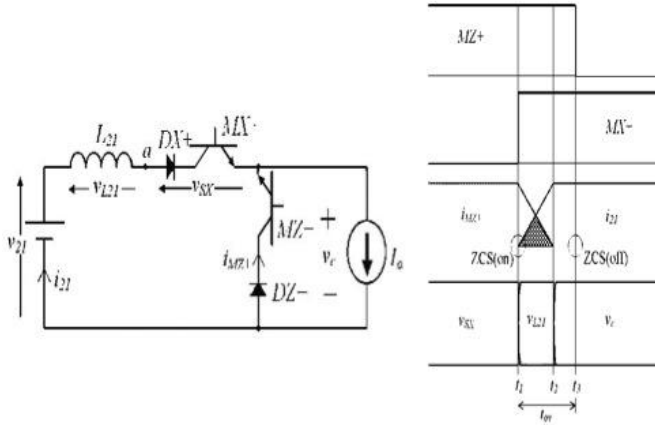$$v_{L21} = L_{21}\frac{di_{21}}{dt} = -L_{21}\frac{I_{out}}{(t_3 - t_2)}. \tag{6}$$

Fig. 8. Operation of natural commutation at the cycloconverter stage.

Apply Kirchhoff's Law to the path:

$$v_{21} = v_{L21} + v_{SX} + v_c. \tag{7}$$

Since v_c is drawn to zero, Equation (6) and (7) can be combined to get:

$$v_{SX} = v_{21} + L_{21} \frac{I_{out}}{(t_3 - t_2)}. \tag{8}$$

Equation (8) implies that during the forced commutation period, the energy stored in the leakage inductance is transferred to the bidirectional switch SX. If the current transition time, i.e. $(t_3 - t_2)$ is small enough, it will generate a sufficient voltage surge to damage the bidirectional switch. Also, note that $MZ+$ turns on under the ZCS condition but that $MX+$ is hard switched. From the analysis performed, it can be seen that if both the transformer secondary voltage and the output current are of the same polarity, the transition from the freewheeling switch to the powering switch will result in forced commutation. Even though an overlapped turn-on time t_{ov} is provided between the switching transition of transistors $MX+$ and $MZ+$, natural commutation does not take place. The following discussions of natural commutation at the cycloconverter stage will clarify the conditions of forced and natural commutation.

3) Natural Commutation at the Cycloconverter Stage: Fig. 8 depicts how the natural commutation at the cycloconverter stage is achieved. The load is a current source, and the output voltage is v_c. During the switching transition between the powering switch and the freewheeling switch, the transistor turn-on time overlaps to allow the natural commutation mechanism to take place.

Assume that both the transformer output voltage and current are positive. Prior to time t_1, $MZ+$ is turned on, and the output current freewheels through the switch Z and the output voltage is kept to zero. There is no current flowing through the transformer, the transistor $MX+$ or the diode $DX+$. When $MX+$ turns under the ZCS condition at time t_1, $DX+$ is forward biased and the potential at point a is literally zero. Since the output current is constant and the input voltage drops across the leakage inductance, the current through $MZ+$ is naturally commutated to switch $MX+$ where the current ramps up. By applying Kirchhoff's Law to the circuit, the following

TABLE I
CYCLOCONVERTER COMMUTATION PROCESS FOR DIFFERENT SWITCHING CONDITION

Transformer secondary voltage	Iout	Incoming switch	Outgoing switch	Commutation Type
$+v_{21}$	+	SX	SZ	Natural
$+v_{21}$	+	SZ	SX	Forced
$-v_{21}$	+	SZ	DX	Natural
$-v_{21}$	+	SX	SZ	Forced
$+v_{21}$	−	SZ	SX	Natural
$+v_{21}$	−	SX	SZ	Forced
$-v_{21}$	−	SX	SZ	Natural
$-v_{21}$	−	SZ	SX	Forced
$+v_{22}$	+	SY	SZ	Natural
$+v_{22}$	+	SZ	SY	Forced
$-v_{22}$	+	SZ	SY	Natural
$-v_{22}$	+	SY	SZ	Forced
$+v_{22}$	−	SZ	SY	Natural
$+v_{22}$	−	SY	SZ	Forced
$-v_{22}$	−	SY	SZ	Natural
$-v_{22}$	−	SZ	SY	Forced

equations are obtained:

$$i_{21} + i_{MZ+} = I_{out} \tag{9}$$

$$\rightarrow \frac{di_{21}}{dt} + \frac{di_{MZ+}}{dt} = 0. \tag{10}$$

Since:

$$v_{l21} = V_{21-peak} \tag{11}$$

and:

$$v_{l21} = L_{21} \frac{di_{21}}{dt} = -L_{21} \frac{I_{out}}{(t_2 - t_1)}. \tag{12}$$

combining Equations (9), (10) and (11) yields:

$$\frac{di_{21}}{dt} = -\frac{di_{MZ+}}{dt} = +\frac{V_{21-peak}}{L_{21}} \tag{13}$$

also:

$$\Delta t = t_2 - t_1 = \frac{L_{21} \times I_{out}}{V_{21-peak}}. \tag{14}$$

where Δ_t is the minimum overlap turn-on time required to complete natural commutation process. The commutation process ceases when the current through $DZ+$ reaches zero. At this instant, the leakage inductance current becomes constant therefore it has no voltage drops. Therefore, the input voltage drops across point c and $DZ+$ is reverse biased. The commutation sequence can be summarized in Table I.

From the analysis, it can be concluded that when the transformer is in the powering mode, i.e. the transformer secondary voltage, v_{21} or v_{22} have the same polarity as the load current i_{out}, the process of storing energy in the leakage inductance can be controlled using the overlapped switching technique. Based on this judgment, it can be predicted that when the transformer is in the regenerating mode, i.e. v_{21} or v_{22} have a different polarity than i_{out}, the process of releasing energy from the leakage inductance can also be controlled. To commutate from the freewheeling switch to the powering switch, the transformer should be in the powering mode. To commutate from the powering switch to the freewheeling switch, the transformer should be in the regenerating mode.
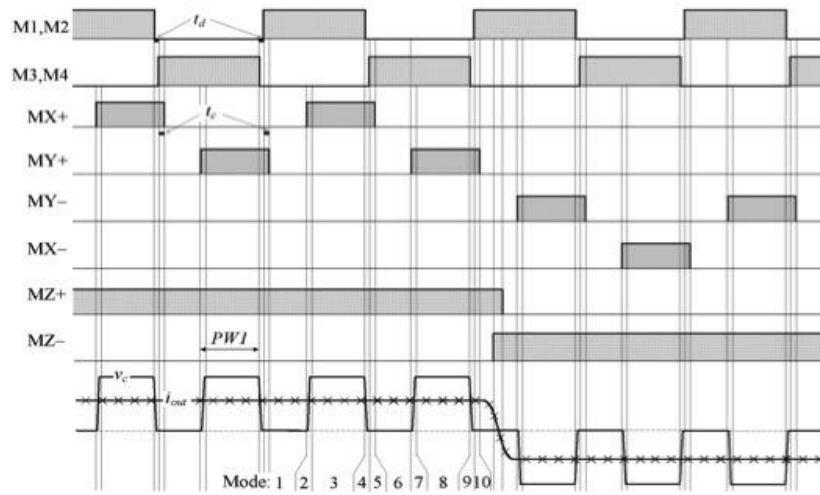
Fig. 9. EAUPWM control signs.

B. Switching Scheme

The switching scheme used is the Edge-aligned unipolar PWM (EAUPWM). Its switching pattern is illustrated in Fig. 9. The output voltage is positively rectified in the first half, and negatively rectified in the second half. To change the output voltage polarity, the switching sequence of the powering switches X and Y must be utilised. Only pulse-width $PW1$ is required to control the powering switches. By using PWM technique to vary $PW1$, the magnitude of the output voltage can be controlled. The transistors in the freewheeling switch SZ are turned on at all times because the diodes in the freewheeling switch provide turn-on and turn-off operation. At the inverter stage, a dead time t_d is added to every switching transition to avoid cross conduction. The overlap natural commutation period t_{ov} is set at the switching transition from the powering switch to freewheeling switch to allow soft-switching and voltage surge reduction. A typical operating waveform has 10 modes; only modes 1 to 5 are explained due to its periodic symmetry. Assume the initial input voltage and the load current are both positive.

- Mode 1 (Freewheeling period): During this period, $M1$, $M2$, $DZ+$, and $MZ+$ are in the "on" state. The load current is shortened with this passage and completely separated from the dc source.
- Mode 2 (1st natural commutation period): $MX+$ is turned on under the ZCS condition to allow the current that flows through $MZ+$ to commutate to $MX+$. When the commutation process ceases, the transformer secondary voltage drops at the freewheeling switch and $DZ+$ is turned off.
- Mode 3 (Powering period): During this period $M1$, $M2$, and $MX+$ are in the "on" state. The instantaneous power flows from the dc source to the load.
- Mode 4 (Inverter dead time period): All four transistors of the inverter are in the "off" state. The current flowing through the HF transformer remains constant because $DZ+$ is still turned off. Therefore, the transformer current is forced commutated from $M1$ and $M2$ to $D3$ and $D4$. Finally, $M3$ and $M4$ turn on under ZVS.

- Mode 5 (2nd natural commutation period): When the forced commutation process at the inverter stage is completed, $DZ+$ is turned on, and load current begins to naturally commutate from $MX+$ to $MZ+$. As the natural commutation process ceases, $MX+$ turn on under the ZCS condition.

IV. EXPERIMENTAL SET-UP

To verify the analysis of the proposed HF-link inverter, a 750W experimental inverter is designed and built. In addition, a Pspice simulation is carried out to validate the experimental results and to check the correctness of the preceding analysis. The prototype consists of two parts; (1) the power circuit and (2) the control signal generation circuits. The control signals are generated using a Siemens MCB80167 fixed-point microcontroller [24]. The pulse width ($PW1$) is calculated by using the regular sampling PWM method proposed by [25]. An International Rectifier IRG4PH50U IGBT and a fast soft recovery diode 60EPF12 are used to build the bidirectional switch. The filter inductor and the HF transformer are wounded on a Ferroxcube ETD59 magnetic core [26]. The switching frequency is set to 10 kHz. The EAUPWM switching scheme is applied.

Snubber circuits are connected in parallel with the transformer secondary terminals. The aim is to reduce the ringing caused by the diode reverse recovery current. Since the current that flow through the leakage inductance is bidirectional, the unpolarized series RC snubber configuration is employed. By measuring the ringing frequency f_r and the leakage inductance L_{leak}, the following equations are used to estimate the values of the snubber resistance R_s and the capacitance C_s:

$$R_s = 2\pi f_r L_{leak} \tag{15}$$

$$C_s = \frac{1}{\pi f_r R}. \tag{16}$$

The transformer secondary leakage inductance is measured at the secondary terminals with the primary terminals shorted. Increasing C_s beyond this value will increase dissipation but will not improve the damping. The empirical method using
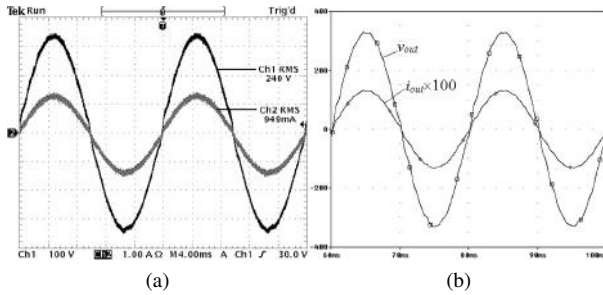
(a)   (b)

Fig. 10. Output waveforms with resistive load. (a) Experimental. (b) Simulation. Vertical scale (experimental): output voltage 100V/div, output current 5A/div, Time scale: 5ms/div.
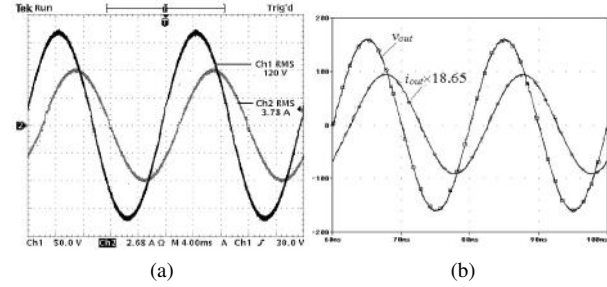

(a)   (b)

Fig. 11. Output waveforms with inductive load. (a) Experimental. (b) Simulation. Vertical scale (experimental): output voltage 50V/div, output current 5A/div, Time scale: 5ms/div.

PSpice is carried out to obtain the optimized values of R_s and C_s. A non-inductive 100 Ω/ 5W thick film power resistor is used. As for the snubber capacitor, a 4.7 μF low loss film and a foil polypropylene appear to be the most suitable.

It should be noted, however, that a PSpice model for the power diode 60EPF12 is not available. A similar model, the APT60D120B from Advanced Power Technology, which has the same characteristics, is used instead. The transformer leakage inductance and the output filter are modeled using parameters measured from the hardware. To reduce the complexity of the simulation, the driver circuit is simulated using an ideal pulse voltage source. Furthermore, the winding resistance of the inductor and the transformers are not included to avoid possible non-convergence problems during the simulation runs.

V. Results and Discussions

A. Output Waveforms

Fig. 10(a) shows the output voltage and the current of the experimental inverter at an output power of 230W. The output filter is chosen as L_f= 1.6mH and C_f= 2.2mF. As can be seen, the output voltage and the current waveforms are almost purely sinusoidal. Fig. 10(b) shows the simulation of the HF inverter under the same operating conditions and component values. As can be seen, there are very close resemblances between the experimental and simulation results. Fig. 10(a) show the experimental waveforms when the inverter is connected to an inductive with a power factor of 0.8. As can be clearly seen, the voltage and current waveforms are not distorted, implying that the inverter is fully capable of bidirectional power flow. The simulation shown in Fig. 13(b) verifies this operation. Using the FFT function of the oscilloscope, the total harmonics distortion of the voltage and current are measured to be less than 1%.

B. Efficiency

Fig. 12 plots the overall efficiency of the proposed inverter (both practical and experimental) with an input voltage of 120V and a switching frequency of 10 kHz over a wide range of output power. For the practical circuit, the efficiency is computed as follows:

1) Using a Voltech PM3000 dual-channel power analyzer, the power at the input and output terminals are measured

simultaneously. The difference between the output and input power (P_{conv_loss}) reflects; (1) the conduction and switching losses of the power switches and diodes, (2) the losses due to the winding resistance of the inductor and transformer and (3) the losses of other stray components in the power circuit.

2) In addition, the power consumption of the driver circuits ((P_{driver_loss}) is also measured. This is considered to be constant at about 10W.

3) If P_o is the defined output power, the overall efficiency can be obtained by:

$$\eta = \frac{P_o}{P_o + P_{loss}}. \tag{17}$$

where $P_{loss} = P_{conv\_loss} + P_{driver\_loss}$. For the Pspice simulation, the efficiency computation is carried out using the built-in power function, marked at the input and output of the power circuit. However, the power consumption of the drive circuit losses is not taken into account because in the simulation the driver pulses are replaced by an ideal pulsed voltage source. Moreover, practical uncertainties such as the winding resistance and the stray components are not modeled to avoid convergence problems.

From the plot, it can be seen that the average efficiency of the practical inverter reaches 90% when the output power is in the range of 300W to 500W. The efficiency at low power i.e. less than 200W is found to be much lower. This is to be expected as power converters, in general, tend to have a lower efficiency when operated at low power [27]. The efficiency drops slightly beyond 500W due to the increase in ohmic losses in the circuit. For comparison, the simulated efficiency is also plotted in the same figure. It can be seen that the measured efficiency is 2-3% lower than the theoretical efficiency. This can be attributed to the fact that the simulation does not take into account the losses in the winding resistances and in other stray components.

Concerning direct comparison with other work, the issue proved to be quite difficult for two reasons: (1) the components (parts numbers) used by other researchers are unknown; as such their electrical and thermal characteristics may not be the same. In some cases, the exact values of the components are not stated. (2) The operating conditions, such as the switching frequency, the input voltage and the power rating of the inverters, as shown in the papers, may be different. Despite these shortcomings, several closely related works are cited here to gain some insight into the performance of
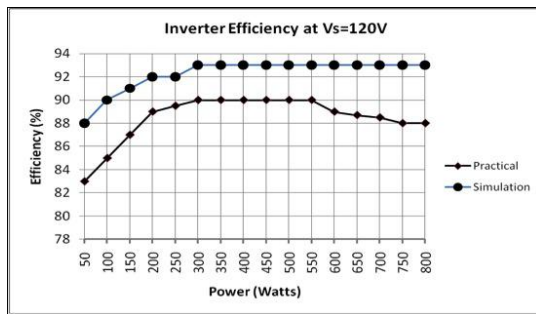
Fig. 12. Overall efficiency vs. output power for the proposed HF inverter.

the proposed inverter. In [23], the overall efficiency of the suggested HF link inverter with asymmetric control is 83%. For a topology that employs the symmetric hard-switching technique and non-regenerative voltage clamp circuits, the efficiency is much lower, i.e. 72%. In both topologies, the inverters are fed by 100 VDC with an input link frequency of 16.7 kHz. Although the types of power switches used are not identified, this factor normally contributes not more than a 1-2% variation to the overall efficiency. In another work [7], the authors have reported an efficiency of 75-85% for their dc-dc type HF link topology. The inverter is rated at 250W, with a very low input voltage, i.e. 23-28VDC. Under these operating conditions, direct comparison with the proposed topology is not very meaningful.

C. Commutation

The principal operating waveforms obtained from the experimental inverter are shown in Fig. 13(a). The current flowing through the transistor *M1*, $I_{C(M1)}$ surges from -0.85A to $+0.5$A in modes 9 and 10. It can be suggested that the negative direction current surge is indeed the current that flows through the anti-parallel diode. The current of the transistor *M4* is forced commutated to the anti-parallel diode of the transistor *M1* during mode 9. This forced commutation process results in ZVS operation at the H-bridge stage. When the commutation process has completed, the voltage across the transformer's secondary gradually increases. In the meantime, a small *RC* snubber, placed across the transformer secondary, draws in current. This results in a current surge (to $+0.5$A) at the primary stage.

The diode reverse-recovery characteristics also affect the switching transition waveforms in modes 2, 5, 7 and 10. At the cycloconverter stage, the diodes are reversed biased when the natural commutation processes are completed. As a result, reverse-recovery current flows through the outgoing bidirectional switch while imposing a positive current surge on the incoming bidirectional switch. The reverse-recovery current oscillates before settling to almost zero ampere, resulting in a voltage overshoot across cycloconverter stage. The *RC* snubbers across the transformer secondary reduce the oscillations in the laboratory prototype. Without the snubbers, an idealized diode requires a longer settling time, even though the magnitude of the reverse-recovery current is relatively small. Fig. 13(b) shows the Pspice simulation of the inverter under the same operating condition. As can be clearly seen from the waveforms, there appears to be very close agreement

between the experimental and simulation results. This confirms the correctness of the analysis that has been carried out on the inverter earlier.

It is not practical to experimentally show the effects on the voltage surge due to the limitation of the device ratings. However, by investigating the waveforms during the natural commutation interval, the operation of the voltage surge reduction can be verified. The first occurrence of natural commutation at the cycloconverter stage is as shown in Fig. 14. Between time t_1 and t_2, the voltage across the transformer secondary, *va* dips to less than half the magnitude of the steady-state voltage. This is because within this interval, the voltage across the transformer leakage inductance drops to allow natural commutation from switch *SZ* to switch *SX*. As a result, the voltage across the transformer secondary is controlled by natural commutation. The use of a *RC* snubber across the transformer secondary results in a slow transition of the voltage across the bidirectional switch. Therefore, the soft-switching operation of the switch *SX* is not obvious at time t_1. The soft-switching operation of the switch *SZ* can be observed during the turn-off instant. The effects of the diode reverse-recovery characteristics can also be observed in the waveforms of I_{DX+} and I_{DZ+}. In addition, the voltage overshoot across the switch *SZ* occurs after the natural commutation has completed at time t_2. This verifies that the voltage overshoot is due to the oscillation resulting from the reversed-recovery current. The oscillation of the reversed-recovery current that occurs after time t_2 is not significant. However, results in a significant oscillation to the voltage across the transformer leakage inductance. The *RC* snubber across the transformer secondary reduces the oscillation in the prototype.

The second natural commutation in Fig. 15 occurs when the voltage across the transformer secondary is inverting from positive to negative. It is observed that the current waveforms during the natural commutation are not as smooth as those shown in Fig. 14. This is because the voltage across the bidirectional switch *SY* is changing from negative to positive. As a result, the current is drawn in to turn off *MY+* and to turn on *DY+*. The current is required to charge and discharge the output capacitances of the power devices. Nevertheless, the soft-switching processes of both bidirectional switches are obvious at time t_1 and t_2. Similarly, the voltage across the switch *SX* overshoots after the natural commutation process at time t_2.

VI. CONCLUSION

This paper describes the analysis and design of a bidirectional and isolated cycloconverter type high frequency link inverter. The main feature of the inverter is its reduced power switch count. It requires the lowest number of switches when compared to other topologies with similar functions and capabilities. To overcome the voltage surge problem, the natural commutation method with an overlapped switching time is applied. Two PWM switching schemes, namely the asymmetric bipolar PWM and edge aligned unipolar PWM, are considered at the cycloconverter stage. For hardware implementation, the latter was selected because it gives better
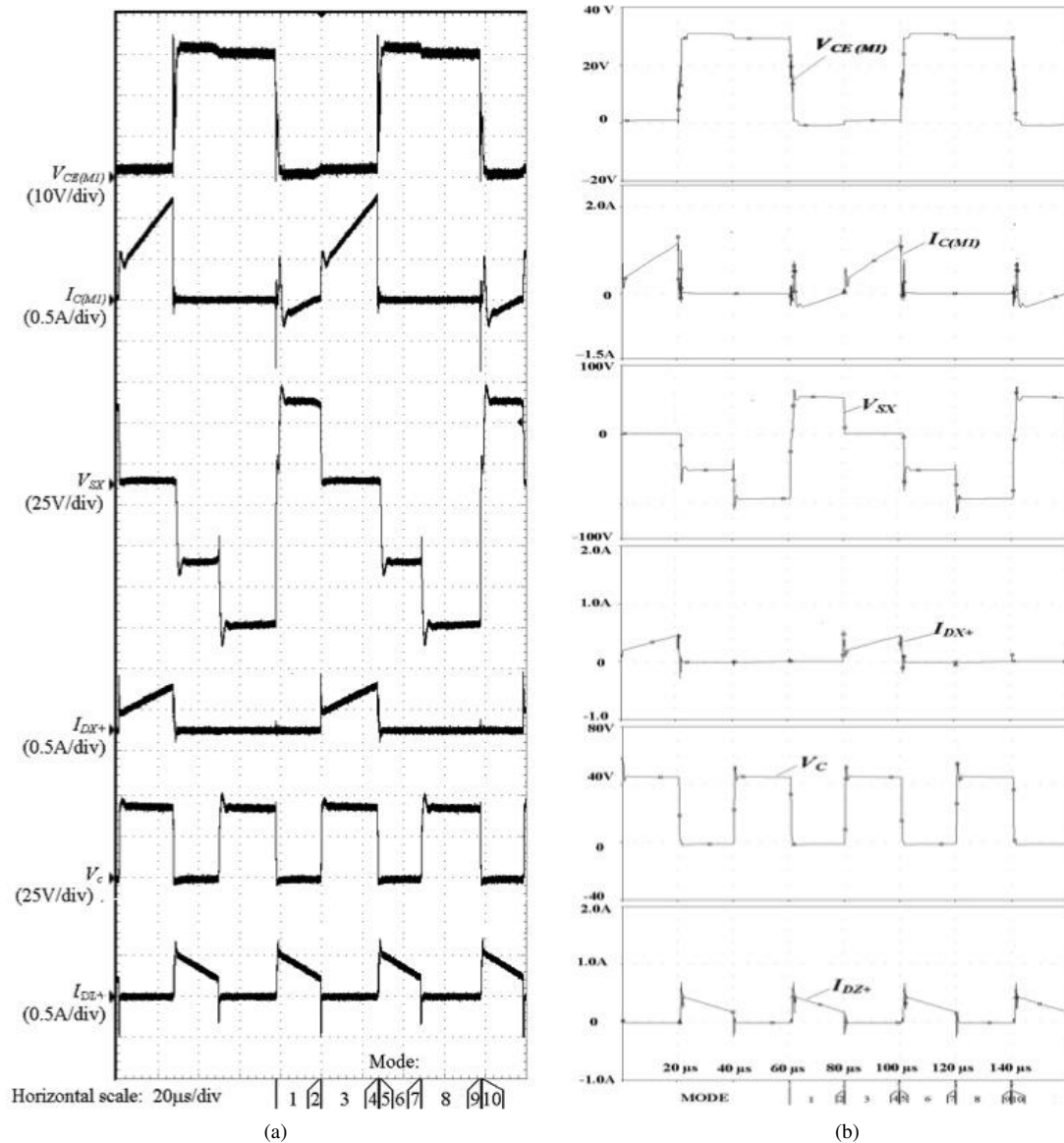
Fig. 13. (a) Experimental operating waveforms (b) Simulated operating waveforms.

efficiency and superior harmonic spectra. To prove the concept, a 750W experimental inverter was built based on a Siemens 80C167 16-bit fixed-point microcontroller. Furthermore, a PSpice simulation was carried out to validate the experimental results. It was found that the laboratory prototype is able to generate a near sinusoidal output voltage with a total harmonic distortion of less than 1%. The conversion efficiency is measured to reach around 90%. The proposed HF inverter can be suitably used for any dc to ac conversion system that requires bidirectional power flow capability.
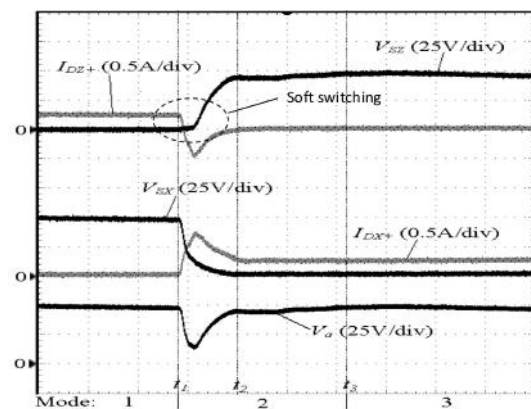
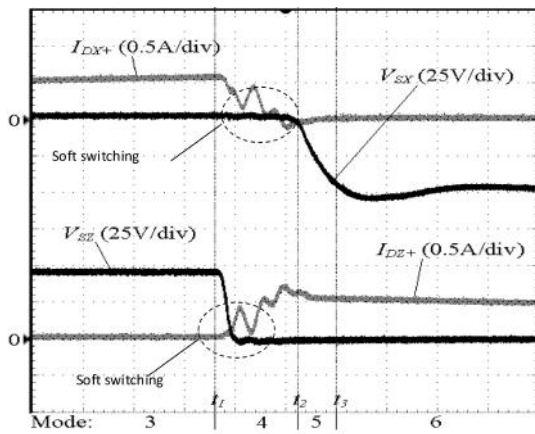Fig. 14. The first natural commutation at cycloconverter stage.

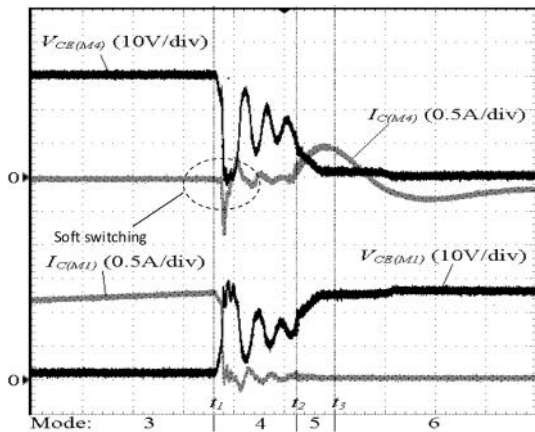Fig. 15. The second natural commutation at cycloconverter stage.

Fig. 16. Forced commutation at bridge inverter stage.

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