IMPACT OF NANOMETER TRANSISTOR ON ANALOG PERFORMANCE

MOHAMAD ASFA HUSAINI BIN ZAKARIA

A thesis submitted in fulfilment of the
requirements for the award of the degree of
Master of Engineering (Electrical)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

DECEMBER 2011

To my beloved father and mother

ACKNOWLEDGEMENT

I would like to express my gratitude to the people who helped me during the research. Firstly, i like to thanks to Prof. Dr. Abu Khari A'ain for being a good and supportive supervisor to me. The guidance and encouragement he showed is the key to the successful of this project.

I also would like to express my thanks to En Izam Kamisian and Muhamad Faisal Bin Ibrahim. They had provided me with brilliant ideas and supportive feedback to aid me in my technical paper writing and research.

Next, I would like to thank my parent. They are really supportive and always encourage me to finish up this project. I would also like to thank to my friends, Muhamad Ridzuan bin Radin Muhamad Amin and Mohd. Fairus bin Ahmad for sharing information and knowledge. Their contribution in this project really helps me to develop my knowledge and understanding.

Lastly, I extend my acknowledgement to Intel Technology Sdn. Bhd. for providing the research grant for the project.

ABSTRACT

Scaling down of transistor dimension is generally being well accepted and adapted by digital designers as they could introduce more design features at almost no increase in silicon area. However, for analog designers, using smaller transistors in their design would cost them extra design efforts as they have less design headroom in hand –amongst others are low supply voltage, signal to noise ratios and transconductance. These issues become more obvious as designers are now using transistor size in nanometer region. This calls for better understanding on how smaller transistor affect circuit performance. This research addresses the above issues, using predictive transistor model, process technologies of 130 nm, 90 nm, 65 nm, 45 nm, and 32 nm as case studies. Analyses have been be carried out to understand which of the analog performances such as gain, power dissipation, output voltage swing, and cut-off frequency would be severely affected as the process shrinks to nanometer region. The circuits designed for the research have also been subjected to variations in process corner namely typical, slow, and fast. The outcome of the research points out several disturbing impacts of nanometer size transistors. First of all, its impact on analog performance of cascode amplifier is truly a great concern. Low voltage supply in nanometer transistors presents a design challenge to cascode amplifier in circuit design. Almost all its major performances are severely affected. For telescopic amplifier circuit, the analog performances such as gain and cut-off frequency are also greatly affected due to linearity issues of the design when one moves toward smaller transistor sizes. However, results on differential circuits have some positive news as it helps soften the impact on voltage gain and voltage swing. It is also worth to mention that based on rough estimation, designers would take longer time to complete the design task, thus slowing down the time of manufactured devices to be marketed.

ABSTRAK

Pengecilan dimensi bagi transistor secara umumnya diterima baik khususnya bagi pereka litar digital di mana mereka dapat memperkenalkan lebih banyak rekaan-rekaan terbaru tanpa perlu bimbang akan kepadatan transistor dalam ruang silikon. Namun begitu, bagi pereka litar analog penggunaan dimensi transistor yang kecil di dalam rekaan litar menyebabkan mereka memerlukan masa serta usaha yang lebih memandangkan terpaksa menghadapi ruang operasi yang lebih kecil. Antara lain adalah sumber bekalan voltan yang kecil, nisbah isyarat-hingar dan trankonduktan. Hal ini menjadi lebih kritikal dengan penggunaan saiz transistor dalam skala nanometer digunakan oleh pereka litar analog dalam rekaan pada masa ini. Dengan ini, pemahaman yang lebih mendalam mengenai kesan penggunaan dimensi yang kecil kepada prestasi litar adalah perlu untuk meringankan beban hasil daripada penskalaan dimensi transistor ini. Penyelidikan ini memberi fokus kepada isu-isu di atas dengan menggunakan model ramalan transistor iaitu 130 nm, 90 nm, 65 nm, 45 nm, dan 32 nm dalam projek ini. Analisis telah dijalankan untuk memahami prestasi litar analog yang manakah akan terjejas teruk apabila teknologi proses nanometer digunakan. Prestasi litar analog yang dikaji tersebut adalah gandaan voltan, kuasa lesapan, ayunan voltan keluaran dan sambutan frekuensi. Proses variasi iaitu “typical”, “slow”, and “fast” dilaksanakan pada rekaan litar analog tersebut. Hasil daripada penyelidikan ini, terdapat beberapa impak negatif dalam nanometer transistor. Pertamanya adalah impak prestasi rekaan litar analog pada penguat kaskod. Sumber voltan yang rendah dalam nanometer transistor telah mewujudkan satu bentuk cabaran dalam merekabentuk penguat kaskod dalam litar analog. Hampir kesemua prestasi litar terjejas dalam penguat kaskod. Bagi litar penguat teleskopik, apabila dimensi proses teknologi berganjak ke dimensi yang lebih kecil, prestasi analog seperti gandaan voltan dan sambutan fekuensi terjejas akibat isu kestabilan dalam rekaan litar. Namun demikian, hasil dari pemerhatian pada litar penguat pembeza, ia telah menunjukkan satu perkara yang memberansangkan di mana impak kepada gandaan voltan dan ayunan voltan keluaran dapat dikurangkan. Selain daripada itu, berdasarkan kiraan secara kasar, peruntukkan masa yang lebih akan diperlukan oleh pereka litar analog dalam merekabentuk litar dan ini akan menjurus kepada kelewatan peranti yang dikilang untuk dipasarkan.

TABLE OF CONTENT

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOL

V_{gs}	-	Gate-to-source voltage
V_{gd}	-	Gate-to-drain voltage
V_{ds}	-	Drain-to-source voltage
V_{th}	-	Threshold voltage
V_T	-	Thermal voltage
V_{dd}	-	Supply voltage
$V_d/V_s/V_g$	-	Drain/source/gate voltage
V_{out}	-	Output voltage (logic) for gate leakage detection circuit
V_{limit}	-	Limit voltage corresponds to allowable I_{gtotal} level
I_d/I_{ds}	-	Drain current
I_{bias}	-	Biasing current
I_{ref}	-	Reference current
TT	-	Typical process corner
FF	-	Fast process corner
SS	-	Slow process corner
A	-	Open loop gain
T_{ox}	-	Oxide thickness
L_{eff}	-	Effective channel length
Ndep	-	Channel doping
C_{ox}	-	Oxide capacitance
C_{js}	-	Depletion region capacitance
W	-	Channel width
L	-	Channel length
T	-	Temperature
λ	-	Channel length modulation
μm	-	micrometer
nm	-	nanometer

LIST OF ABBREVIATION

CMOS	-	Complementary Metal Oxide Semiconductor
SoC	-	System On Chip
NIMO	-	Nanoscale Integration and Modeling
ASU	-	Arizona State University
MOS	-	Metal Oxide Semiconductor
IC	-	Integrated circuit
MOSFET	-	MOS Field effect transistor
NMOS	-	n type MOS
PMOS	-	p type MOS
BSIM	-	Berkeley short channel IGFET model
SPICE	-	Simulation Program with Integrated Circuit Emphasis
CUT	-	Circuit under test
BSIMPD	-	BSIM partial-depletion SOI MOSFET model
SOI	-	Silicon on insulator
PTM	-	Predictive Technology Model
CD	-	Critical Dimension
ACLV	-	Across the Chip Length Variation
SNR	-	Signal Noise Ratio
RDF	-	Random Dopant Fluctuations
LER	-	line-edge roughness
LWR	-	line-width roughness
DR	-	Dynamic Range
TT	-	typical process
SS	-	slow process
FF	-	fast process

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Background

In the past, analog design has comfortable settled down using large scale of complementary metal oxide semiconductor, CMOS transistor. But, it is quite obvious that when analog designs move to smaller dimensions, there should be considerable improvements in performances. Though such advantages are obvious, the finding of the pathways to their realization is a hard task. Careful examination is required in both physical device behaviors and simulation methods. Attempts to design analog circuits at smaller dimensions come with a price. There are a lot of problems that are new to most of analog designers.

As transistors size move towards smaller dimension, the problem faced by circuit design engineers becomes more pressing and this is especially true for analog designers. The nature of analog design which is very sensitive to process variations pose serious design issue when one does vertical or horizontal migration. Horizontal migration refers to migration from foundry to foundry due to economic or costs reason. Vertical migration refers to migration from one process node to smaller process node. Between these two, vertical migration causes serious concern as smaller transistor dimension bring with it new sets of design issues which are of not real concern for digital circuits. An example is channel modulation, λ which has big impact on analog circuit performance. Its value is getting smaller when it migrates to

smaller node which causes difficulty for analog designers to achieve high gain and good match between transistors. For that reason, analog designers will continuously iterate the design cycle till all the design specifications are met. In the era where competitors are aiming to reach their product to market as early as possible, this traditional analog design process is surely of great concern.

The above scenario cause serious concern for analog designers and one of the approaches which could be taken is to make sure that they have the knowledge on the impact of vertical scaling on circuit performance. Since smaller device behavior is very difficult to model accurately, analytical descriptions used for circuit simulation will inevitably introduce further error into the design effort. Thus it could be pointed out that it is an utmost important for analog designers to appreciate and understand which of the design parameters would severely affect design specifications as this could reduce time to market through reduction in fine tuning the design.

1.2 Problem Statement

Demand for System On Chip (SoC) has led to the integration of mixed mode digital and analog circuits on the same substrate. In digital design, the fundamental idea of 'more is better' [15] tells us an obvious challenge in analog design. It is not surprising that most of the design infrastructure is focused on digital applications, particularly in the nanometer regime. However, with considerable growth occurring outside of mainstream 'computational' applicators (such as communications), increasing attention is being paid to 'analog issues' in both simulation and design. As these issues begin to be addressed, analog design at smaller dimensions becomes possible.

This has left analog designers of no choice but to face design problems introduced by the nanometer size transistors. The problems to maneuver and 'juggle' all the design specification require deep understanding of how the process affects the circuit performance. Only with good understanding of the challenges brought by small size transistor will pave the way for fine tune in the design process to meet all design specifications. Good understanding of the challenges will only be available

once detail analysis has been performed on the advantages and disadvantages of analog performance posed by small transistor size in particular nanometer range.

1.3 Research Objective

This research aims to focus on these issues:

1. To study the impact of vertical scaling on analog circuit performance based on several generation of Predictive Technology Model (PTM) which was developed by Nanoscale Integration and Modeling (NIMO) Group at Arizona State University [1]. The processes are 130 nm, 90 nm, 65 nm, 45 nm and 32 nm. The study was conducted through literature review as well as hand calculation and simulation work using Tanner Tools design software. Analog specifications such as power dissipation, gain, output resistance, cut-off frequencies and stability have been used as gauge meter to determine the impact of vertical scaling on smaller transistor dimension.
2. To evaluate the effectiveness of design reuse
3. To find out the degree of design difficulty when design migrates to nano region process

1.4 Scope

There are 3 phases in this research. This research was totally based on simulation using PTM which is 130 nm, 90 nm, 65 nm, 45 nm and 32 nm processes. Circuit performance such as gain, power dissipation, output swings were monitored in all process corners analysis.

Based on available PTM models, sample circuits which are widely used have been designed. In particular, the performance of single input and differential inputs circuits were compared. Circuits such as cascode amplifier, simple differential amplifier as well as differential telescopic amplifier have been used as sample circuits. All these circuits have been simulated in process corners analysis to

understand the impact of scaling down on specific circuit performance. Analyses have also been carried out on circuit performances mentioned above. Comparison on performance was also conducted to get more insight on design issues. Analysis on design time has also been conducted as the node process move toward smaller dimension.

1.5 Contributions

The literature review conducted in this research indicates that there is inadequate work conducted to analyze the impacts of transistor scaling in nanometer regime which focuses more on circuit analog performances such as output voltage swing, cut-off frequency despite the impact on gain and power dissipation. The usage of mathematical analysis in nanometer transistor seems hard to deal with since there are many more physical parameters have to be considered than before. Because of that, researchers always tend to use mathematical CMOS level 1 model. Since most researchers tend to use mathematical analysis, the actual impact of transistor in nanometer regime will not entirely visible. Thus, in order to understand the impact of nanometer transistor, the data were manipulated into figures and tables. This is the main contribution of this work since a lot of data based on simulation results from 130 nm, 90 nm, 65 nm, 45 nm and 32 nm processes are presented.

The concept of 'design reuse' that has been introduced by other researchers is also less reliable when the transistor size moves towards a smaller dimension. This is another contribution of this work where it is shown that 'reuse design' has its own issue.

Another contribution of the work come from the result presented from differential amplifier which shows that it is less affected by vertical scaling. The last but not least contribution is an indicator that shows design time will be prolonged as one migrates towards nanometer region.

1.6 Thesis Organization

There are five chapters in this thesis. In chapter 1, the background of this research is introduced to highlight a general idea about this research as well as the problem statement, research objectives, project scope and its contributions.

Literature review is covered in chapter 2. This chapter consists the research papers that been studied during this research. The introduction of process variation in analog design is discussed in this chapter. Besides, the design challenges as well as scaling effect in nanometer transistor are also discussed in this chapter. At the end of chapter 2, recent works by other researchers on nanometer transistor are introduced.

The methodology of this research is described in chapter 3.The flow of the circuit simulation is described as well as the explanation on how to rewrite the SPICE model parameter to include the process variation effect in it. The explanation of analog circuit performances is also included in this chapter.

Chapter 4 consists the analysis regarding the impact of nanometer transistor on analog performances. There are three types of analysis in this chapter which are the impact of corner process, node process and transistor size to analog performances in nanometer transistor.

The last chapter which is chapter 5 concludes this research and recommends possible future work.