**Student Paper**

# Modeling and Simulation of Nanoscale Temperature Behavior for Multilayer Full Chip System

Norma Alias*[a], Md. Rajibul Islam[b], and Abdul Hafidz Haji Omar[c]

[a] *Ibnu Sina Institute, Faculty of Science, University Technology Malaysia, Malaysia,*
[b] *Department of Mathematics, Faculty of Science, University Technology Malaysia, Malaysia,*
[c] *Department of Therapy & Rehabilitation, Faculty of Biomedical and Health Science Engineering, University Technology Malaysia, Malaysia.*
*Email: norma@ibnusina.utm.my

Thermal effects become gradually more significant as devices get smaller on-chip. Modeling and simulations indicate that chip temperatures will increase exponentially beyond acceptable values, prompting researchers to investigate thermal effects. Research and technology development at the atomic, molecular or macromolecular levels, in the length scale of approximately 1 - 100 nanometer range, to provide a fundamental understanding of phenomena and semiconductor devices at the nanoscale and to create and use structures, devices and systems that have novel properties and functions because of their small and/or intermediate size (US NSET, 2000).

Temperature is defined as the average kinetic energy of all particles in the sample. According to the theory, there should be a standard divergence to go along with this average, but we have yet to see a thermometer that gives standard variation. When one considers temperature in mixtures of different kinds of molecules or systems that are not at equilibrium, at the nanoscale there should be localized regions of various temperatures contributing to this average.

Temperature distribution is frequently calculated in non-equilibrium molecular dynamics simulations. This paper focuses on the nanoscale temperature behavior modeling for multilayered full-chip system. The simulation involves a large scale of computational complexity and high cost of execution time. Therefore, an early prediction of temperature behavior for the system using mathematical simulation is required. In this study, we proposed the development of partial differential equation based on Poisson's equation of two dimensional elliptic equation. Subsequently, with the algorithm introduced by Wang & Mazumder (2004), we developed a C language programming code to promote the modeling of the power density distribution as well as the temperature behavior of multilayer full-chip structure. Green function is one of underlying concept under Boundary Element Method (BEM), The Green function describes the temperature distribution in the chip when a unit point power source is present. Numerical computational method such as BEM is often used in solving partial differential equations that have been formulated into integral equations. Its involve placing source and field plane near each other and gathering the temperature distribution data inside the full chip when a unit of power source is located. In this study, Green Function is being used due to its ability in solving inhomogeneous differential equations depending on boundary conditions of semiconductor devices. In multilayered chip structure, the continuity conditions are enforced between adjacent layers where the bottom surface of each chip is assumed to be convective (Zhan & Sapatnekar, 2005).

In these theoretical models, the kinetic energy of each particle at various points in time is taken into account in order to provide a better understanding of molecular scale events. One might then define local temperature as - the average kinetic energy of a specified set of atoms within the system. While this is still a classic method, it allows discrete statements to be made about localized parts of a system.



978-1-4244-8854-4/10/$26.00 ©2010 IEEE

This algorithm takes only four iterations in about 656042 $\mu s$ in completing the calculation and the computational complexity is 1600 $m$. The computational complexity involves 16,000 times of multiplication, 3200 times of addition and 3200 times of division. Figure 3 shows the power density distribution on a field plane (M x N in size), when a power of 1W given on the same size source plane. The two-dimensional temperature profile is visualized in figure 4, while figure 5 shows the three-dimensional temperature behavior on multilayered full chip of nanoscale structure. The temperature distribution is dependent on the value of power density given to the multilayered chip. The benefit of nanoscale temperature behavior prediction is to reduce the numbers of rejected full-chip. In chip industry, the process in visualizing the power and temperature distribution on multilayered chip involves large scale of computational complexity.

The novelty of our research is the simulations of power density modeling and temperature distribution inside the multilayered full-chip nanoscale structure governing by Poisson's equation of two dimensional elliptic equation. The accuracy and efficiency of the simulation on nanoscale structure will show the power distribution of a full-chip system associated with the temperature profile using the proposed Poisson's equation. The potential future research would be to develop and implement the parallel algorithm of the power density and temperature visualization on distributed parallel computer system.

**References**

[1] B.Wang and P. Mazumder, "Fast Thermal Analysis for VLSI Circuits via Semi-analytical Green's Function in Multi-layer Materials," *IEEE International Symposium on Circuits and Systems*, pp. 409-412, 2004.

[2] Y. Zhan and S. S. Sapatnekar, "A High Efficiency Full-Chip Thermal Simulation Algorithm," *Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design*, pp. 635 – 638, 2005.

[3] US NSET, *Definition of Nanotechnology*, February 2000. http://www.nsf.gov/crssprgm/nano/reports/omb_nifty50.jsp

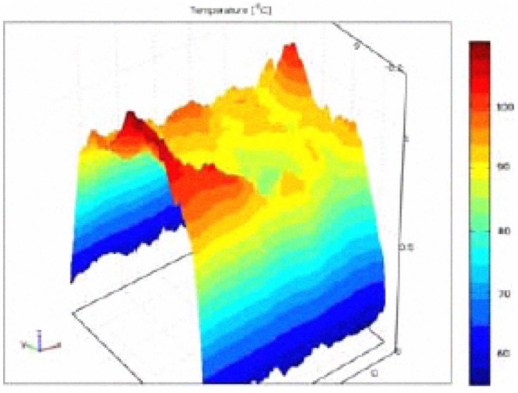

Fig. 1: 3D prediction of temperature behavior

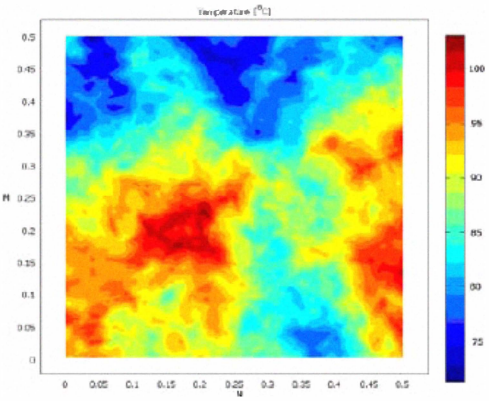

Fig. 2: 2D temperature profile

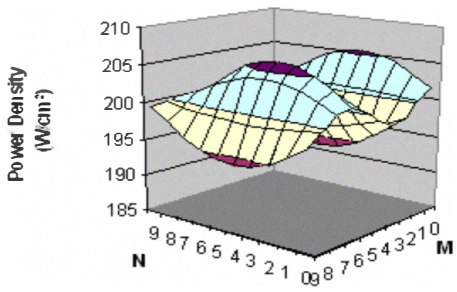


Fig. 3: 2D power density distribution