USB SOFT CORE WITH ALTERA NIOS PROCESSOR

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To my beloved wife

and son

who was born during the study of this course

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ABSTRACT

This objectives of this project learning the process of implementing an System-on-Chip (SoC) using the Altera development board. The chosen board is the Excalibur board which consists of the APEX 20KE200 FPGA. Besides this, Quartus II software is needed as the platform for the development of this project. USB was used as example soft core component to be added to the SoC with the IP obtained from the Opencores web site. As the Nios the system uses the Avalon bus system, while the USB IP core is built for Wishbone bus system, a bridge which allows the both bus systems to communicate was required. This project succeeded in proving the functionality of the bridge. The USB core can either be programmed as Host or Slave. For the USB to communicate to the outside world, physical (PHY) layer circuit was required. The PHY chip used was the Fairchild USB1T11A. To build the PHY printed circuit board (PCB), the Santa Cruz connector located on the Altera development board was used. The PHY circuitry was built on a PCB which was then plugged into the Santa Cruz connector. The final task for the project was testing the USB driver.

ABSTRAK

Objektif projek adalah untuk mempelajari proses pembangunan System-on-Chip (SoC) dengan menggunakan papan pembanguanan Altera. Papan yang dipilih adalah papan Excalibur yang menggunakan FPGA APEX 20KE200. Disamping itu, perisian Quartus II diperlukan sebagai pelantar bagi pembangunan sistem projek ini. USB dipilih sebagai komponen teras lembut yang akan dikaji dengan menggunakan IP yang didapati dari laman web Opencores. Disebabkan mikropemproses Nios menggunakan sistem bas Avalon, sedangkan teras IP USB menggunakan sistem bus Wishbone, satu titi yang dapat menghubungkan Wishbone dengan Avalon diperlukan. Projek telah berjaya membuktikan fungsi titi tersebut. Teras USB ini boleh dijadikan sebagai *Host* atau *Slave*. Untuk USB ini berkomunikasi dengan dunia luar, litar fizikal (PHY) diperlukan. Komponen PHY yang digunakan adalah komponen USB Fairchild USB1T11A. Untuk membina litar PHY ini, penyambung Santa Cruz yang ada pada papan pembangunan Altera ini digunakan. Litar PHY ini dibina pada papan litar bercetak yang kemudiannya akan disambungkan pada penyambung Santa Cruz. Langkah terakhir merupakan pengujian pemacu USB.

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LIST OF ABBREVIATIONS

RISC	-	Reduced Instructions Set Computer
FPGA	-	Field Programmable Gate Array
DSP	-	Digital Signal Processing
SOC	-	System on Chip
UART	-	Universal Asynchronous Receiver Transmitter
DAC	-	Digital Analog Converter
ADC	-	Analog Digital Converter
USART	-	Universal Synchronous Asynchronous Receiver Transmitter
ARM	-	Advanced RISC Microprocessor
USB	-	Universal Serial Bus
DMA	-	Direct Memory Access
SOPC	-	System On Programmable Chip
IP	-	Intellectual Property
Mbps	-	Mega bits per second
CRC	-	Cyclic Redundancy Check
NRZI	-	Non Return to Zero Inverted
FIFO	-	First In First Out
PHY	-	Physical Layer
SDK	-	Software Development Kit
CPU	-	Central Processing Unit
PLD	-	Programmable Logic Devices

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CHAPTER 1

INTRODUCTION

1.1. Background

In today's technology trend, Design and Reuse (D&R) is the current trend of technology with the implementation of IP core based SoC Design. The Altera FPGA is widely used as the programmable device to support the D&R. This is even more convenient with the development of System on Programmable Chip (SOPC) where Altera is leading the industry with its FPGA chips and the Quartus Application tools.

The Altera Nios is 32-bit softcore RISC processor that is optimized for Altera field-programmable gate array (FPGA) devices. It is a powerful embedded processor and is mainly used to control reconfigurable circuits running on the Altera FPGA.

A USB core is quite useful to implement a system-on-chip (SoC) that can connect to a wide variety of devices.

1.2. Literature Research

The availability of open source intellectual property (IP) cores such as those archived by OpenCores is a step in this direction. Most of the open source cores are designed for Wishbone SoC bus compatibility. Some work will be needed to make the open-source cores to work seamlessly with the Avalon bus present in Nios.

1.3. Objective

The main objective of the project is to**o implement USB soft core on Avalon Bus for Altera Nios Processor.**

In more details, it can be illustrated as below:

- Implement USB softcore on Avalon bus
- Configure the USB softcore in FPGA using the Altera development board with Nios processor
- Perform USB communication testing with external device

For academic learning the objective is to implement a USB softcore, like those that can be downloaded from the OpenCores, normally in Wishbone Bus, on a Nios Processor which has Avalon Bus.

One of the ways to do is to connect the USB softcore with Wishbone Bus to a bridge to Avalon Bus. However, since this is an academic project, with the objective to learn about SOC, this is perfectly a project that can provide the learning towards learning SOC, Embedded System, IP cores, USB as well as software development for Embedded System.

In order to complete this project, there are a few skills that need to be acquired.

These skills are:

- Understanding of the APEX Development Board
- Using Quartus II/SOPC in instantiation of the Nios System
- Familiarization in using the SDK
- Understanding of the Avalon Bus
- Understanding of the USB

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