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ANALYSIS AND CONTROL OF THE UNLOADED BI-DIRECTIONAL DC/DC CONVERTER TO PERFORM AN ACTIVE DAMPING FUNCTION

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Abstract. The sub-system interaction and instability phenomena is a common problem in the Distributed Power System (DPS). The interaction arises because an individual converter known as constant power load (CPL), has internal control function such as to regulate the converter output voltage, which results in the converter tends to draw a constant power. The input impedance of CPL has a negative incremental input impedance, which tends to create instability as it is connected to a system. This paper presents the analysis and control of the DC-DC converter used to perform an active damping function in a DPS, comprising L-C filters and CPLs. The DC-DC converter was modelled using averaged technique. The small-signal analysis is performed and the controller was designed on such a way to regulate the converter input current. The design of the control loop parameters based on the frequency domain is demonstrated. The effectiveness of the active damping method was verified by MATLAB Simulink simulation.

Keyword: Active damping, DC-DC converter, averaging technique, constant power load, distributed power supply

Abstrak. Interaksi di antara sistem dan fenomena ketidakstabilan adalah masalah biasa di dalam sistem kuasa teragih. Fenomena ini wujud kerana penukar bersifat beban berkuasa tetap, iaitu sistem kawalan dalamannya yang berfungsi menetapkan voltan keluaran penukar. Galangan masukan bagi penukar adalah bergalangan negatif menaik yang menjurus kepada ketidakstabilan.
Dalam kertas kerja ini, analisa dan kawalan terhadap penukar AT-AT yang berfungsi sebagai pemampas aktif telah dilakukan. Penukar AT-AT disambungkan ke sebuah sistem mudah yang terdiri dari penapis L-C dan sebuah beban berkuasa tetap. Penukar AT-AT telah dimodelkan menggunakan teknik purata, dan analisa isyarat kecil telah dilakukan bagi mereka bentuk pengawal bagi mengawal arus masukan penukar. Reka bentuk parameter gelung kawalan adalah berpandukan kepada domain frekuensi. Keberkesanan pemampas aktif dibuktikan menerusi simulasi MATLAB Simulink.

Kata kunci: Pemampas aktif, penukar AT-AT, teknik purata, beban berkuasa tetap, bekalan kuasa teragih

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1.0 INTRODUCTION

Sub-system interaction and instability phenomena is a common problem in DPS. DPS is a system, usually DC, where the power processing functions are distributed among many power processing units or DC/DC converters at the point of need. The DPS is increasingly being used in applications such as aircraft, spacecraft, hybrid-electric and electric vehicles, ships, defense electronic power systems, industrial production lines, communication, and computer systems. It is due to its beneficial in terms of weight, size, isolation, voltage regulation, flexibility, capability to integrate a large variety of loads, and also enables one to control more easily the quality of power reaching each separate board [1 - 2]. However, DPS has some drawbacks such as interaction between the converters and bus instability, as well as imbalance in power distribution among parallel converters, which leads to an unequal distribution of output current, hence may create excessive stress on some of the modules and increase their rate of failure [3 - 5].

Since the cost has reduced, switching regulators are more widely used in many applications. Very often with one switching regulator serving as the source for several other converters, for example switching regulators, inverters and motor drives, the potential for load-source interaction is therefore, very high. The interaction arises because each individual converter has internal control functions, such as the regulation of the converter output voltage or motor speed. As a result, the converter tends to draw a constant power and therefore, has a negative incremental input resistance within the bandwidth of the converter control loop. When the source voltage falls, then the operation of the internal controller results in the converter drawing more current. This in turn could cause the source voltage to fall even further.

This paper discusses in detail a DC/DC converter which may be used to perform an active damping function in a DPS comprising L-C filters and CPLs. The first topic is the proposed circuit and its waveforms. The second topic is on the converter averaged modelling and small-signal analysis techniques in which the derivation of the transfer functions of the converter is performed. The third topic discusses on the regulation of the converter input current in both operating modes - sinking and sourcing power. The fourth topic is on the design of the control loop parameters based in the frequency domain and also explains the design of converter output voltage control loop, as well as the integrator wind up phenomena. The effectiveness of the averaged model is verified in the Matlab Simulink simulation.

2.0 BASIC CIRCUIT AND WAVEFORMS

A basic block diagram of the damping network connected to a DC bus is shown in Figure 1 and the detailed circuit configuration of the active damping network is shown in Figure 2. The active damping network in Figure 2 utilises capacitive and inductive energy storage elements as well as a half-bridge leg. This network was

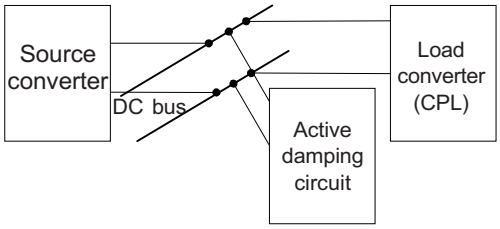


Figure 1 System connection block diagram

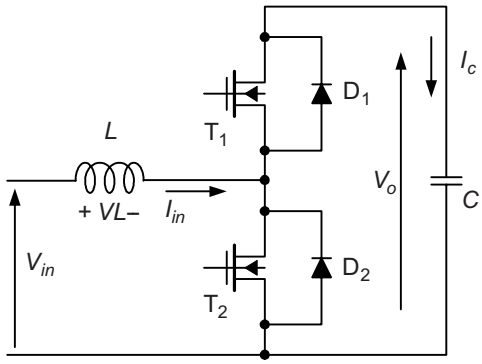


Figure 2 Active damping network

proposed for use as an active damper in [6-8] but no detailed analysis has been undertaken on the operation of the circuit in this mode.

The converter in Figure 2 would draw no average power, however, by appropriate control the converter could transiently draw or return current to the DC bus in order to damp any instabilities. One way of achieving this would be to make the converter input impedance look like an AC resistance, which would have a damping effect on the system poles and ensure that the net system resistance remains positive.

The basic operation of the circuit can be analysed as follows. It is assumed throughout that the energy storage capacitor C in the converter has a smooth DC voltage, which is greater than the DC bus voltage V_{in}. The transistors, T_1 and T_2 are operated in anti-phase with a variable duty-ratio, the duty-ratio of T_2 being D. The converter then has two modes of operation depending upon the direction of the converter inductor current I_{in}.

When I_{in} is positive, the circuit operates like a boost converter, the inductor current is switched between T_2 and D_1, and energy is delivered to the capacitor. As T_2 turns off, the inductor current flows through D_1 during the period of dead time. As soon as the dead time ends, the current is diverted from D_1 to T_1. Sketched waveforms for this mode of operation are shown in Figure 3(a). When I_{in} is negative, the circuit operates as a buck converter, taking energy from the capacitor and returning it to the DC bus. Device T_1 and D_2 are then carrying the inductor current. As T_1 turns off, the current is diverted from D_2 to T_2. The waveforms are shown in Figure 3(b).

If the average inductor current is zero, that is the triangular component of the inductor current is positioned symmetrically about the zero axis, there will be no net energy transfer between the converter and the DC system.

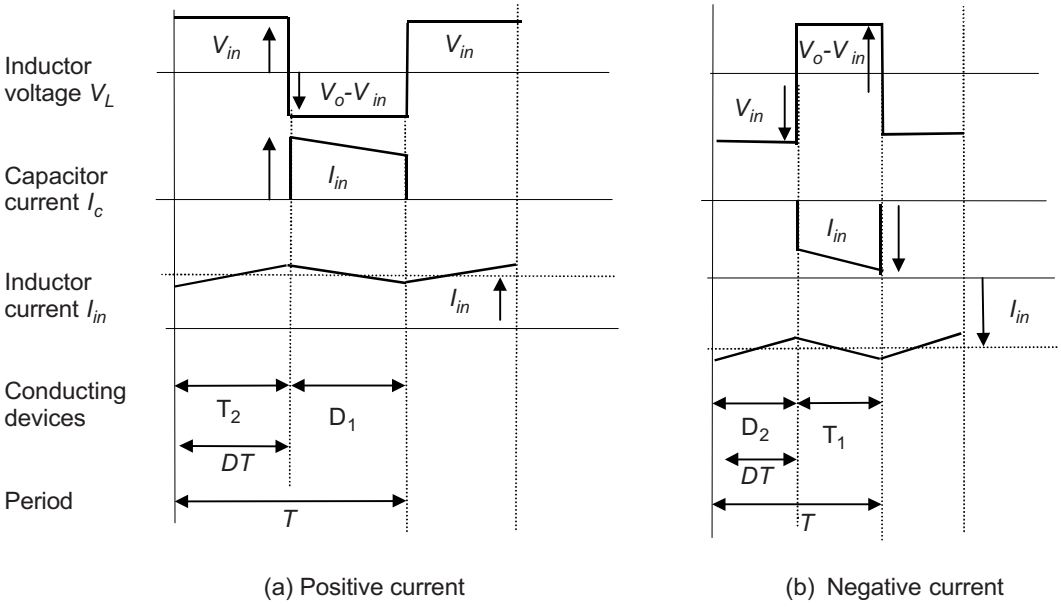


Figure 3 Idealised circuit waveforms

3.0 SYSTEM PARAMETERS

In order to examine the dynamic characteristics of the converter and the performance of the controller in a consistent way, a fixed set of typical system parameters is used throughout. The DC supply voltage, V_{in} is assumed to be 270 V, the converter output voltage, V_o is assumed to have a nominal value of 400 V and the transistor switching frequency was taken to be 20 kHz. The filter inductor value L was chosen to be 1 mH giving a peak inductor ripple current of around 2.5 A. The value of the inductor is also important in determining the maximum rate of change of input current I_{in} under transient conditions. The value of the output filter capacitor C must be chosen to ensure that the system has sufficient energy storage capacity. For example, assuming that the converter may be required during a transient to provide approximately 300 J of energy into the DC system, for example, a 30 A current pulse for 37 ms, and assuming the capacitor is initially charged to the nominal value of 400 V, then the capacitor value is chosen to ensure that the converter output voltage does not fall below the level for proper circuit operation. Considering the capacitor energy:

$\frac{1}{2}C\left[V_{o\,initial}{}^2 - V_{o\,final}{}^2\right] = 300$ J, and for normal operation of the converter

$$V_{o\,final} > \frac{V_{in}}{1-D_{min}} = \frac{270}{1-0.1} = 300 \text{ V}$$

The required capacitor value is therefore, calculated to be $C = 8.6$ mF. A value of 1 mF is used in this paper.

4.0 AVERAGED AND SMALL-SIGNAL LINEARISED MODELING

The technique of averaging is commonly used in power electronics in order to examine the dynamic behaviour of a converter. The actual variables are replaced by local average variables which are assumed to be constant across a switching cycle. In this way, a single equation is formed to represent the low frequency evolution of the variables, replacing the separate equations which describe the individual switched configurations of the converter. The averaged equations frequently contain products of system variables, that is they are non-linear, and in order to derive linear transfer functions for the system, small-signal linearisation techniques are employed. This procedure is followed here.

For the averaging process, the notation of a bar over a variable is used to show the local averaged value. The general equations for the local average inductor voltage and capacitor current over a switching period T are given as:

$$\overline{V}_L = \frac{1}{T}\int_0^T v_L dt \tag{1}$$

$$\overline{I}_c = \frac{1}{T}\int_0^T i_c dt \tag{2}$$

For an inductor, $v = L\,{}^{di}\!/_{dt}$, and for a capacitor, $i = C\,{}^{dv}\!/_{dt}$. Therefore, the rates of change of average inductor current and average capacitor voltage are given by Equations (3) and (4) respectively.

$$\frac{d\overline{I}_{in}}{dt} = \frac{\overline{V}_L}{L} \quad \text{or} \quad \dot{\overline{I}}_{in} = \frac{\overline{V}_L}{L} \tag{3}$$

$$\frac{d\overline{V}_o}{dt} = \frac{\overline{I}_c}{C} \quad \text{or} \quad \dot{\overline{V}}_o = \frac{\overline{I}_c}{C} \tag{4}$$

The analysis can be performed by referring to Figure 3(a). The average value of the inductor voltage is given by:

$$\overline{V}_L = \frac{1}{T}\left(\overline{V}_{in}DT - \left(\overline{V}_o - \overline{V}_{in}\right)(1-D)T\right) = \overline{V}_{in}D - \left(\overline{V}_o - \overline{V}_{in}\right)(1-D)$$
$$= \overline{V}_{in} - \overline{V}_o(1-D) \tag{5}$$

$$\therefore \dot{\overline{I}}_{in} = \frac{\overline{V}_{in} - \overline{V}_o(1-D)}{L} \tag{6}$$

Similarly, the average capacitor voltage is given by:

$$\bar{I}_c = \frac{1}{T}\left[\bar{I}_{in}(1-D)T\right] = \bar{I}_{in}(1-D) \tag{7}$$

$$\therefore \dot{\bar{V}}_o = \frac{\bar{I}_{in}(1-D)}{C} \tag{8}$$

Since the equations contain products of the circuit variables and the transistor duty-ratio, they must be linearised. Taking a first order approximation for the Taylor series of the variables gives:

$$\begin{aligned}\delta\dot{\bar{I}}_{in} &= \frac{\partial}{\partial\bar{V}_{in}}\left[\dot{\bar{I}}_{in}\right]\delta\bar{V}_{in} + \frac{\partial}{\partial\bar{V}_o}\left[\dot{\bar{I}}_{in}\right]\delta\bar{V}_o + \frac{\partial}{\partial D}\left[\dot{\bar{I}}_{in}\right]\delta D \\ &= \frac{1}{L}\delta\bar{V}_{\text{in}} - \frac{(1-D)\delta\bar{V}_o}{L} + \frac{\bar{V}_o\delta D}{L}\end{aligned} \tag{9}$$

where δ denotes a small change in a variable. The same process for the capacitor voltage yields:

$$\begin{aligned}\delta\dot{\bar{\mathrm{V}}}_o &= \frac{\partial}{\partial\bar{I}_{in}}\left[\dot{\bar{V}}_o\right]\delta\bar{I}_{in} + \frac{\partial}{\partial D}\left[\dot{\bar{V}}_o\right]\delta D \\ &= \frac{(1-D)}{C}\delta\bar{I}_{in} - \frac{\bar{I}_{in}\delta D}{C}\end{aligned} \tag{10}$$

Equations (9) and (10) are two simultaneous equations, with two independent variables, $\delta\dot{\bar{I}}_{in}$ and $\delta\dot{\bar{V}}_o$ and two inputs, $\delta\bar{V}_{in}$ and δD. In order to obtain transfer function relations, these two equations are converted to the Laplace domain:

$$s\delta\bar{I}_{in} = \frac{1}{L}\delta\bar{V}_{in} - \frac{(1-D)\delta\bar{V}_o}{L} + \frac{\bar{V}_o\delta D}{L} \tag{11}$$

$$s\delta\dot{\bar{V}}_o = \frac{(1-D)}{C}\delta\bar{I}_{in} - \frac{\bar{I}_{in}\delta D}{C} \tag{12}$$

where s is the Laplace operator.

Substituting Equation (12) into Equation (11) so that $\delta\bar{V}_o$ can be eliminated and the small-signal inductor current can be represented in terms of the small-signal input voltage and small-signal duty ratio.

$$\delta \bar{I}_{in}\left(s+\frac{(1-D)(1-D)}{sCL}\right)=\delta D\left(\frac{\bar{V}_o}{L}+\frac{\bar{I}_{in}(1-D)}{sCL}\right)+\frac{\delta \bar{V}_{in}}{L} \tag{13}$$

In order to obtain the transfer function between small-signal input current and small-signal duty ratio, the small change in the input voltage, $\delta \bar{V}_{in}$ can be neglected. This is possible since these are linear equations. The small-signal transfer function is shown in Equation (14).

$$\frac{\delta \bar{I}_{in}}{\delta D}=\frac{\dfrac{\bar{V}_o}{L}+\dfrac{\bar{I}_{in}(1-D)}{sCL}}{s+\dfrac{(1-D)^2}{sCL}}=\frac{s\dfrac{\bar{V}_o}{L}+\dfrac{\bar{I}_{in}(1-D)}{CL}}{s^2+\dfrac{(1-D)^2}{CL}} \tag{14}$$

Equation (14) gives the small-signal transfer function between duty-ratio and the converter input current. By referring to Equations (11) and (12), the small-signal converter model can be written in the state space matrix form as shown in Equation (15).

$$\begin{bmatrix}\delta \dot{\bar{I}}_{in}\\ \delta \dot{\bar{V}}_o\end{bmatrix}=\begin{bmatrix}0 & -\dfrac{(1-D)}{L}\\ \dfrac{(1-D)}{C} & 0\end{bmatrix}\begin{bmatrix}\delta \bar{I}_{in}\\ \delta \bar{V}_o\end{bmatrix}+\begin{bmatrix}\dfrac{\bar{V}_o}{L}\\ -\dfrac{\bar{I}_{in}}{C}\end{bmatrix}\delta D \tag{15}$$

The converter system poles are given by setting the denominator in Equation (14) to zero, Equation (16). The zeros of the transfer function are obtained by setting the numerator to zero. The result is given in Equation (17).

$$s=\pm j\frac{(1-D)}{\sqrt{LC}}=\pm j\sqrt{\frac{(1-D)^2}{LC}} \tag{16}$$

$$s=-\frac{\bar{I}_{in}(1-D)}{V_oC} \tag{17}$$

This shows that the system poles depend upon the steady-state duty-ratio, but are always located on the imaginary axis of the complex s-plane, which indicates that the system stability is in a critical condition. The zero in the system is based on the steady-state current direction. With positive steady-state current, the zero is located on the left side of the s-plane. However, if the current direction is reversed, the zero will move to the positive side of the s-plane, and with zero current, the zero is placed at the origin.

The movement of the zero with positive and negative current has limited meaning in this context since the converter cannot operate with a truly steady-state inductor

current that is non-zero. The circuit can only source or sink current for finite periods of time, limited by the circuit's finite energy storage capacity.

The right-half plane zero is thought to arise with negative current since the energy storage capacitor is being discharged; as the capacitor voltage falls the converter will be unable to sustain operation with a negative current and I_{in} would therefore, end up reversing. The right-half plane zero may be moved back towards the origin by choosing a larger capacitor value or by increasing V_o, that is increasing the energy stored in capacitor C.

By using both Equations (11) and (12), a block diagram model of the small-signal equations may be constructed relating both the control and input voltage to the inductor current and capacitor voltage, as shown in Figure 4. The block diagram was used in Simulink to examine the characteristics of the model and aid the design of the controller.

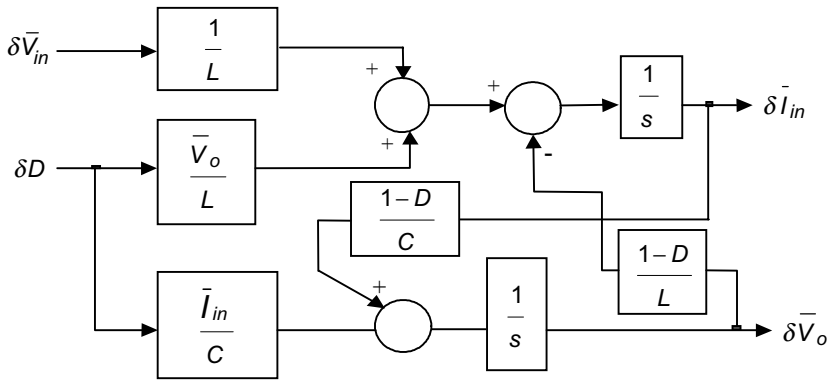


Figure 4 Block diagram of small-signal converter model

5.0 REGULATION OF CONVERTER INPUT CURRENT

In order to force the converter input current I_{in} to follow a command signal, a feedback loop is added around the system as shown in Figure 5. I_{in} is compared with the command or reference signal I_{inref}, the error is then passed through an integral controller having a compensator zero and gain K_a to form the duty-ratio signal for the converter. Using Equation (14), the open loop transfer function of the system is given by:

$$\frac{\delta\bar{I}_{in}}{\delta I_{inref}} = \frac{\left(s\frac{\bar{V}_o}{L} + \frac{\bar{I}_{in}(1-D)}{CL}\right)\left(\frac{s+z}{s}\right)K_a}{s^2 + \frac{(1-D)^2}{CL}} \tag{18}$$

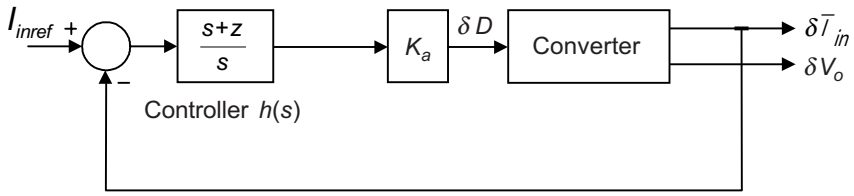


Figure 5 Closed-loop system with current controller, h(s)

where z and K_a are the compensator zero and forward gain of the current controller respectively.

The closed loop transfer function of the system is given by Equation (19):

$$\frac{\delta \bar{I}_{in}}{\delta I_{inref}} = \frac{\left(s\frac{\bar{V}_o}{L} + \frac{\bar{I}_{in}(1-D)}{CL}\right)(s+z)K_a}{s^3 + \frac{K_a V_o}{L}s^2 + \left(\frac{(1-D)^2 + I_{in}(1-D)K_a}{CL} + \frac{zK_a V_o}{L}\right)s + \frac{zK_a I_{in}(1-D)}{CL}} \tag{19}$$

To plot the root locus of the closed loop system, we equate the characteristic equation of Equation (19) to zero and rearrange to give:

$$-\frac{1}{K_a} = \frac{s^2\frac{V_o}{L} + s\left(\frac{I_{in}(1-D)}{CL} + \frac{zV_o}{L}\right) + \left(\frac{zI_{in}(1-D)}{CL}\right)}{s^3 + s\frac{(1-D)^2}{CL}} \tag{20}$$

Figures 6 to 7 show the root locus of the system poles as the control gain varies from zero to infinity. The locus in Figure 6(a) shows two positive values of I_{in}, whilst two negative values are shown in Figure 6(b). Then, Figures 7 and 8 show the effects of different steady state duty-ratio and zero position on the system poles. The following parameters are used in all the plots: z =1000 rads^{-1}; L = 1 mH, C = 1 mF, V_o = 400 V, I_{in} = ± 3 A and ± 30 A; D = 0.325.

The plots in Figure 6(a) and (b) show that there are three poles and two zeros in the system. The poles have the same movement patterns with different current levels. The complex poles begin at the imaginary axis and move to the left-hand side of the s-plane, one towards the zero and the other towards minus infinity on the real axis. However, the pole at the origin moves with different directions, depending upon the current. For the positive current, it moves to the left towards the zero, moving further to the left with higher currents. For the negative current, it moves to the right towards the zero.

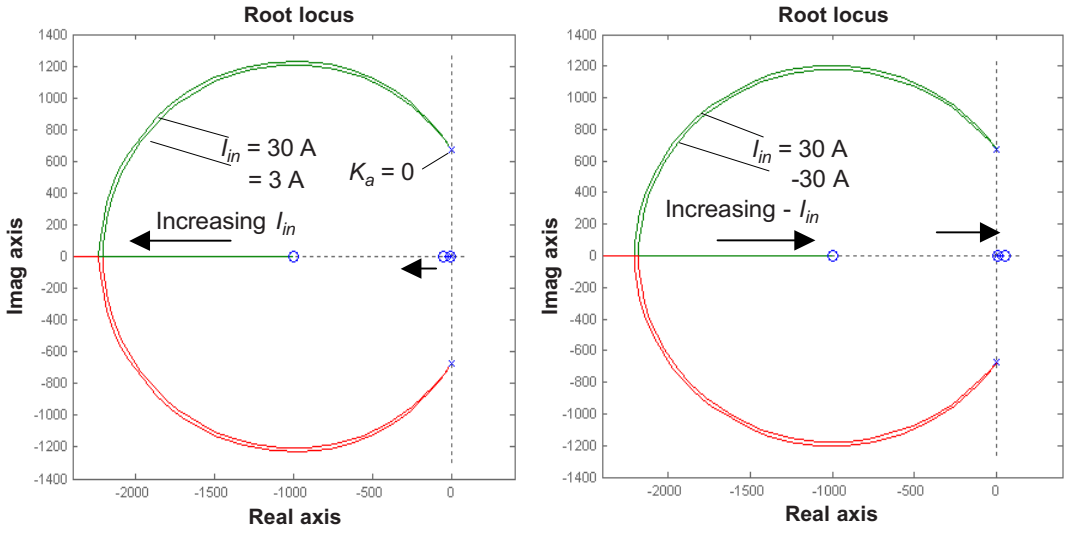


Figure 6 Pole locus for two values of current

Figure 7 shows the effect of different values of duty-ratio on the pole positions by plotting Equation (20) for a range of values of D. The steady-state input current is kept constant at +30 A throughout. As D is increased, the radius of the circular pole locus is seen to reduce. The higher the duty-ratio, the lower the pole natural frequency. In addition, the higher the duty-ratio, the closer the real pole is to the origin, which may result in a longer time constant in the transient response.

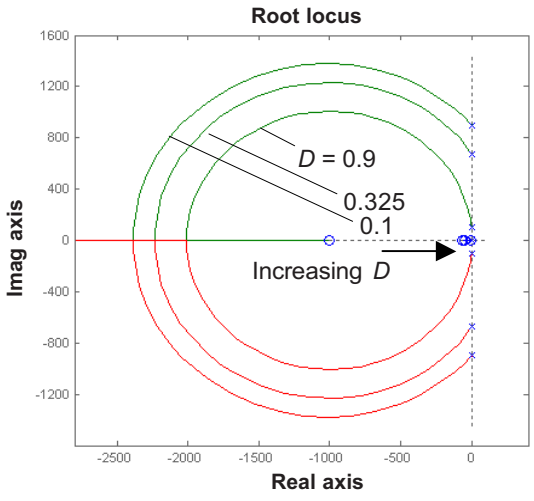


Figure 7 Pole locus for three values of D

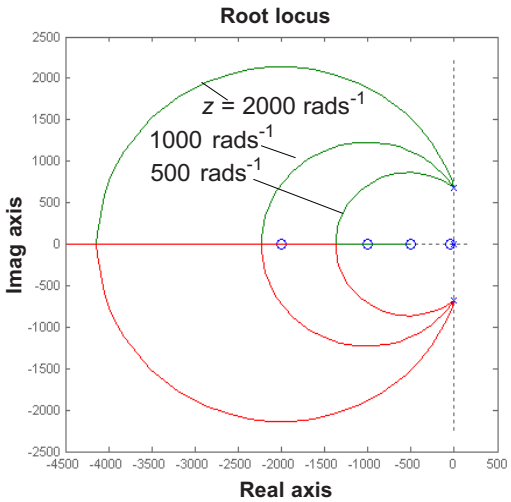


Figure 8 Pole locus for three values of the compensator zero

The plot in Figure 8 shows the pole movement as gain K_a varies from zero to infinity for different values of compensator zero, the steady-state input current is again kept constant at +30 A. Figure 8 indicates that the larger zero results in a larger radius pole locus. As seen above, the poles begin at the imaginary axis and move towards the left-hand side of the s-plane for positive current.

The choice of the zero position is to control the transient response of the system. For a small zero value, the system closed loop poles are positioned near to the origin, which results in slow dynamics in the system. Too high a value for the zero results in the complex pole locus remaining close to the imaginary axis and a very high value of K_a is required to move the poles well into the left-half plane. An intermediate value for the zero is therefore, most desirable.

6.0 DESIGN OF THE CONTROL LOOP PARAMETERS

The design of the control loop parameter is undertaken in the frequency domain, and bode plots are used throughout the design process. To illustrate the design process, the bandwidth of the control loop, or the unity gain frequency of the loop, is chosen to be 4.5 kHz (28 krads^{-1}). Over this frequency range, the current control loop will ensure that the converter input current follows the demand signal closely. Based on this bandwidth, the switching frequency is calculated. The normal design requirement is that the switching frequency is four times bigger than the bandwidth to prevent switching related instabilities or jitter in the control loop. Therefore, the switching frequency is chosen to be 20 kHz.

The value of the zero is chosen assuming the following parameters and operating conditions: L = 1 mH, C = 1 mF, V_o = 400 V, I_{in} = 30 A; D = 0.325. Using Equations (16) and (17), the converter system poles and zero are located at ± 675 rads^{-1} and -50.63 rads^{-1} respectively. To achieve a phase margin of approximately 90°, the compensator zero must be placed at least one decade below the cross-over frequency, so a value of 1000 rads^{-1} was chosen. A lower value than this would be undesirable since the closed-loop poles would remain close to the origin, producing a slow time constant. In order to achieve a bandwidth of 4.5 kHz with a phase margin of 90°, the forward gain K_a must be chosen to be 0.07.

Figure 9 shows the MATLAB Simulink block diagram for the open loop system. It shows the controller $h(s)$ in series with a forward gain K_a, connected to the DC-DC converter, which is modelled by state space matrices. The matrices are taken from Equation (15) and shown here in Equation (21). The controller transfer function is given in Equation (22). There are two output ports, the inductor current I_{in} and capacitor voltage V_o. However, the relationship of I_{in}/I_{inref} is of particular interest.

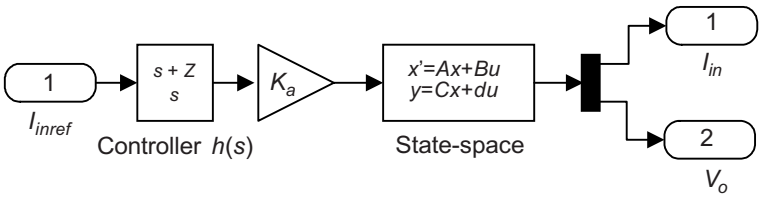


Figure 9 MATLAB Simulink open loop system

$$[A]=\begin{bmatrix} 0 & -\dfrac{1-D}{L} \\ \dfrac{1-D}{C} & 0 \end{bmatrix};\quad [B]=\begin{bmatrix} \dfrac{\overline{V}_o}{L} \\ -\dfrac{\overline{I}_{in}}{C} \end{bmatrix};\quad [C]=\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix};\quad [D]=\begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{21}$$

$$h_c(s)=\frac{(s+1000)(0.07)}{s} \tag{22}$$

The open loop response of I_{in}/I_{inref} is shown in Figure 10. The parameters used are: I_{in} = 30 A; C = 1 mF; L = 1 mH; D = 0.325; V_o = 400 V, K_a = 0.07; z = 1000 rads^{-1}. It is observed that the crossover frequency is at 28 krads^{-1} or 4.5 kHz and the phase margin is at 90° as required. The magnitude peak in the plot is due to the undamped poles in the system. The cross-over frequency is insensitive to the variations in the duty-ratio

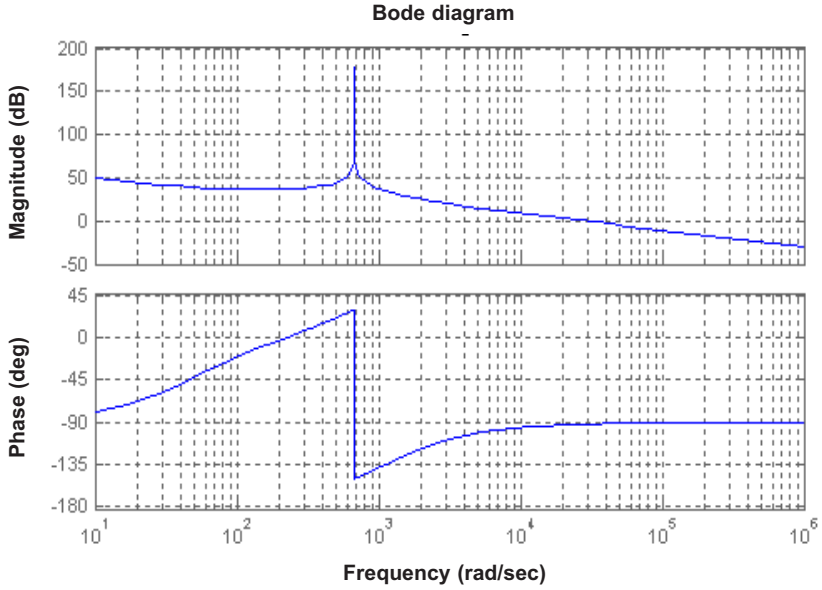


Figure 10 Open loop I_{in}/I_{inref} frequency response plot

and average input current I_{in} as can be seen by considering the high frequency asymptote of the converter $\delta I_{in}/\delta D$ transfer function, Equation (14). Since the converter zero is always positioned close to the origin, then above the complex pole frequency the $\delta \bar{I}_{in}/\delta D$ transfer function may be approximated as: $\delta \bar{I}_{in}/\delta D = V_o/sL$.

The high frequency asymptote of the controller $h(s)$ is K_a, therefore, replacing s with $j\omega$, and equating the magnitude to unity gives the cross-over frequency ω_{co} as:

$$\omega_{co} = \frac{K_a V_o}{L}$$

This approximation is valid providing that the converter complex pole frequency remains well-below the cross-over frequency. The complex pole frequency will be at its maximum when D is minimum, in theory this is zero, but practically will be limited to a value of 0.1 say. Assuming $D = 0$, the complex pole frequency is 1000 rads^{-1}, well below the cross-over frequency in this case.

The closed-loop MATLAB Simulink system connection is shown in Figure 11, and the closed loop frequency response plot of $\delta I_{in}/\delta I_{inref}$ is shown in Figure 12 using the same parameters and operating conditions as before; $L = 1$ mH, $C = 1$ mF, $D = 0.325$, $I_{in} = 30$ A, $z = 1000$ rads^{-1} and $V_o = 400$ V. From the plot, it is clear that the crossover frequency is about 28 krads^{-1}.

As a comparison, Table 1 shows the results of the closed-loop system in Figure 11 over a range of different operating conditions, with both directions of current and two extreme conditions of duty-ratio. The other parameters are as before.

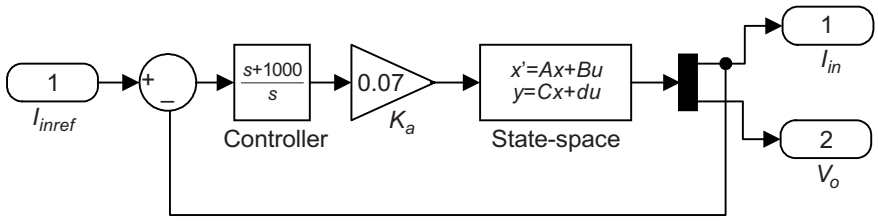


Figure 11 MATLAB Simulink closed loop system

Table 1 Closed loop system performance for a wide range of conditions

Current, I_{in}	30 A	30 A	3 A	3 A	–30 A	–30 A
Duty ratio, D	0.1	0.9	0.1	0.9	0.1	0.9
Cross over freq (krad^{s-1}), ω	28	28	28	28	28	28
System damping, ς	2.6312	2.6448	2.6375	2.6452	2.6445	2.6467
First pole (rad^{s-1})	–2700	–26969	–26937	–26962	–27025	–26969
Second pole (rad^{s-1})	–1065	–1039	–1069	–1039	–1042	–1038
Third pole (rad^{s-1})	–66	–7	–7	–1	66	7

The results confirm that the system bandwidth is not affected by the different operating conditions. The system is over-damped since all poles are on the real axis. It is noticed that with higher duty ratio, the real pole moves closer to the origin, resulting in the system having a slower dynamic response.

It is also noticed that the negative input current places one of the poles in the right-half side of the complex plane, which suggests that the system is unstable. This arises due to the movement of the converter zero into the right half plane with negative converter input current. As noted before, this is attributed to the finite energy storage capacity of the circuit. The positive real axis pole implies an exponential growth or divergence in the system behaviour, and this is thought to be due to the limited energy storage in the capacitor. As the pole is very close to the origin, the exponential growth will be very slow and this is not thought to be a problem since the converter will only operate in this condition for short periods of time. This conclusion is confirmed by the simulation results.

7.0 DESIGN OF THE CONVERTER OUTPUT VOLTAGE CONTROL LOOP AND INTEGRATOR WIND UP PHENOMENA

In practice the unloaded, bi-directional DC-DC converter also requires a voltage loop to ensure that the converter output voltage returns to its original value after a transient period. For example in an active damping system, during a transient period, there is a transfer of energy to/from the active damping device, the capacitor voltage will vary and then slowly return to the nominal value due to the action of the voltage controller loop. This is achieved by the output of the voltage controller forming an additional current reference signal to the current controller. To ensure there is no significant interference between this loop and the current control loop, a much lower speed and lower cross-over frequency are required for the voltage control loop. From the closed loop transfer function plot of $\delta I_{in}/\delta I_{inref}$ in Figure 12, the transfer function of the converter current control loop is approximately unity from low frequency up to its cross-over frequency, ω_{co}. The average capacitor current of Equation (7) is restated here for convenience $\overline{I}_c = \overline{I}_{in}(1-D)$. Consequently in Laplace form, the capacitor voltage is given by $\overline{V}_c = \overline{I}_c / sC$. The transfer function between the output voltage and reference current can be therefore shown as:

$$\frac{\overline{V}_o}{I_{inref}} = \frac{\overline{V}_c}{I_{inref}} = \frac{1-D}{sC} \tag{23}$$

Since the $\overline{V}_o / I_{inref}$ transfer function has an integral characteristic, then a zero following error between V_o and V_{oref} may be achieved in the steady state by simply using a proportional controller with gain K_v, Figure 13.

From Figure 13, the loop transfer function is given by $(1-D)/sC \times K_v$. At the cross-over frequency, the magnitude of the loop transfer function is unity, that is

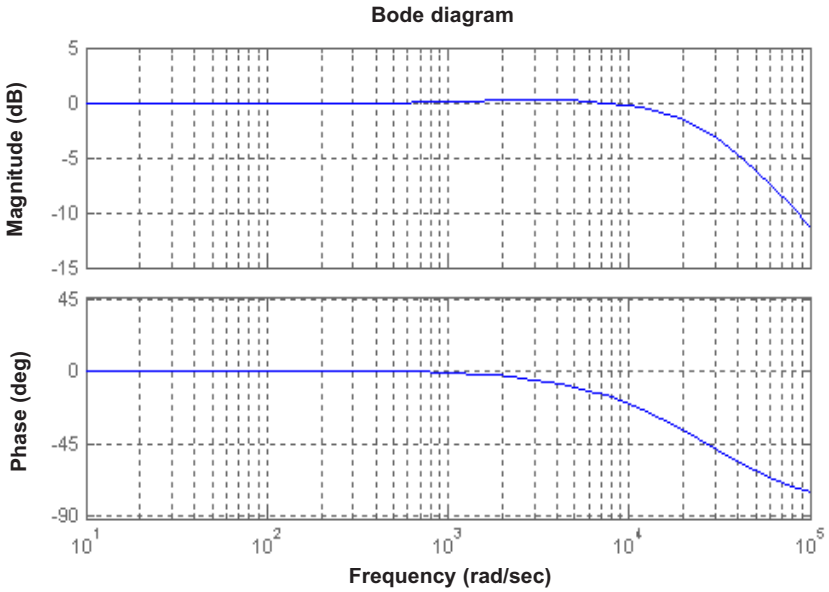


Figure 12 Closed-loop system response

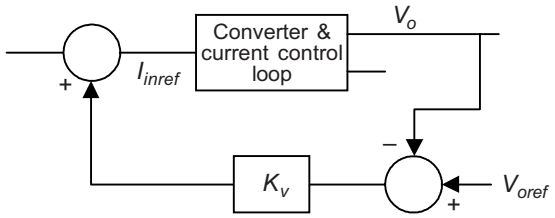


Figure 13 Block diagram of current and voltage control loop

$1 = (1-D)/\omega_{vo}C \times K_v$. This equation indicates that the cross-over frequency of the voltage control loop is proportional to the voltage controller gain for a fixed value of D. To ensure that the voltage control loop does not interfere with the current loop, w_{vo} must be chosen to be very much less than w_{co}. A very conservative choice of w_{vo} is to make it four orders of magnitude below w_{co}, giving a value of 3 rads^{-1}. Assuming C = 200 mF and D = 0.5, the K_v is calculated as 0.0012.

Integrator wind up is a common problem in a system which includes integral control and a saturation function. Here, the saturation arises due to the pwm modulator; if the modulator input falls outside the limits of 0 and 1, no further change occurs in the transistor switching pattern. Consider a large transient in the system, a high error signal results in the integrator output rising to the maximum limit of the modulator range. The integrator output continues to rise above this level even though there is no

further change in duty-ratio. When the error signal reverses, there is then a significant delay while the integrator output falls before the transistor duty-ratio reduces from its maximum. This delay can result in uncontrolled overshoots and oscillations in the output. To prevent this, the integrator must stop integrating when its output exceeds the limits of the modulator.

Figure 14 shows a Simulink solution to this problem in the current controller. The controller transfer function was designed as in Equation (22). Here, the original controller transfer function is rearranged to ease the circuit implementation in the simulation. Either of the two conditions have to be fulfilled to stop the integrator: firstly, when the integrator output is bigger than 0.9 and the integrator input is positive ($[V_d > 0.9]$AND$[V_{error} > 0]$ and secondly, when the integrator output signal is less than 0.1 and the integrator input is less than zero($[V_d < 0.1]$AND$[V_{error} < 0]$). When either condition is detected, the integrator input is switched to ground to prevent any further change in output until the error signal reverses. Both input and output signals of the current controller need to be sensed and the logic manipulation is undertaken in the switch command box.

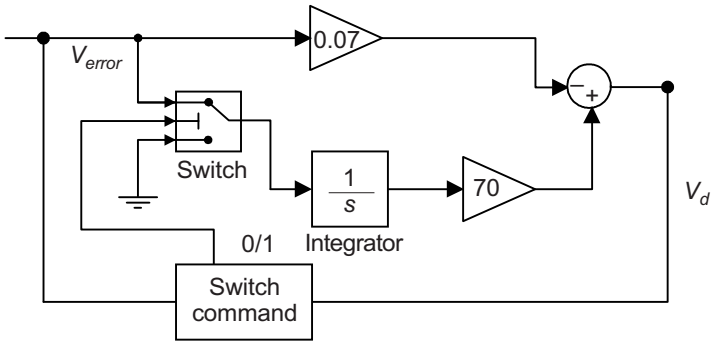


Figure 14 Current controller with integrator wind up solver

8.0 SIMULINK SIMULATION RESULTS

The closed loop converter circuit in Figure 15 has been simulated using Simulink, with the help of the integrator anti-wind block in the current controller. Once the simulation had settled to a steady-state with 400 V at the output and 0 A in the inductor, a series of positive and negative steps were applied at the current reference input to demonstrate the system operation. The parameters used are as before, section V, with $K_a = 0.07$, $z = 1000$ rads^{-1}, $L = 1$mH, $C = 1$mF.

The results of the inductor current I_{in} are shown in Figure 16(a) and (b) where a short positive current pulse is demanded at 15 s and a negative pulse at 25 s, both current pulses have a duration of 4 ms. Figure 17 shows the plot of the converter capacitor voltage V_o. The plots indicate that the system behaves satisfactorily, that is

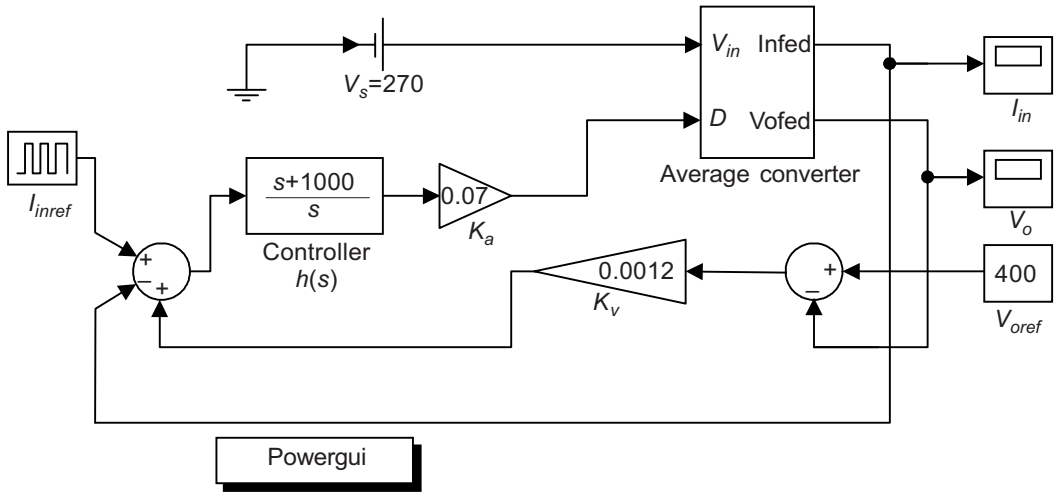
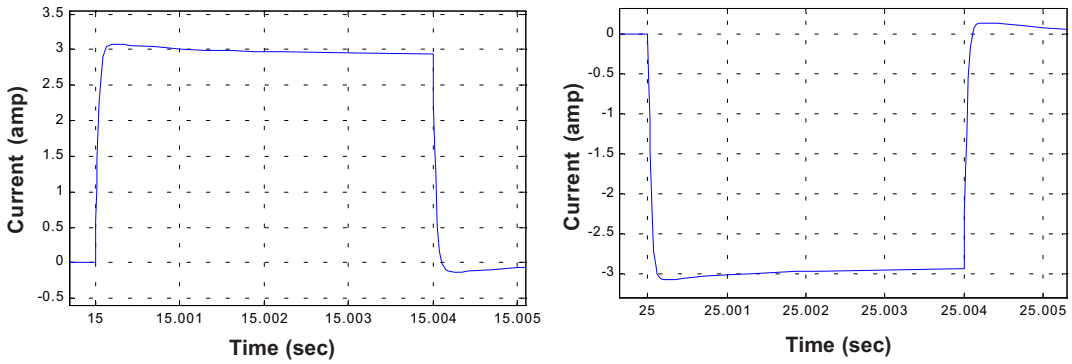


Figure 15 Block diagram for the system simulation

the actual current follows almost exactly the demand current, there is virtually no overshoot and the rise time is approximately 0.2 ms. This is consistent with the high frequency pole position listed in Table 1.

A small droop is evident in the inductor current pulses and is due to the voltage controller. The positive inductor current causes the capacitor voltage to rise as shown in Figure 16 and the voltage controller acts to reduce I_{in} resulting in a droop in Figure 15. Figure 16 shows that the capacitor voltage gradually falls back to 400 V in a time of 8 s.

The plot in Figure 16(a) shows that the positive current step at 15 s causes the capacitor voltage to rise up rapidly because the capacitor is charged by the current. The final



(a) Positive current (b) Negative current

Figure 16 Simulation result of converter inductor current, I_{in}

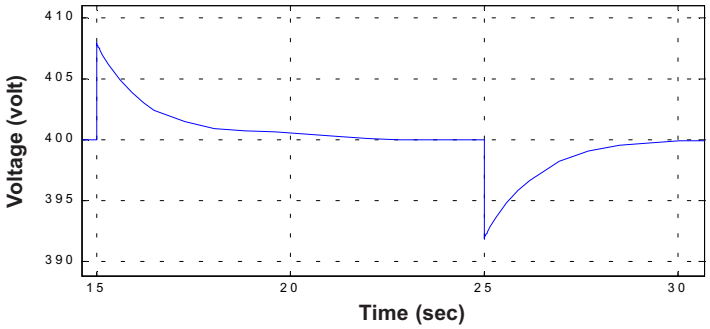


Figure 17 Simulation result of converter capacitor voltage, V_o

value of capacitor voltage depends on the magnitude of current, the capacitor value, the period of the current pulse, and its initial condition voltage. Here, the peak voltage reached is about 408 V.

Likewise, the negative step imposed at 25 s causes the capacitor voltage level to go down to 392 V. This implies that the capacitor voltage discharges its energy to the DC bus. Soon after the negative step is applied, the voltage controller pulls the voltage back to its original value, by causing a positive current to flow into the capacitor.

9.0 CONCLUSION

The analysis, theoretical design and simulation of the unloaded bi-directional DC-DC converter were examined extensively. The analyses using averaged and small-signal techniques were discussed in detail. It was shown that the converter input current could be satisfactorily controlled by the use of a single feedback loop of inductor current. An additional slow loop was required to ensure that the capacitor voltage remained within acceptable limits. The results were verified by MATLAB Simulink simulation.

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