Multilevel inverter topologies

Abstract

Multilevel voltage source inverter (MVSI) is very attractive in high voltage and high power applications such as adjustable speed drives and electric utility applications. The development of MVSI began in the early 1980's when Nabae et al. [1] proposed a neutral point clamped (NPC) PWM inverter. Since then several multilevel topologies have evolved. The general structure of the MVSI is to synthesize a sinusoidal voltage out of several levels of dc voltages [2]. The so-called multilevel inverter starts from three levels. The MVSI can therefore be described as a voltage synthesizer. . There are several advantages offered by the MVSI. In Voltage Source Inverter (VSI), the maximum voltage level output is determined by the voltage blocking capability of each device. By using a multilevel structure, the stress on each device can be reduced in proportional to the number of levels, thus the inverter can handle higher voltages [3]. As a result, an expensive and bulky step-up transformer can be avoided in various applications. In another perspective, the harmonic in the output waveform can be reduced without increasing switching frequency or decreasing the inverter power output [4]. As the number of voltage levels reach infinity, harmonic content will be low enough to avoid the need of filters [5]. The number of the achievable voltage levels, however is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. In motor application, high dV/dt in power supply generates high stress on motor windings and requires additional motor insulation. Furthermore, high dV/dt of semiconductor devices increases the electromagnetic interference (EMI), common-mode voltage and possibility of failure on motor. With several levels in output waveform constructed by multilevel inverter, the switching dV/dt stresses are reduced [4].