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Analytical modeling of high performance single-walled carbon nanotube field-effect-transistor

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ABSTRACT

We present a novel analytical modeling of a zigzag single-walled semiconducting carbon nanotube field effect transistor (CNFET) by incorporating quasi-one-dimensional (Q1D) top-of-a-potential barrier approach. By implementing multimode carrier transport, we explore and compare the performance of a low- (360 cm^2/Vs) and high-mobility (7200 cm^2/Vs) CNFET model with experimental data from nanotube and 45 nm MOSFET, respectively, as well as existing compact models. Mobility and carrier concentration models are also developed to obtain a good matching with physical data. For a high mobility CNFET, we found that a maximum of 120 μA is obtained. In addition to this, a CNT-based inverter is also developed by constructing n-type and p-type CNFET in ORCAD's analog behavioral model (ABM). A gain of as high as 5.2 is forecasted for an inverter of 80 nm CNFET.

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1. Introduction

It is well known that when channel length of a conventional MOSFET is scaled down the short channel effect arises and become more pronounced in sub-100 nm channel lengths. It is therefore critical to develop a new generation of nanoscale transistors that can uphold a performance as good as or even better than that of state-of-the-art MOSFETs. Carbon nanotube (CNT) is no doubt a good candidate for sustaining the progress in nanotechnology as it has excellent electrical and transport properties over silicon. For instance, its quasi-one-dimensional (Q1D) character with near ballistic transport allows the carriers to travel swiftly in only one particular direction [1]. Experiments have shown that this Q1D character of CNT transistors results in superior performance with enhanced mobility [2], fairly good transconductance and high current on–off ratio [3]. Rapid progress on CNT transistor development also enables the possibility to fabricate a logic gate made of CNT (carbon based inverter) [4].

In a quantum wire, saturation velocity is in fact an intrinsic velocity that relies on temperature in a nondegenerate regime whereas it is a function of carrier concentration in the degenerate regime [5]. The focus of the present work is on development of an analytical model of short channel CNFET, where the limitations due to the saturation velocity are being evaluated and utilized. This analytical model in low and high mobility CNTs is evaluated in MATLAB and ORCAD's PSPICE.

2. Quasi-one-dimensional (Q1D) model

CNT subband structure plays a predominant role in predicting transport properties in a Q1D nanoscale device. The carriers in Q1D device are confined in two directions, in our case *y*- and *z*-direction, to form a quantum wire; while they are free to move in *x*-direction (quasi-free direction along the length of the nanotube). In this case, L_x maintains its bulky character with $L_x \gg \lambda_D$ and therefore its analog-type continuous characteristic in the *x*-direction is expressed as

$$E_k = E_{c1} + \frac{\hbar^2 k_x^2}{2m^*} \tag{1}$$

where E_{c1} is the conduction band edge lifted from its bulk value E_{c0} by the zero-point quantum-confined energy in *y*–*z* plane. The carrier concentration depends on the probability distribution

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function $f(E)$ and density of quantum states (DOS) $g_{dse}(E)$ [6,7]. Integral of the DOS together with the Fermi function give for linear carrier concentration per unit length n_1 the expression

$$n_1 = \int_{E_c}^{E_{top}} g_{dse1}(E) f(E) dE = N_{c1} \Im_{-1/2}(\eta) \tag{2}$$

where

$$\Im_i(\eta) = \frac{1}{\Gamma(i+1)} \int_0^{\infty} \frac{x^i}{\exp(x-\eta)+1} dx \tag{3}$$

$$\eta = \frac{E_F - E_{c1}}{k_B T} \tag{4}$$

$$N_{c1} = 2(m^* k_B T / 2\pi\hbar)^{1/2} \tag{5}$$

N_{c1} is the effective density of states and $\Im_i(\eta)$ is the Fermi–Dirac (FD) integral of order i ($i = -1/2$ for Q1D nanostructure). A semiconductor degenerates when the Fermi level lies above the conduction-band edge by approximately $3k_BT$ or that much below from the valence-band edge. Similarly, when the energy level is in the forbidden band gap by $3k_BT$ below the conduction band or $3k_BT$ above the valence band, the carrier gas is nondegenerated.

The Fermi–Dirac integral of Eq. (3) when approximated in these two extremes (degenerate and nondegenerate) is given as follows:

$$\Im_i(\eta) = \exp(\eta) \quad \text{(nondegenerate)} \tag{6}$$

$$\Im_i(\eta) \approx \frac{1}{\Gamma(i+1)} \frac{\eta^{i+1}}{i+1} = \frac{\eta^{i+1}}{\Gamma(i+2)} \quad \text{(degenerate)} \tag{7}$$

Similar expressions can be developed for Q2D and bulk samples. Fig. 1 shows normalized carrier density for bulk, Q2D MOSFET and Q1D CNFET versus the level of degeneracy η. As is evident from Fig. 1, both MOSFET and CNFET normalized densities do not approximate accurately the non-degenerate limit beyond $\eta = 0$. CNFET enters the degenerate regime faster than the MOSFET as concentration increases beyond $\eta = 0$.

To accurately model a CNFET, the ultimate saturation velocity plays a key role. The velocity response to the applied electric field changes from a linear behavior in low electric field to saturated velocity in an infinite electric field. At equilibrium, the velocity vectors are randomly oriented, resulting in vector sum to zero in any direction. When an electric field is applied, the carriers in CNT channel drift and initiate a non-zero drift velocity in the direction of the applied electric field. In a low electric field the drift velocity (v_d) response to the electric field (E) is linear with mobility μ_o as the slope ($v_d = \mu_o E$). In the other extreme, particularly in nanoscale conducting channels, the electric field is necessarily high and the velocity vectors streamline in the direction of the applied electric field for holes and in the opposite direction for electrons. In this extreme, the ultimate drift velocity, known as saturation velocity, is the intrinsic velocity given by [7]

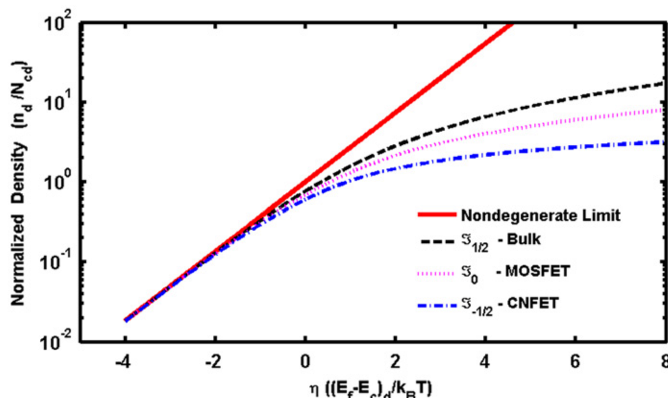

Fig. 1. Normalized carrier density for bulk, MOSFET and CNFET.

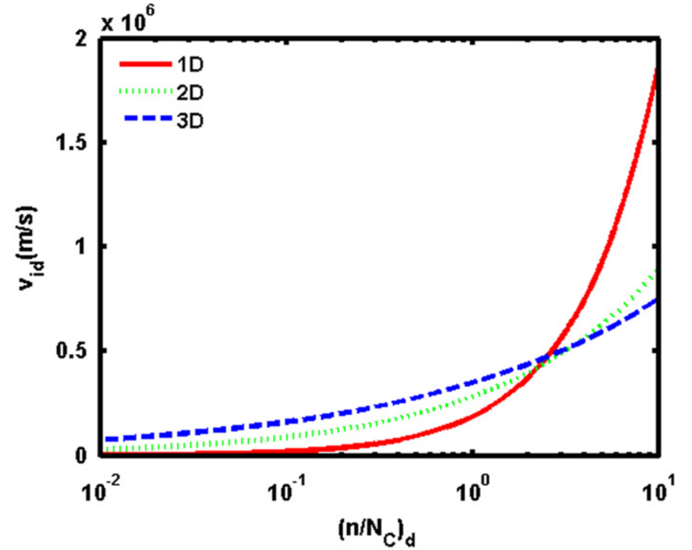

Fig. 2. Ultimate velocities in the degenerate regime for 3D, 2D and 1D structure versus normalized carrier density.

$$v_{id} = v_{satd} = v_{thd} \frac{N_{cd}}{n_d} \Im_{(d-1)/2}(\eta_d) \tag{8}$$

with

$$v_{thd} = \sqrt{\frac{2k_BT}{m^*}} \frac{\Gamma((d+1)/2)}{\Gamma(d/2)} \tag{9}$$

where d in Eqs. (8) and (9) is the dimensionality ($d = 1$ for CNFET, $d = 2$ for a MOSFET and $d = 3$ for a bulk material). Fig. 2 shows the intrinsic velocity as a function of normalized carrier concentration for all dimensionalities $d = 1$, 2 and 3. The intrinsic velocity is a function of temperature and independent of carrier concentration in the nondegenerate regime, while in the degenerate limit, the intrinsic velocity depends strongly on carrier concentration but is independent of temperature [5]. The intrinsic velocity shown in Fig. 2 is appropriate for $T = 300$ K.

A number of empirical relations to characterize the drift velocity in response to the electric field exist, the most notable one being the one given below [8]:

$$v_{dn(p)} = \frac{\mu_{on(p)} E}{\left[1 + (E/E_{cn(p)})^{\gamma_{n(p)}}\right]^{1/\gamma_{n(p)}}} \tag{10}$$

where $E_{cn(p)} = v_{satn(p)}/\mu_{on(p)}$ is the critical electric field and $\gamma_{n(p)} = 1-2.8$. The value of $\gamma_{n(p)}$ does not change the extreme behavior, but results in faster approach towards saturation as $\gamma_{n(p)}$ is increased; $\gamma_{n(p)} = 1$ is convenient for transistor modeling.

3. Modeling of CNFET

The potential at the top of the barrier versus gate voltage can be expressed as [9]

$$E_{C1} = -qV_{GS} + q^2 n_{1D}/C_e \tag{11}$$

where carrier concentration n_{1D} from Eq. (2) is assumed to be in the degenerate regime. The threshold voltage is defined as

$V_T = -E_F/q$ while the drain current I_D as a function of the gate voltage V_{GS} and drain voltage V_{DS} is given as

$$I_{DS} = n_{1D} q v_d = \sqrt{\frac{8m^* q(V_{GS}-V_T)}{\pi^2 \hbar^2 (1+C_q/C_e)}} q \frac{\mu_o}{L} \frac{V_{DS}}{1+V_{DS}/V_C} \quad (12)$$

with

$$C_e = \frac{2\pi\varepsilon}{\ln((2t_{ins}+t_{CNFET})/t_{CNFET})} \quad (13)$$

$$C_q = \frac{2q^2}{h v_F} \quad (14)$$

$$V_c = \frac{v_{sat}}{\mu_o} L \quad (15)$$

$$v_{sat} = v_{i1Deg} = \frac{\hbar}{4m^*}(n_{1D}\pi) \quad (16)$$

Here $C_e \approx 1.9752 \times 10^{-10}$ F/m is the electrostatic capacitance per unit length with $t_{ins} = t_{CNFET} = 1$ nm, $L = 80$ nm and $\varepsilon = 3.9\varepsilon_o$ for SiO_2 as an insulator. The effective mass for the 1.57 nm diameter (20, 0) CNT is $0.051m_0$.

4. Results and discussion

Fig. 3 shows a schematic diagram for the MOSFET-like 80 nm CNFET. The drain and source form ohmic contacts with semiconducting nanotube while a thin insulator SiO_2 is injected between the terminal gate and CNT channel to ease the charge controlling process. The performances of these tubes are carried out by analyzing low- and high-mobility CNFETs.

4.1. Low mobility CNFET model

The low mobility CNFET of $L = 80$ nm is chosen with a mobility $\mu_o = 360$ cm^2/Vs. The mobility in p-type conventional MOSFET is obtained by incorporating channel conductance $g_{ds} = I_{ds}/V_{ds} = 2K(V_{GS}-V_T)$ with $K = \mu C_G/2L^2$. A mobility of 395 cm^2/Vs at gate voltage bias 1 V in an experimental CNFET [3] is obtained, which compares favorably with $\mu_o = 360$ cm^2/Vs for low-mobility CNFET. These findings are consistent with those from the random network single-wall-nano-tube (SWNT) model of Snow et al. [10], who reported mobility exceeding 150 cm^2/Vs. The carrier concentration is computed to be $n_{1D} \approx 3.25 \times 10^8$ m^{-1} using Eq. (16). The saturation velocity for 1-conduction-subband transport is found to be 5.82×10^5 m s^{-1} with quantum capacitance $C_q \approx 1.3310 \times 10^{-10}$ F/m. Gate capacitance is calculated as $C_g = (C_e C_q)/(C_e + C_q) \approx 6.36$ aF. The threshold voltage and critical voltage are given as $V_T = -0.05$ Vand $V_C \approx 1.2927$ V, respectively. The highest on-current with gate voltage $V_{GS} = 1.0$ V is around 15 μA. The simulated I–V characteristics are compared with the experimental results on 80 nm high doping nanotube [11] in Fig. 4. The comparison shows that the model agrees very well with the experimental data [11]. Even with high bias voltage, CNFET does not show current saturation due to its low mobility, which enhances the critical voltage.

Fig. 5 shows the gate characteristics of the CNFET. At the power supply of $V_{DD} = V_{DS} = 0.5$ V, the on–off current ratio is found to be as high as $\approx 10^3$ even for a low mobility device. With the drain voltage $V_{DS} = 0.5$ V, the subthreshold swing (SS) is approximated at 75 mV/dec, which compares favorably well with 70 mV/dec reported in [11]. The drain-induced barrier lowering (DIBL) in low-mobility CNFET is evaluated to be 132.65 mV/V, perhaps due to threshold voltage V_T strongly dependent on V_{DS}.

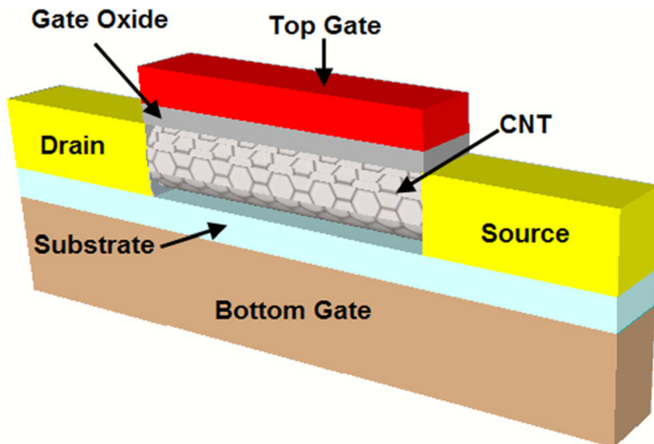

Fig. 3. Schematic diagram for CNFET with ohmic contact.

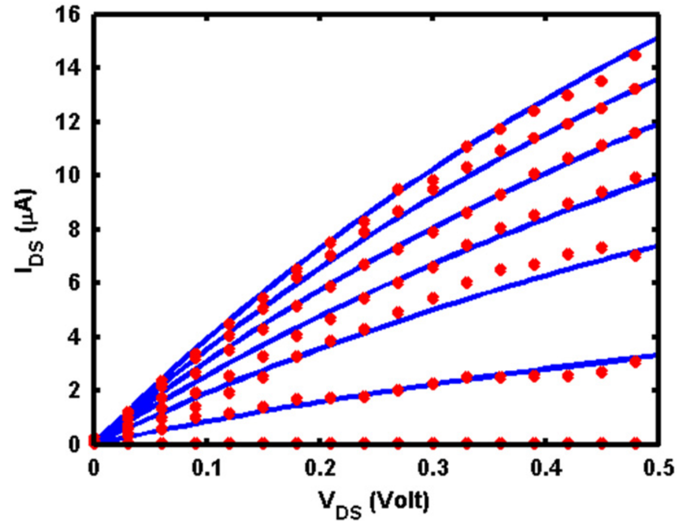

Fig. 4. Comparison of I–V_{DS} characteristic between the low mobility 80 nm CNFET (solid lines) and 80 nm experimental model [11] (dotted line). Both devices are biased with gate voltage −0.2 V till 1 V with 0.2 V step increment.

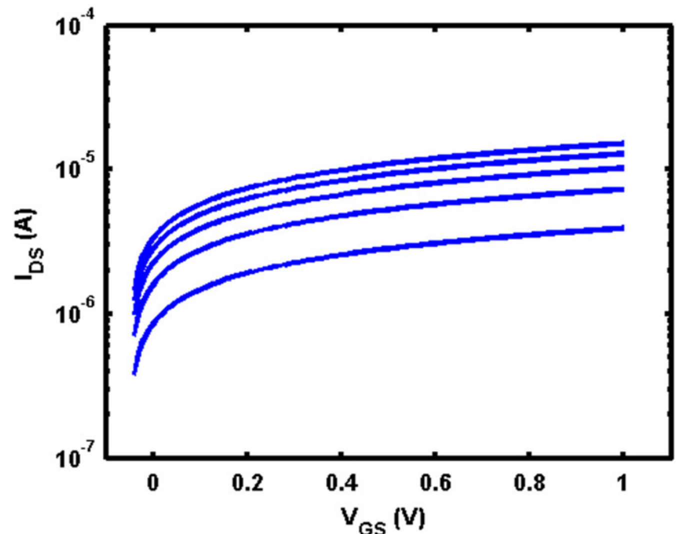

Fig. 5. I–V_{GS} graph for low mobility 80 nm CNFET device with drain voltage from 0 V at the bottom until 0.5 V at the top with 0.1 V step increment.

4.2. High mobility CNFET model

The following parameters are being used for the high mobility model: $L = 80$ nm and mobility $\mu_o = 7200$ cm^2/Vs. Previous work [2] shows that mobility in semiconducting CNT can reach as high as 79,000 cm^2/Vs in a long-channel CNT (≈ 300 μm), but degrades due to ballistic effects. The threshold voltage and critical voltage are given as $V_T = 0.32$ V and $V_C \approx 0.1780$ V, respectively. The analytical model for CNT also includes multimode transport, where higher subbands contribute to the current [12]. The Q1D saturation velocity for 3 subbands is $\approx 1.60 \times 10^6$ m s^{-1}. This brings carrier concentration to $n_{1D} \approx 8.95 \times 10^8$ m^{-1} with quantum capacitance at $C_q = 4.8331 \times 10^{-11}$ F/m and gate capacitance $C_g = 3.11$ aF. This small capacitance makes it possible for CNFET to reach terahertz frequency range. As Fig. 6 shows, the maximum current carried by all three subbands can reach 120 μA for $V_{DS} = V_{GS} = 1$ V. The multimode transport [13] is expected to boost the maximum saturation current of shorter SWNT to around 70 μA [14]. This is a significant improvement over the long-channel CNT, where current is about 20–25 μA [15,16].

The simulated *I–V* characteristic for a high mobility CNFET is evaluated against the experimental data of a 45 nm channel length n-type MOSFET (NMOS) from Taiwan Semiconductor Manufacturing Company Limited (TSMC) [17]. Since the experimental data are in A/μm, $W = 200$ nm device is simulated utilizing a 90-nm analytical MOSFET model [18,19]. The results are shown in Fig. 6.

Both devices have the same saturation current at $V_{GS} = 1$ V. MOSFET has a lower current for $V_{GS} = 0.5$–1.0 V. CNFET stands to benefit greatly with its high I_{on} current by reducing the access time in non-volatile random access memory (NRAM) [20] over silicon dynamic RAM (DRAM) [21]. MOSFET has a slight gain since its DIBL effect is at 24.3 mV/V. The DIBL for high mobility CNFET is thrice that of MOSFET at 85.86 mV/V but still within the controlled region. The SS is 67.5 mV/dec, which is slightly better compared with MOSFET with 78.3 mV/dec.

Fig. 7 shows the performance of high mobility CNFET device evaluated using the I_D–V_{GS} graph. The on–off current ratio can be at least $\approx 10^6$ with bias voltage of $V_{DD} = 1$ V as used in this model. As a result, the leakage current during the switching process is kept fairly minimal. Table 1 indicates the device specifications for both low and high mobility models. Generally, the high mobility model has better performance due to its superior on–off current ratio, high mobility and low gate capacitance (high frequency).

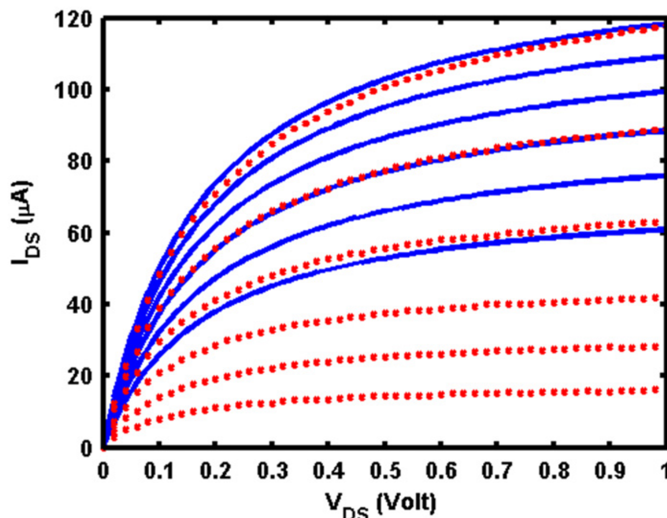

Fig. 6. Comparison of I–V_{DS} characteristic between the high mobility 80 nm n-type CNFET (solid lines) and 45 nm analytical NMOS model [17] (dotted lines). Gate voltage is applied from 0.5 to 1.0 V with 0.1 V step increment.

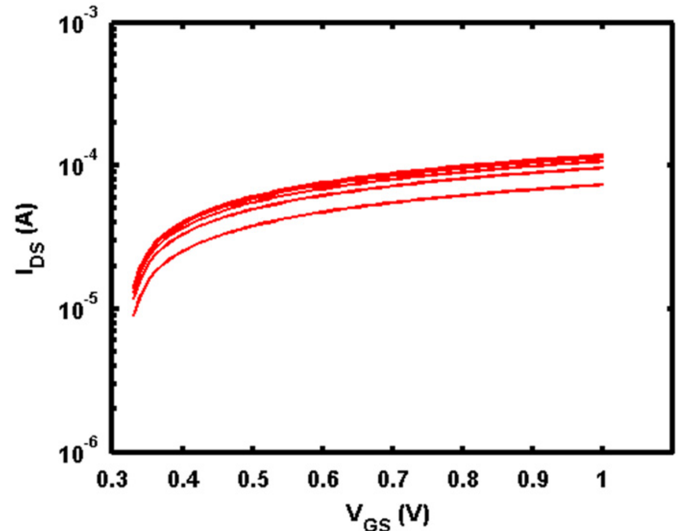

Fig. 7. I–V_{GS} graph for high mobility 80 nm CNFET device with drain voltage from 0 to 1 V (bottom to top) with 0.2 V step increment.

Table 1
Device model specification.

Parameter	Low mobility	High mobility
Chiral vector, (n, m)	(20 0)	
Tube diameter, d (nm)	1.57	
Effective mass, m^*	0.051	
Gate insulator thickness, t_{ox} (nm)	1	
Channel length, L (nm)	80	
Mobility, μ_o (cm^2/Vs)	360	7200
Carrier concentration, n (m^{-1})	3.25×10^8	8.95×10^8
Dielectric constant, ε_r	3.9	
Saturation velocity, v_{sat} (m s^{-1})	5.82×10^5	1.60×10^6
Critical voltage, V_C (V)	1.29	0.18
Gate capacitance, C_g (aF)	6.36	3.11
Conductivity parameter, K (μA/V)	17.89	174.73
DIBL (mV/V)	132.65	85.86
Subthreshold swing, SS (mV/dec)	75	67.5
On–off ratio	10^3	10^6

In addition to the performance evaluation with MOSFET, the accuracy of our n-type CNFET model with existing compact models [22,23] is assessed. Figs. 8 and 9 show a comparison of the simulated n-type CNFET with the compact models from Stanford [22] and Arizona [23], respectively. In order to have a good agreement with these existing models, the gate voltage-dependent mobility and carrier concentration have been developed and applied in the simulated CNFET. At high gate bias, our simulated models overestimate the saturation drain but give a precise prediction below $V_{GS} = 0.6$ V for both compact models. The models are able to fit the characteristics curves of Stanford (~ 1.49 nm) and Arizona model (~ 1 nm) of different diameters and with Schottky barrier.

4.3. Analog behavioral model (ABM) SPICE modeling

SPICE simulation is carried out on short channel CNFET using a set of functional ABM black-block model [24]. In this design, we used a bottom-up approach that is easily modified for small building blocks. Fig. 10 shows an ABM model of voltage-controlled current source (VCCS) n-type CNFET that has

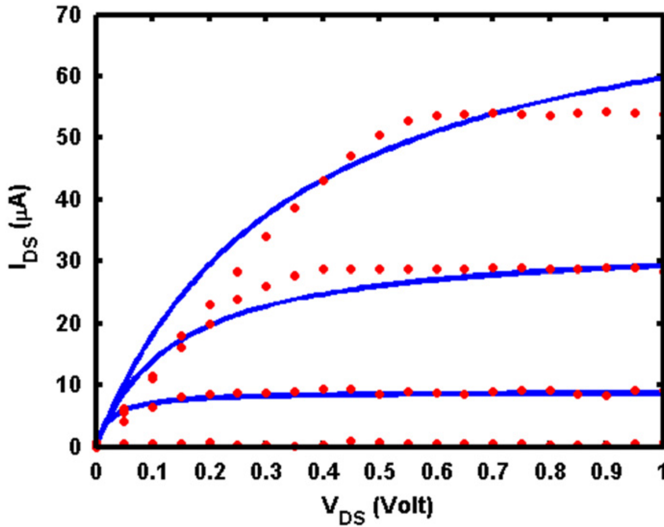

Fig. 8. I–V_{DS} characteristic of the simulated n-type CNFET (solid lines) as a comparison against the Stanford CNFET model (dotted lines) [22] with gate voltage-dependent mobility and carrier concentration. Gate voltage is applied from 0.4 V at the bottom to 1.0 V at the top with 0.2 V step increment.

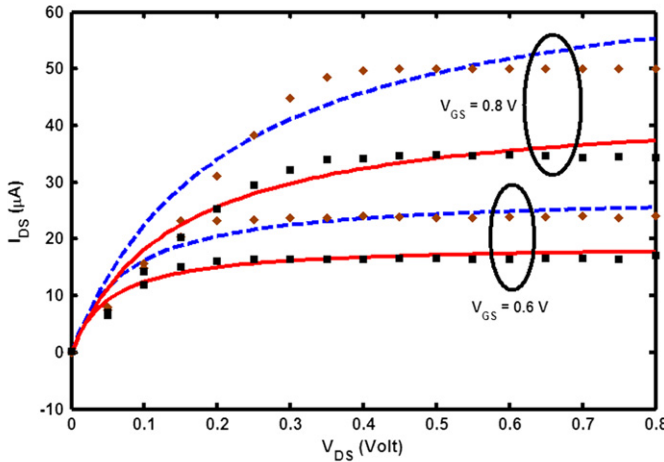

Fig. 9. The n-type CNFET model (solid and dotted lines) is simulated and compared against the MOS-CNT (filled diamond) and SB-CNT (filled boxes) [23] compact models for gate voltage 0.6 and 0.8 V.

three-voltage input and one current output similar to a conventional MOSFET equation.

By adopting pessimistic optimization [25], similar steps are taken to simulate an inverter using a p-type CNFET SPICE model. Fig. 11 shows the current–voltage characteristic of both n- and p-type CNFET. These two nanoscale devices are then biased from 0 to 1 V in the configuration depicted in Fig. 12. A characteristic of a NOT logic gate is observed when the voltage shifts to zero at high voltage and vice versa. The voltage transfer curve (VTC) of 5.2 is achieved. It is found that a complementary device such as this has been successfully fabricated and is able to provide gain higher than one [26]. For example, high performance top-gate complementary inverter has a VTC up to 3.6 [4].

5. Conclusion

The performance and electrical properties for low and high mobility 80 nm CNT models are compared, verified and found to

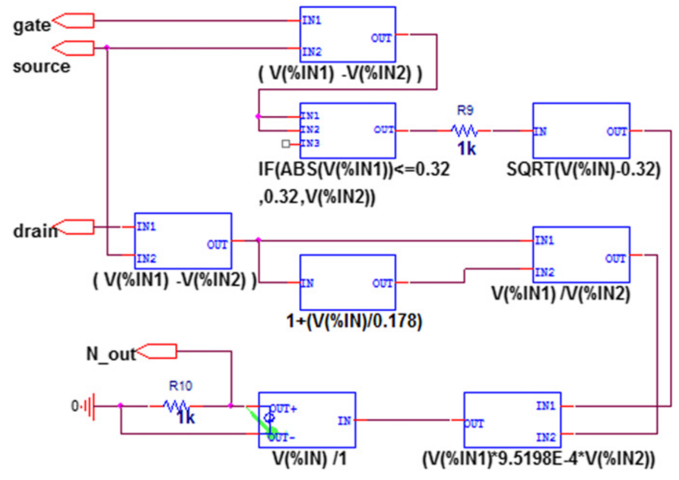

Fig. 10. ABM model of a n-type CNFET with gate, source and drain voltage as inputs and drain current as output.

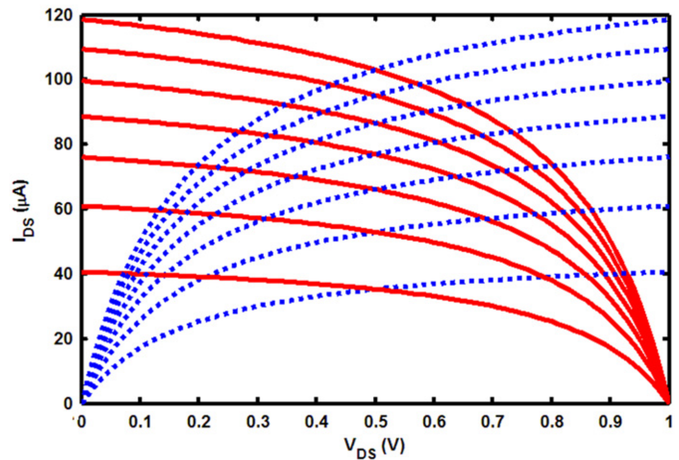

Fig. 11. Drain current versus drain voltage characteristic of 80 nm n-type (dotted lines) and p-type (solid lines) CNFET. Gate voltage is from ± 0.4 to ± 1.0 V in ± 0.1 V steps increment (bottom to top)

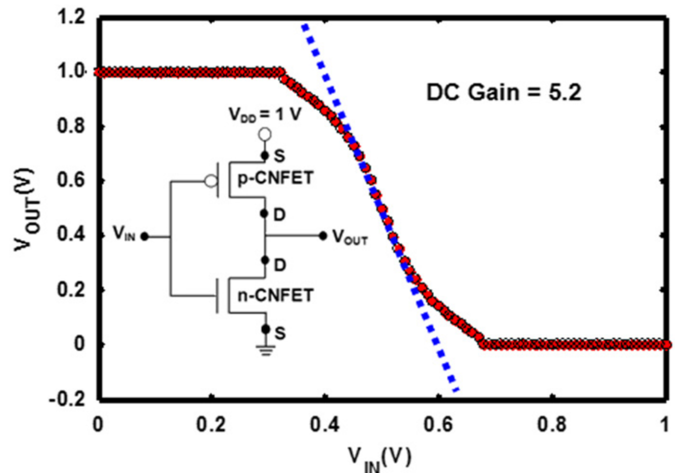

Fig. 12. Transfer characteristics of CNFET inverter (filled circles) and the corresponding dc gain (dotted lines). Inset shows a CNT inverter.

be in good agreement with experimental data. The high mobility model has mobility 20 times that of the low mobility model with carrier concentration around $\approx 10^8\,\mathrm{m}^{-1}$. Low DIBL in the high mobility model indicates that the threshold voltage is less dependent on drain bias voltage. Thus, this short channel effect can be controlled well in the high mobility model. Unlike in the low-mobility model, high DIBL exhibits a reduced threshold voltage due to the high drain bias voltage, which reduces barrier height at source end of the channel [27]. The high-mobility model has faster transient switching in between the on- and off-states compared with the low mobility model due to its steeper SS. Three times higher on–off current ratio in the high mobility model compared with the low mobility model shows the excellent electrical properties of short channels. The validity of our model in logic gate level is explored by simulating an 80 nm CNFET inverter in ORCAD ABM and revealed to have a promising high DC gain of 5.2.

Lundstrom and Guo [9] have extensively used non-equilibrium Green's function (NEGF) in calculating transport properties of CNFETs and nanoscale MOSFETs. Their formalism is inherently difficult to follow and adopt for numerical work. This work based on intrinsic velocity [1] for Q1D nanostructures affords an easy and transparent way to assess and model the performance of functional devices of all dimensionalities.

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