FPGA IMPLEMENTATION OF CPFSK MODULATION TECHNIQUES FOR HF DATA COMMUNICATION

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Abstract—**Digital modulation based on FSK is widely used in HF data communication. This is due to simplicity in implementation by noncoherent detection and robustness due noise and phase synchronization error.Hardware based design using FPGA can reduced system size. The proposed modulation integrates both the transmitter and receiver modules into a single FPGA. Further reduction in components is achieved by adopting a multiplierless and parallel algorithm at the receiver module. This is proven by comparing with conventional noncoherent detection algorithm.**

I. INTRODUCTION

In HF(High Frequency) data communication systems[1,2], FSK (Frequency Shift Keying) digital modulation is widely used. The simplicity in the implementation is the main reason for its popularity. Since noncoherent detection is possible, additional components such as timing recovery circuits[3] are not necessary as required in PSK(Phase Shift Keying) modulation. In addition, FSK is robust to noise and phase synchronization error that present in a HF communication environment to multipath fading[4]. Existing implementation utilized DSP processor[1,2]. The use of hardware based design such as FPGA(Field Programmable Gate Array) can further miniaturize system size and more features into existing systems. The important of FPGA in communication system application was described in[5,6]. This paper describes the implementation of a CPFSK(Continuous Phase FSK) modem on the FLEX10K board EPF10K70RC240. Both transmitter and receiver modules are integrated into a single FPGA. This is achieved by adopting a multiplierless and parallel algorithm at the receiver module comparison with conventional noncoherent detection demonstrate significant reduction in components.

II. SIGNAL MODEL

The received signal is within a bit-duration is given as

$$y(t) = x(t) + w(t) \tag{1}$$

where $x(t)$ is the true signal, and $w(t)$ is the interference due to additive white Gaussian noise with zero mean and power σ_p^2. The true signal $x(t)$ is [7]

$$\begin{aligned} x(t) = x_1(t) &= A\cos 2\pi f_1 t \quad \text{bit '1'} \\ x_0(t) &= A\cos 2\pi f_0 t \quad \text{bit'0' } t_0 \le t \le t_0 + T_b \end{aligned} \tag{2}$$

where A is the signal amplitude, f_1 and f_0 are the frequencies of the signal, t_0 is any arbitrary time instant, and T_b is the bit-duration. For simulation purposes, the modulation parameters of the signal are as follows: subcarrier frequencies f_1 f_0 at 1400 and 1800 Hz, bit-rate of 100 bits/sec and sampling frequency of 8000 Hz. The time and frequency domain representation of the signal for transmitting a binary sequence '1110010' is shown in Fig. 3.

A. *Generation Of CPFSK*

A conventional FSK signal can be expressed as

$$\begin{aligned} x(t) &= \cos\ 2\pi\left(f_c \pm f_{dev}\right)t \\ &= \cos\ 2\pi\left(f_c + \frac{h}{2T_b}\right)t \\ &= \cos\left(2\pi f_c t + \frac{\pi h}{T_b}t\right) \end{aligned} \tag{3}$$

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where h is the modulation index, f_{dev} is the deviation frequency, f_c is the center frequency and T_b is the bit duration. By assuming that $\varphi(t) = \pi ht / T_b$ Equation (3) can be derived as

$$x(t) = \cos(2\pi f_c t \pm \varphi(t))$$

$$= \frac{1}{2}\cos(2\pi f_c t)\cos(\pm\varphi(t)) - \frac{1}{2}\sin(2\pi f_c t)\sin(\pm\varphi(t))$$

$$= \frac{1}{2}\cos(2\pi f_c t)\cos(\varphi(t)) \; u \; \frac{1}{2}\sin(2\pi f_c t)\sin(\varphi(t)) \qquad (4)$$

From Equation (4), CPFSK signal can be produced by using 4 different signals with 2 frequencies. Consider f_c=1200Hz, h= 4 and T_b=1/100. The carrier frequency and modulation index derived from the modulation parameters in section 2.0 are

$$f_c = f_1 - f_0/2 = 1200$$

$$h = 2T_b f_{dev} = 2(1/100)(1800-1400)/2 = 4 \qquad (5)$$

B. Detection of CPFSK

In FSK modulation, the binary information is represented in frequency mode. This information can be extracted by calculating the power spectrum of the signal in frequency domain. The peaks of the power spectrum occur at the frequency of the signal. Spectrum based detection[8] utilizes the concept of the power spectrum. The BER (bit-error rate) performance is slightly lower than the coherent detection but phase synchronization is not critical in spectrum based detection. The power spectrum can be express as

$$S_{xx}(f) = \frac{1}{T_b}|X(f)|^2 = \frac{1}{T_b}\left|\int_{t_0}^{t_0+T_b} x(t)\,b^*(t,f)\,dt\right|^2 \qquad (6)$$

where $x(t)$ is the signal and $b(t,f)$ is the basis function. If a complex sinusoid is used as basis function, the resulting spectrum is the Fourier spectrum. The basis function based on the complex square wave defined within a period $T=1/f$ is

$$b(t,f) = 1 \quad -\frac{1}{4f} \le t \le \frac{1}{4f} \qquad (7)$$

$$= -1 \quad \frac{1}{4f} \le |t| \le \frac{1}{2f}$$

$$= j1 \quad 0 \le t \le \frac{1}{2f}$$

$$= -j1 \quad -\frac{1}{2f} \le t \le 0$$

The square wave basis function is chosen to eliminate multiplication in the hardware implementation.

III. IMPLEMENTATION METHODOLOGY

The designed system is divided into 2 major parts, which is the transmitter and receiver part. Before the hardware of the system is being design, each method is generated and tested using MATLAB.

A. Transmitter

The transmitter is designed using the digital sine-cosine generator[9]. This generator is capable to generate both sine and cosine wave which have same frequency simultaneously. Let $s_1[n]$ and $s_2[n]$ denote the two outputs of a digital sin-cosine generator given by

$$s_1[n] = \alpha \sin(n\theta)$$
$$s_2[n] = \beta \cos(n\theta) \qquad (8)$$

Equation (7) can be express for $n=n+1$

$$s_1[n+1] = \alpha \sin((n+1)\theta) = \alpha \sin(n\theta)\cos\theta + \alpha\cos(n\theta)\sin\theta = \cos\theta s_1[n] + \alpha/\beta \sin\theta s_2[n] \qquad (9)$$

$$s_2[n+1] = \alpha \cos((n+1)\theta) = \beta\cos(n\theta)\cos\theta - \beta\sin(n\theta)\sin\theta = \cos\theta s_2[n] - \beta/\alpha \sin\theta s_1[n] \qquad (10)$$

Equation (8) and (9) can be express as

$$s_1[n+1] = \cos\theta s_1[n] + (\cos\theta + 1)s_2[n] = \cos\theta s_1[n] + \cos\theta s_2[n] + s_2[n] = \cos\theta * (s_1[n] + s_2[n]) + s_2[n] \qquad (11)$$

$$s_2[n+1] = \cos(\theta - 1)s_1[n] + \cos\theta s_2[n] = \cos\theta s_1[n] + \cos\theta s_2[n] - s_2[n] = \cos\theta * (s_1[n] + s_2[n]) - s_2[n] \qquad (12)$$

Equation (11) and (12) show that sine and cosine signal can be generated by using one multiplier, 2 adders and 2 add/sub module depends on type of signal. Another adder and shift register are needed to

implement CPFSK. The transmitter is implemented based on pseudo code shows in Fig 1.

```
// pseudo code to generate CPFSK signal
for ( n=0;n<nbit;n++)
{   // generate cosA & sinA
    add1= sA1[n-1] + sB1[n-1];
    mult1= cosA * add1;
    sA1[n]= mult1 + sA2[n-1];
    sA2[n]= mult1 - sA1[n-1];

    // generate cosB & sinB
    add2= sA2[n-1] + sB2[n-1];
    mult1= cosB * add2;
    sB1[n]= mult1 + sA2[n-1];
    sB2[n]= mult1 - sA1[n-1];

   //x[n]=1/2*cosA*cosB(+-)1/2*sinAsinB
    mult1=1/2 *sA1[n]*sB1[n];
    add3=mult1;
    mult1=1/2 *sA2[n]*sB2[n];
    x[n]=add3+ mult1;
    //add/sub depends on generating bit '1/0'
}
```

Figure1. Pseudo code to generate CPFSK signal.

B. *Receiver*

Square wave detection is designed and implemented as receiver system to optimize implementation of hardware such as using ASIC and FPGA by avoiding the use of multipliers. A multiplier is required to calculate the signal-basis function product $x(t)b^*(t,f)$ in Equation (14). If the complex square wave is being used as a basic function, then the multiplication function can be done by replacing the multiplier with a sign check and compliment module. The overall system is generated based on pseudo code shows in Fig. 2.

```
// pseudo code to detection of CPFSK;
sum0=0;
sum1=0;

for ( n=0;n<nbit;n++)
{
   // f0[n] is basis function
   // x[n] is input
   // for frequency=f0

    if (f0[n]=1)
      { if ( x[n]>0)
          { sum0= sum0 + x[n];}
            else  if ( x[n]<0)
                    { sum0= sum0 - x[n];} }

   // f1[n] is basis function
   // x[n] is input
   // for frequency=f1

    if ( f1[n]=1)
    {       if  ( x[n]>0)
            {           sum1= sum1 + x[n];}
      else   if ( x[n]<0)
             {          sum1= sum1 - x[n]; }
}

if (sum1> sum0 )
   {   bit='1'    else bit='0' }
```

Figure 2. Pseudo code to generate square wave detection.

IV. RESULTS

Two types of CPFSK modems were designed. Both utilized the sine-cosine generator at the transmitter module. But the difference is at the receiver module where one utilized the conventional noncoherent detection and the other the square wave detection. Table1 summarize, the component list for implementing the noncoherent and square wave detection. The number of component required to implement the square wave detection is 60% less compared to the noncoherent detection. This is because of the parallel structure and no multiplier is used in the detection algorithm.

TABLE I. List of components for square wave and noncoherent detection.

Components	Logic cell per unit	Square wave (unit)	Non coherent (unit)
Multiplier16X16	470	0	1
Shift register 16:4 bit	17	1	2
Shift register 16:1 bit	19	4	0
Preset Counter-8 bit	24	1	2
Counter-9 bit	8	1	2
Counter-4 bit	5	1	2
Register 10 bit	11	0	1
Register 8 bit	9	0	1
Register 16 bit	16	2	8
Multiplexer 2:1(16bit)	16	0	4
Multiplexer2:1	1	0	4
Multiplexer2:1 (8bit)	8	0	1
Select2	1	0	2
Adder 8 bit	11	0	2
Adder 16 bit	17	4	2
Compare 2	21	1	1
Basis function	16	4	0
ROM		82 LC	110 LC
Control unit		29 LC	80 LC
Rx		426LC	1060 LC

V. CONCLUSION

This paper describes the design of an FSK modem on an FPGA. The hardware approach is adopted with the objective to miniaturize the system size. Two types of modems were developed with different detection scheme: conventional noncoherent and square wave detection. The square wave detection has 60% less components because of the parallel structure and no multiplier is used in the algorithm. Thus, the modem designed with the square wave detection can be made smaller.

VI. REFERENCES

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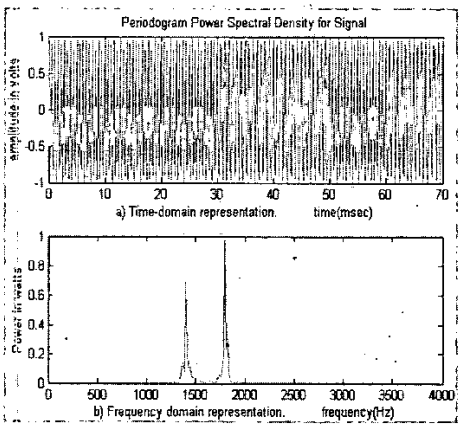

Figure 3. Time and frequency representation of an FSK signal.