Simple Analogue Active Filter Testing using Digital Modelling

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Abstract- This paper presents a new approach to detect analogue catastrophic faults via digital modelling for an analogue filter. Area of interest in this paper is to prove that analogue circuit can be translated into logic gates (0's or 1's) and investigates the effectiveness of analogue fault (short and open) in analogy approximate to digital stuck-at fault model. The purpose of testing fault that connects active component to supply terminal (stuck-at fault) is to investigate the characteristic of the output response, whether can successful model analogue fault to logic level. The approach is to sensitise primary input with an arbitrary frequency square-wave as stimuli and observes output signature in transient and frequency response in order to distinguish Go or No-GO. It is a simple method to accelerate production test without any extra circuitry. This approach has been implemented to a frequency-dependant circuit (Butterworth low pass filter) in order to verify its functionability.

Keywords
Analogue Filter, Digital Modelling, Square-wave stimulus

I. INTRODUCTION

Testing analogue integrated circuits is a challenging work as to consider about circuit performance need to be measured and verified functionality of the circuit under test (CUT). This always requires longer test time in production as compare to digital systems. With the limitation of testable input, the analogue testing has reached a crucial point and that's why DFT and BIST are main concentration in analogue testing. However, these two techniques require area overhead in which area of die becomes crucial.

Transient response strategy in testing analogue circuit becomes an issue since numerous of information can be abstracted from this domain. According to [1], since the input is a sequence of pulse two basic parameters can be varied: amplitude and width. In [2], the author tests analogue circuit by changing amplitude stimuli that is not suitable for testing on existing digital tester. In [1][3-4], authors proposed a method similar to this paper's scope (by changing pulse frequency), but they used pseudo-random binary sequence (PRBS) as stimuli and enhance the capture response by using ADC.

The idea of this paper is to introduce a simple test to evaluate the CUT performance using digital model. The advantage of this approach is to test analogue CUT without extra circuitry and test tools, as square-wave stimuli is available in digital tester.

This paper is organized in the following way: Section II explains the idea of digital modelling [1] and test methodology, while Section III presents the test results and discussion. Section IV concludes the paper.

II. MODELING METHODOLOGY

The idea of digital modelling was proposed by A. P. Dorey et al [1]. They proposed to model analogue faults as digital catastrophic fault (Stuck-at 0 and Stuck-at 1).

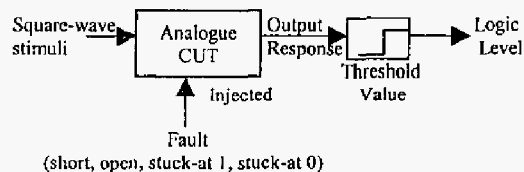

Fig. 1. Digital model of analogue faults

The proposed approach as shown in Fig. 1 is based on pulse or square-wave to stimulate primary input CUT. Digital circuits can generate this stimulus. Therefore, a conventional analogue signal generator is not required to generate the test stimuli.

The upper limit of the faults resistor for stuck-at fault has to be calibrated and it is show in Table 1 for the unity gain analogue filter. Analogue faults (short and open) are also introduced to verify that this detectable fault can be observed at the output as well.

The amplitude of output response of the faulty circuit would either shift up and down from its nominal fault free response. This is the key of digital modelling. Output response is then translated to logic level.

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Threshold value can be arbitrary depends on technology applied either TTL or CMOS, to distinguish output response to either logic 1 or logic 0.

Afterwards, by using conventional fault dictionary method, it can verify output response in logic form to detect fault, but test method is not the main point of discussion. By modelling analogue circuit and faults using digital modelling, it not only reduces required memory size for digital ATE but also cuts short testing time.

III. RESULT AND DISCUSSION

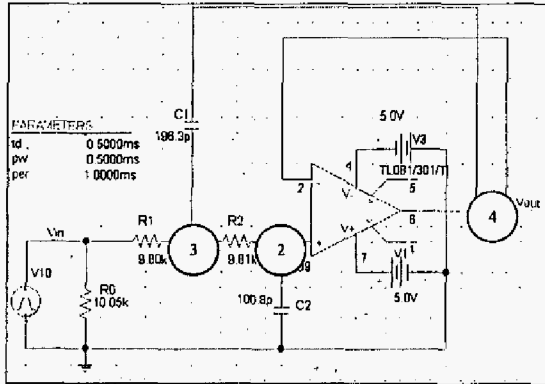


Fig. 2. Fault free unity gain Low pass filter with cutoff frequency = 100kHz

A unity gain second order Voltage-Control-Voltage-Source (VCVS) low pass filter shown at Fig. 2 is chosen as a test vehicle. To verify the practical result, SPICE simulator simulates test vehicle and both results are compared to support that digital modelling can work perfect in this fully analogue circuit.

Targeted fault in this research scope is concentrated on catastrophic fault, which means Stuck-at faults (short-to-V_{DD} or short-to-V_{GND}), shorts and open faults. A square-wave with variety of test frequencies was injected to CUT input, at this case 1 kHz had been using.

Table 1. Experimental result

Table 1.1: Stuck-at 0 (at test frequency = 1 kHz)			
Node	*Fault free impedance*	*Faulty impedance (Correspondence Voltage)*	*Transient response*
2	29.60 kΩ	0.1 – 4.90 kΩ (0.0 V – 1.0 V)	Detectable
3	19.84 kΩ	0.1 - 2.42 kΩ (0.0 V – 1.0 V)	Detectable
4	0.00 Ω	0.1 – 68.8 Ω (0.0 V – 1.0 V)	Detectable
Table 1.2: Stuck-at 1 (at test frequency = 1 kHz)			
Node	*Fault free impedance*	*Faulty impedance (Correspondence Voltage)*	*Transient response*
2	29.60 kΩ	0.1 - 7.97 kΩ (3.5 V – 5.0 V)	Detectable
3	19.84 kΩ	0.1 - 4.24 kΩ (3.5 V – 5.0 V)	Detectable
4	0.00k Ω	0.1 - 59.4 Ω (3.5 V – 5.0 V)	Detectable

Table 1.3: Short and open faulty result				
No.	*Short*	*Transient*	*Open*	*Transient*
1	R0	*	R0	*
2	R1	Undetectable	R1	Detectable
3	R2	Undetectable	R2	Detectable
4	C1	Detectable	C1	Undetectable
5	C2	Detectable	C2	Undetectable

Table 2. Simulation result

Short and open faulty result				
No.	*Short*		*Open*	
1	R0	*	R0	*
2	R1	Undetectable	R1	Detectable
3	R2	Undetectable	R2	Detectable
4	C1	Detectable	C1	Undetectable
5	C2	Detectable	C2	Undetectable

*R0 is in parallel with the input stimuli either short or open, it would not affect voltage dropped or current consumed on the overall circuit performance.

For future expansion, logic 0 is defined for output voltage below or at 1.00 V; logic 1 is defined above or at 3.50 V. Therefore, output response will translate to logic (101010...) form in fault free condition. The fault would shift the amplitude of the output response either upward or downward if a fault is introduced in the CUT. Under this circumstance, if a voltage shift above 3.50 V, it is considered as logic 1, otherwise, if it shifts below 1.00 V, it would be defined as logic 0.

Fault that short-to-V_{GND} for example, node 2 in Table 1.1 can be detected and this is shown in Fig. 3. Impedance measurement is the strong evident to prove it works. For the faulty impedance of 4.90 kΩ, as both fault free and faulty impedance in parallel, the equivalent new impedance for node 2 would be approximately 4.20 kΩ. From basic Ohm Law, if resistance drops, voltage for that node decrease and thus, when output response is measured, it goes to approximate 1.00 V that is considered as logic 0 (it is 5 V for fault free). In vice versa, it is true for node 2 when it is short-to-V_{DD}. The ultimate logic for this fault is logic 1 (it is 0 V for fault free) and the result in transient response (for faulty impedance = 7.97 kΩ) shown in Fig. 4.

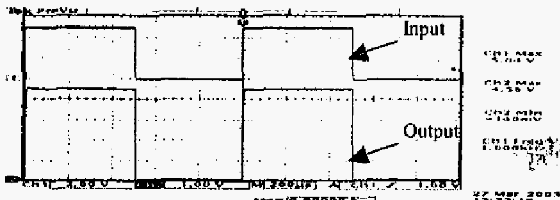


Fig. 3 (a): Fault Free

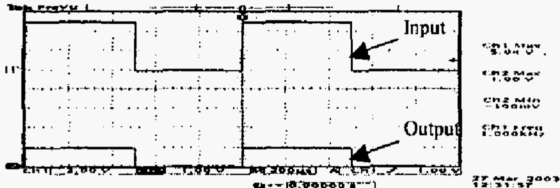


Fig. 3 (b): Faulty for node 2 (short-to-V_{GND})

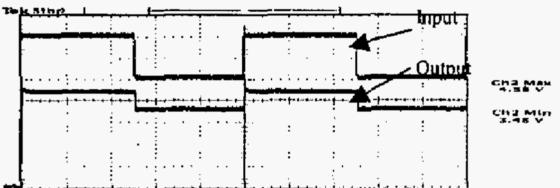


Fig. 4: Faulty for node 2 (short-to-V_{DD})

When R2 is made open and short circuits the transient response shows in Fig. 5 and Fig. 6 respectively. The graphs show that only R2 open fault can be detected and translated to logic 0.

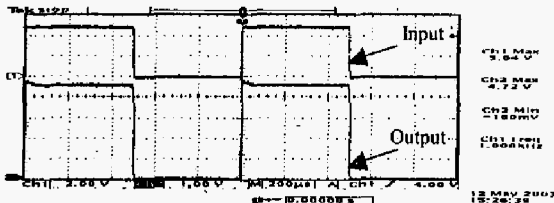


Fig. 5: Response of R2 Short in transient domain

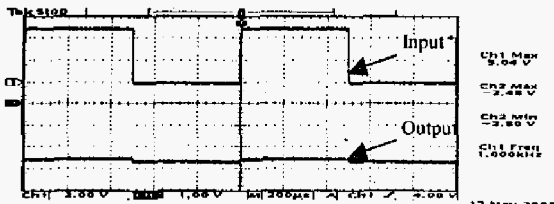
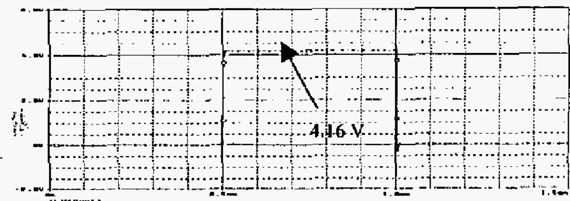
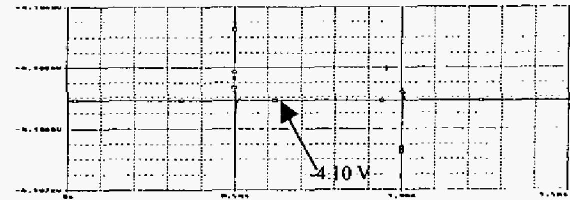


Fig. 6: Response of R2 Short in transient domain

From the observation, analogue faults such as C1 (short), C2 (short), R1 (open) and R2 (open) in transient domain can be detected and modelled to digital value. They were verified through simulation. Fig. 7 shows the simulation response of R2 short and open circuits.



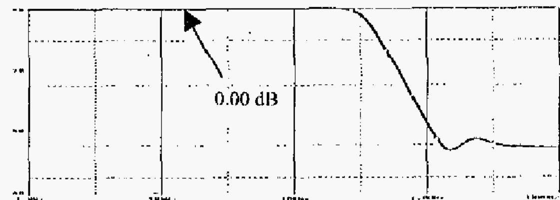
7 (a): Fault Free



7 (b): Faulty

Fig. 7. Response for (a) R2 –open 7 (b) R2-short

Frequency response of these detectable analogue faults shifted from their nominal shape, which can be easily identified as compared to fault free. Fig. 8 shows the simulation response for R2 (open) in frequency domain. It highlights the difference between a fault free response and a faulty response due to R2 open circuit. As long as test frequency sweeps within the passband of the CUT, fault coverage would not be affected.



8 (a): Fault Free

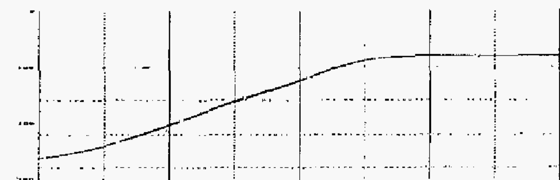

8 (b): Faulty

Fig. 8. R2 (open) in frequency response

Soft faults, which were caused by C2 open, C1 open, R1 short and R2 short are not suitable to use digital model.

From the frequency response, several conclusions could be analysed as below:

1) If the magnitude of the gain of the frequency response is below than the fault free gain before cutoff or totally shifted out of the nominal shape, it is considered detectable.

2) A fault is categorised as detectable in transient response if the magnitude substantially different from the fault free magnitude.

3) Fault which only cause the change in the cutoff frequency or phase shift would unlikely be detected by digital modelling.

Fig. 9 shows a CUT with gain = 2 but with cutoff frequency 10 kHz. Now, R3 and R4 are choose model fault using this propose approach. From the simulation, R3 (short) and R4 (open) can successfully model both fault to logic 1. This is shown in Fig. 10, while Fig. 11 shows frequency response for both detectable faults.

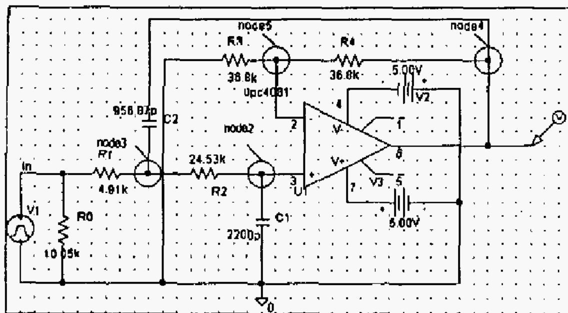


Fig. 9. CUT with gain =2

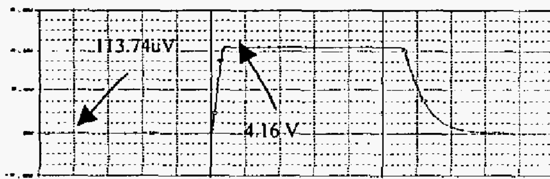


Fig. 10 (a): Fault Free

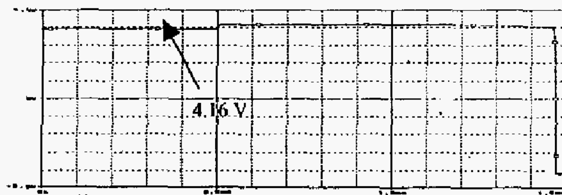


Fig. 10 (b): Faulty (R3-short)

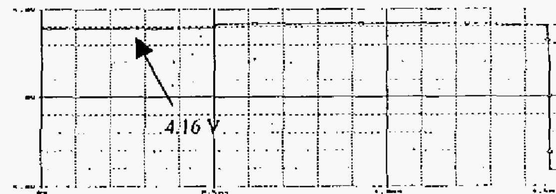


Fig. 10 (c): Faulty (R4-open)

Fig. 11(a): Fault free

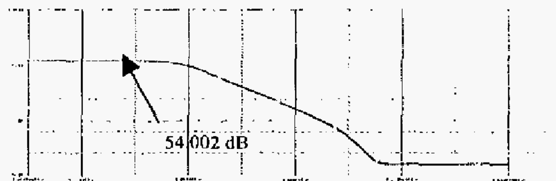


Fig. 11 (b): Faulty (R3-short)

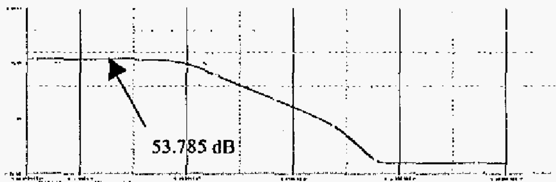


Fig. 11 (c): Faulty (R4-open)

IV. CONCLUSION

Fault, which alters the amplitude of the frequency response, is suitable as digital model. This is supported by transient response. In vice versa, fault that does not alter the amplitude of the frequency response is not suitable as digital model. This is also supported by transient response.

V. REFERENCES

[1] Mahmoud A Al-Qutayri and Peter R Shepherd, "PRBS Testing of Analog Circuits", Testing Mixed Signal Circuits, IEE Colloquium, pp.4/1 -4/5, 15 May 1992.

[2] Heinzh H. Schreiber, "Fault Dictionary Based upon Stimulus Design", IEEE Trans. Circuits and Systems, Vol. CAS-26, pp.529-537, 1979.

[3] P. R. Shepherd, A. Bertin and M. A. Al-Qutayri, "Implementation of the Transient Response Measurement of Mixed-signal Circuits", European

Test Conference 1993, Proceedings of ETC 93, Third, pp. 66 –73, 19-22 April 1993.
[4] P. R. Shepherd, M. A. Al-Qutayri and P. S. A. Evans, "Testing mixed signal integrated circuits", Design and Test of Mixed Analogue and Digital Circuits, IEE Colloquium, pp.4/1 -4/4, 15 Nov 1990.
[5] A. P. Dorey, P. J. Silvester and R. J. Ball, Development in Integrated Circuit Testing, UK: Academic Press Limited, pp.391-405, 1987.