DIE DESIGN OF A TRANSMITTING TRANSISTOR IN A 175 MHz POWER AMPLIFIER AT 28V

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Abstract – **This paper presents the die design of a NPN transistor, which is targeted for operation in a power amplifier. The proposed die is designed using epitaxial planar bipolar junction technology. The transistor die is designed for operation in the 175MHz frequency range with a 28V biasing. It is capable of producing a maximum output power of 4W. It can be utilized in Class A, Class B or Class C power amplifiers meant for transmission purposes such as in mobile communication, industrial communication or military transmitters. The power amplifier is typically placed before the antenna in transmitter systems. It is best to couple the design in a two-stage amplifier to produce a significantly higher-powered signal for transmission.**

I. INTRODUCTION

Transmitters are an essential block in wireless communication and broadcasting systems today. The basic role of a transmitter is to process and transmit the desired information signal. The function of a power amplifier in a transmitter is to enhance or increase the power of the transmitted signal to enable it to be received at the receiver point after undergoing a series of losses. The power transistor is the heart of the operations of a power amplifier.

The designed power transistor is operated in a power amplifier too. In order to evaluate the operations and parameters of the die, it is biased in a Class B common-emitter power amplifier test circuit here. Class B power amplifiers are biased at cutoff such that it operates in the linear region for 180% of the input cycle and is in cutoff for another 180%. The primary factor in selecting a Class B power amplifier is because of the high efficiency of the device. The circuit has been designed to house the power transistor to work optimally. The disadvantage of this power amplifier is the signal shape distortion produced in the output signal. However this issue is negligible here since the main objective of the circuit is to test the operations of the power transistor.

As mentioned earlier, epitaxial planar bipolar junction technology is used in the designing of the die. Bipolar junction technology is used to create a NPN transistor die here. This particular technology was chosen compared to CMOS, GaAs MESFET, HEMT or III-V HBT technology due to the optimum functioning of semiconductor devices operating below 3GHz frequency, in this technology. The devices tend to yield better power density values, good noise characteristics and excellent RF integration capabilities with moderate linearity and efficiency using the bipolar junction technology. Practically speaking, bipolar junction devices are cheap to fabricate and have very high maturity level in the industry. Implementation of the epitaxial technology, whereby a low-concentrated epitaxial layer is grown above the substrate, helps to lower the resistivity of the substrate and affects certain important parameters, which will be discussed later on. The term planar here points to the even deposition of materials such as silicon dioxide throughout the die.

II. THE TRANSISTOR DIE AND TEST CIRCUIT

Following are certain parameters of the designed transistor operating in the test circuit. The circuit housing the designed transistor is simulated in the Multisim Version 7 software to derive its performance.

Certain important parameters of the transistor that have to be given specific concentration while

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designing the die are such as the frequency and the power output. The die is designed for operation in the Very High Frequency (V.H.F) band, 175MHz to be specific. This particular frequency band is usually used for non-broadcasting FM transmission and for high-band V.H.F TV broadcasting. The term power output would already highlight the importance of the output power parameter. The transistor is designed to output a maximum power of 4 Watts. It is indeed obvious that this output power is insufficient for transmission purposes. The transistor would have to be coupled in a two-stage or three-stage power amplifier to amplify the power of a signal up to a level permissible for transmission. In fact, a large number of power transistors, if not all, are designed for housing in a multi-stage power amplifier.

The transistor's operations and performance is tested in an unneutralized Class B common-emitter power amplifier biased at 28 V. The circuit is a test circuit designed specifically to enable the transistor to operate optimally. The circuit and the simulation results are displayed in the test and results section.

III. DIE DESIGN ISSUES

The die designing procedure of large signal amplifiers such as this power transistor is similar to the designing of small signal amplifiers in certain ways. They defer mainly only in the issue of achieving higher power output. The design considerations taken in order to achieve the other parameters are more or less the same in both amplifiers except in their values.

As mentioned earlier, the output power is an important parameter of the power transistor. The emitter plays the most important role in achieving this. The emitter must be dimensioned in such a way to enable the transistor to deliver the required output power while also minimizing performance-degrading effects such as capacitances. The emitter area and periphery are important matters in achieving this due to the '*Emitter- Crowding* ' effect as shown in Figure 1.

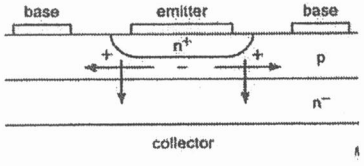

Fig. 1 '*Emitter- Crowding* ' Effect

This effect is caused by the electrons of the base that make the base positive at the edge of the emitter and negative at the center of it. Therefore, the I_c is only concentrated at the edges of the emitter, making the emitter periphery the main factor in determining the output power. Under normal operating conditions, only about 1-2 μm of the edge of the emitter is operational while the rest, mainly in the middle of the emitter, is redundant and merely introduces capacitance in the die. Practically speaking, it is best to create an emitter design with the width of 2-4 μm for the reasons mentioned above. For an emitter design with the stated width, an emitter periphery of 2mm is needed to produce an output power of 1 Watt. A narrower emitter, say around 2 μm wide is more beneficiary such as for parasitic loss reasons, but would demand a higher amount of periphery per watt output. By applying the 2-4μm width count, it is obvious that a total emitter periphery of 8mm is needed here to achieve an output power of 4 Watts. Designing a narrow and long emitter layout would not be practical in the sense of die area.. Therefore it is suitable to design many '*fingers*' of around 3 μm wide to give the total periphery needed. This approach is deemed the '*Interdigitated*' approach .The emitter design is split into several parallel parts with the base design contacts in between the fingers. An '*Interdigitated*' approach die design is shown in Figure 2.

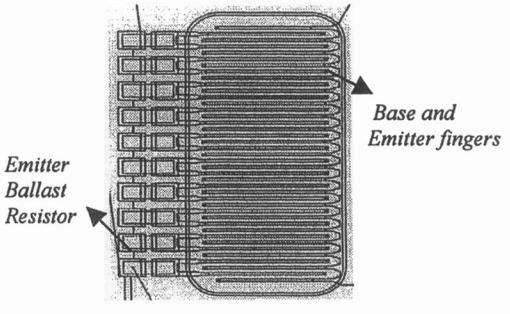

Fig. 2 Interdigitated approach

The finger pitch is inversely proportional to the operating frequency of the die. A high operating frequency would result in a small pitch. All the fingers are connected at one end by metallization. Voltage drop along each finger must not exceed 25 to 30mV in order to prevent any one of the fingers at the other end to be cut off from the metallization piece. It can be seen here that the emitter is split into such fingers for

many beneficial reasons such as die area consideration and to lower parasitic loss due to area redundancy.

The base can be split into fingers similar to the emitter to reduce thermal resistance, increase base periphery and add more bonding pads to increase gain. The distance among base fingers is usually taken as 2 times the thickness of the die, which is 300 μm usually. However this technique tends to also introduce unwanted capacitance in the die. Splitting of the base is not necessary for low power devices, say 3 or 4 Watts and therefore is not applied here. A single base with multiple contact points (each point with p+ tubs to enhance contact) approach is applied.

Emitter ballast resistors are always an essential built-in component in power transistor dies. It is a must especially for transistors meant for operation in Class A and Class AB power amplifiers. Its primary function is to distribute the collector current, I_c equally among all fingers and thus preventing it from being concentrated at the middle of the die where the temperature is highest, causing an increase in thermal resistance. Each emitter finger is provided with a ballast resistor .The resistance of the resistor is controlled by means of dopant concentration to enable a voltage drop of 200 to 300 mV across the fingers at normal DC collector current. The resistors are created by means of depositing a polysilicon layer on top of the silicon dioxide layer. The resistors can also be produced by implanting p+ diffusions into the epitaxial layer by the side of the base areas but this approach introduces parasitic capacitance and is implemented for multi-base designs usually.
The temperature coefficient (t.c.) of a diffused emitter resistance is positive and at practical operating temperatures(~125°C),the resistance increases by 0.1%K.The t.c. of a polysilicon resistor is much smaller. The creation of the resistors are shown in Figure 3 and Figure 4.

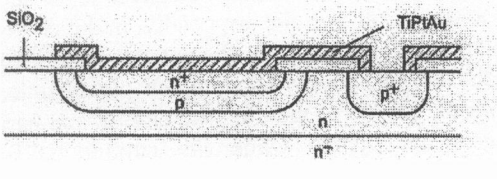

Fig. 3 P+ Diffusion as a resistor

Another important parameter that needs to be given special consideration here would be the frequency transition, f_T . The f_T is designed to be typically 500MHz in order to accommodate for the 175MHz operations that was intended for this transistor. This f_T value can be achieved by implanting a shallow base with low dopant concentration. The h_{FE} parameter too has to be considered when designing the base as the h_{FE} is dependant on the dopant concentration and junction depth of the base. The relation between this particular parameter with the base can be seen clearly from the equation $h_{FE} = I_C / I_B$. A h_{FE} value of 50 would be ample for operations in the RF region.

The reverse bias parameters too, especially the breakdown parameter has to be given due consideration. There are a total of 7 breakdown voltages that are common that is BVCBO , BVCEO , BVEBO , BVCES , BVCEX , BVCER and BVCEY. However in designing the device, attention is given only to the BVCBO and BVCEO parameters. The BVCBO, reverse collector to base voltage with the emitter open, and the BVCEO ,reverse collector to emitter voltage with the base open, are important parameters in the common-base(CB) and common-emitter(CE) operations respectively. For devices operating at 28V V_{CC}, it is a must to provide a BVCBO value of around 65V with the typical value being 80V.This can be achieved by depositing an epitaxial layer of around 1.6 to 2.0 Ωcm^{-1} with the default dopant concentration of around 10^{14} . The BVCEO is designed to be at a typical value of 40V.Power transistors are also prone to second breakdowns. The breakdown happens at a voltage of between the BVCEO and BVCBO value. However this process can be prevented if the epitaxial thickness is made sure to be thicker than the collector depletion layer at the second breakdown voltage.

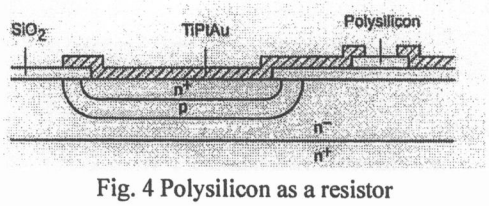

Fig. 4 Polysilicon as a resistor

All other parameters such as leakage and capacitance values are designed similar to considerations taken when designing other devices such as small signal amplifiers.

IV. TEST AND RESULTS

Two tests and their respective results are displayed in this segment.

A. TEST CIRCUIT SIMULATION

The transistor test circuit and its simulation results, done in Multisim V7 are displayed below. The test was performed in order to verify that the parameters targeted are appropriate for the device to deliver the expected output, The transistor is modeled in the software according to the targeted parameters. Displayed results are a collective of all results garnered by varying the input signals. The circuit is impedance matched.

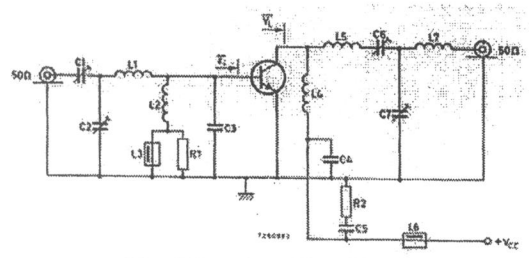

Fig. 5 Transistor Test Circuit

C1 = C6 = 4 to 29 pF air trimmer with insulated rotor
C2 = C7 = 4 to 29 pF air trimmer with non-insulated rotor
C3 = 39 pF ceramic
C4 = 100 pF ceramic
C3 = 15 nF polyester
L1 = 1 turn enameled Cu wire(1.0mm) ; Int. diam. 10mm ; leads 2 x 10 mm (~35nH)
L2 = 6 turns enameled Cu wire(0.7mm) ; Int. diam. 4mm ; leads 2 x 10 mm (~80nH)
L3 = L6 = ferroxcube choke
L4 = 8 turns enameled Cu wire(0.7mm) ; Int. diam. 4mm ; leads 2 x 10 mm (~100nH)
L5 = 5 turns enameled Cu wire(1.0mm) ; Int. diam. 8mm ; leads 2 x 10 mm ; winding pitch 1.0mm (~130nH)
L7 = 4 turns enameled Cu wire(1.0mm) ; Int. diam. 6mm ; leads 2 x 5 mm ; winding pitch 1.0mm (~130nH)
R1 = R2 = 10 Ω carbon

Collective results :

f(MHz)	P_S (W)	P_L (W)	I_C (A)
175	<0.40	4	<0.22

G_p (dB)	η (%)	Z_i (Ω)	Y_L (mS)
>10	>65	2.3+j1.6	8.9-j18.1

B. DIE FIGURE

Other than considering the parameters of the device, some attention has to be given towards the layout of the die. It is customary to run a few process simulations in order to produce the accurate design. These process simulations are emphasized particularly on deriving the lateral diffusion of the base and emitter tubs. It is used to determine the spacing between the emitter fingers and base contact points of the die. Dopant concentration and outer diffusion are the other issues observed when running these simulations. Following are collective results of the lateral diffusion for the emitter well and base p+ tubs at contact point.

Measurement(μm)	Left Lateral Diffusion	Right Lateral Diffusion
Emitter Fingers	1.2	1.1
Base Contact P+	1.9	1.9

After having considered the necessary parameters and performing the process simulations using the Silvaco Athena simulator, the design of the necessary layers were done in the DW-2000 software. A total of 5 layers are needed for the die design, which are base, emitter, contact, metal and plasma nitride. The collector layer is supported by the epitaxial formation on the substrate of the die as mentioned earlier. The plasma nitride layer acts as a shield on the die especially in hindering contaminations. Figure 6 illustrates the top view of the die design shown with the metallization covering the top of the die. The emitter and base fingers are visible while the emitter ballast resistor structure is not visible. Figure 7 illustrates the cross section of the die for a small portion only as the whole die has a similar repetitive cross section. It is illustrated with the emitter finger in the middle with two base contacts accompanying it by the sides. It is indeed an interdigitated single base approach.

The lateral diffusion factor is taken into consideration in spacing the emitter fingers with the base.

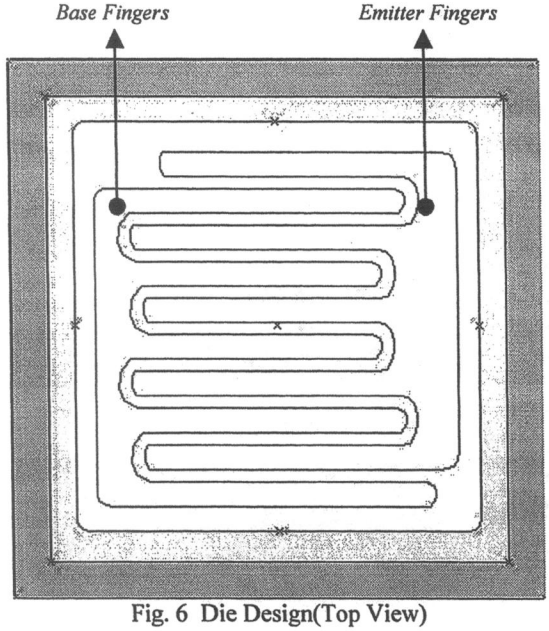

Fig. 6 Die Design(Top View)

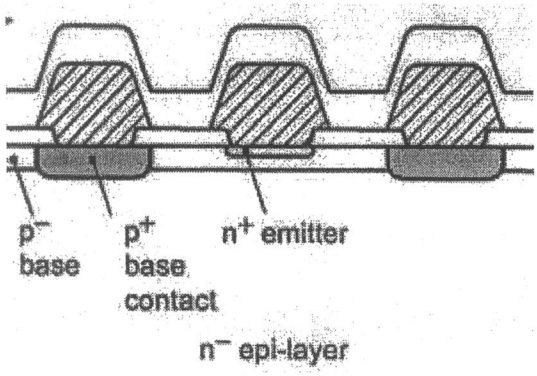

Fig. 7 Portion of Die Cross Section

V. Conclusion

A power transistor die was designed successfully according to targeted specifications. The die is able to operate optimally in a 28V biased power amplifier at 175MHz with a maximum power output of 4W.

VI. References

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