AN INVESTIGATION ON ADC TESTING USING DIGITAL MODELLING

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ABSTRACT

This paper presents an analysis of test results of digital model approach on Analogue-to-digital converter (ADC). The approach is to inject primary input with arbitrary frequencies and periodical digital pulse. The output response is sampled and analysed in order to distinguish between GO or No-GO. Furthermore, the proposed technique is also coupled with power supply voltage control test technique to investigate the fault coverage margin. Histogram test, conventional industrial test technique, simulates concurrently were also employed as a comparison study.

Keywords: ADC, Digital modelling, pulse stimulus, mixed mode test, unify circuit test, Power Supply Voltage Control test

1. INTRODUCTION

Testing ADC consume a lot of time and resources (memory of tester), especially in conventional method – Code Density Test Method or Histogram Test.

Because of a lot of information can be abstracted directly from transient response the circuit-under-test (CUT), it is much more convenient to directly make use of this resource on testing ADC compared with other methods that involves output response transformation [2–4]. This also need precise input stimuli such as Sine Wave Curve Fit (SWCT) [5], Spectral test [6] and Histogram test (Sine-wave stimuli) [7]. All these methods are complex specification-based ADC test that required no fault model, but time-consuming calculation to perform verification and testing. Almost a decade researchers work with transient response, in [8], they proposed that analogue and mixed mode CUT could be tested unify by a Pseudo Random Binary Sequence (PRBS). The output data is then analysis and processed using mathematical calculation, such as sample values, rate of change, auto-correlation and cross-correlation and response digitisation. However, it is difficult to select appropriate optimise bit length and interval for PRBS to stimulate the CUT. Some basic knowledge must be obtained from CUT in order to generate enough Fourier components for PRBS to test critical region in the CUT. Besides, data processing involves a lot computation. All these lead to longer testing time and consume large memory size.

In [9], DFT (Interface Scan bus) was proposed on CUT in order to increase fault coverage especially for particular fault. Besides, they categorized any detectable fault using generated Index Functionality of cross-correlation function from the CUT. However, this is rule out in this research scope, as it requires extra circuitry into the CUT.

This paper is organized in the following way: Section II explains the idea of digital modelling, while Section III presents catastrophic fault model and CMOS process technology. Digital modelling test methodology, Histogram Test and Power Supply Voltage Control test technique will be described in Section IV. Results and discussion are explained in Section V, and finally, Section VI concludes the paper.

2. DIGITAL MODELLING

Digital Modelling is a simple test technique, which was originated by A.P. Dorey et al. [1]. However, no serious work has been done to explore the strength of this approach. The proposed approach as shown in Fig. 1 is based on a periodical digital pulse or square-wave with an arbitrary frequency to stimulate primary input of CUT. The key of digital modelling approach for analogue circuit was described further in [10]. However, in this paper, the main idea to implement digital modelling approach is to unify mixed-signal test in one go. In order to distinguish output response between logic 1 and logic 0, a voltage shift above (V_{DD}X0.70) V is considered as logic 1, otherwise, if it shifts below (V_{DD}X0.20) V, it would be defined as logic 0 (these threshold values are based on high CMOS microcontroller critical input voltage specification as for future work expansion and can be altered depends on targeted CUT and CMOS process technology).

3. TRANSISTOR FAULT MODEL AND PROCESS TECHNOLOGY

The evaluation of digital modelling approach in simulation requires transistor level fault model analysis.

0-7803-8560-8/04/$20.00©2004IEEE

Fig. 2 depicts 5 transistor defects and 2 in-circuit node defects. In general, fault model for transistor terminal short represents a resistor with the value between 1 Ω and 1 kΩ, while for terminal large open the value are 1 MΩ (interconnect open) and 10 MΩ (gate open) [11]. Some paper [8] also proposed to simulate the entire open fault in 100 MΩ as well. However, in this paper, R1 and R2 are purposely chosen to correspond to the narrow open-circuit at diffusion layer; while R3-R5 corresponds to large resistive short-circuit at adjacent diffusion layer. R6 and R7 represent low resistive short between certain node to supply or ground (metalisation layer).

4. TEST METHODOLOGY

This section explains test set up for the proposed test technique.

4.1. Digital Modelling Test Technique

The basic idea of digital modelling is to model or translate the effect of an analogue fault to logic level by injecting an arbitrary frequency square-wave (a pulse) stimuli. In order to determine whether the CUT will functionally fail or not, the transient response of the faulty circuit is observed and compared with fault free signature. Several facts stated below are to support why some setting and value have been chosen.

a) A square-wave or pulse is chosen due to its transient characteristic. In [11], AC/transient test is required to obtain higher fault coverage for analogue circuit and, it is easy to generate from industry power supply instrument and digital tester. Besides, it can be directly implemented to the digital circuit. Therefore, it is suitable to use for testing mixed mode circuit.
b) It has been proven that there is no significant effect to the coverage by changing the test stimulus frequency in [10]. This is supported in Fig. 4, which shows the results of selected faulty nodes M275 (Gate-to-Source short circuit) and M276 (Gate-to-Source short circuit) with two stimuli in different test frequency (10 Hz and 100 kHz). This shows that frequency does not affect test coverage (as long as it is within the typical operating region.
c) Transient response contains a lot of information about circuit performance and it is easier to analysis it in logic level. Requirement of complex hardware can be avoided if the logic level could be further categorized into different level.

Therefore, a 1 kHz square-wave was with 5 V amplitude was chosen to stimulate the CUT. Supply voltage of ± 5 V and a reference voltage as 10 V (this reference voltage is based on typical design work).

4.2. Power Supply Voltage Control Test technique

Power Supply Control test technique [11] was also coupled with digital Model technique to test the CUT. This is due to high fault coverage that had been achieved using power supply voltage control approach on digital and analogue circuits. It was found in [11] that the effect of defects has better change to propagate in the CUT to its primary output which resulted them to be exposed by analysing the sequence of bias point analysis.

In this paper, the power supply and reference voltage of CUT were discretely reduced and digital Modelling test was also applied. This to cause variation in V_{DS} and V_{GS} as reported in [11]. For this investigation, CUT was configured and simulated like the setting in Table 1.

The idea to simulate Test **I** is to accommodate for resistor string have better fault exposure. Besides, it is to investigate the effect of reference voltage change to the fault detection by lower down the value. Test **II** and test **III** simulate in order to observe the result of reducing power supply contribute to the fault exposure when it is coupling with the digital modelling test technique. Another purpose of Test **II** is to provide a better change to comparator modules, which contains fault, for fault exposure.

4.3. Histogram Test Technique

As a comparison study, the conventional ADC test technique, histogram test was performed. Two parameters – Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) were observed. If either INL or DNL is over |0.5| LSB (in fault free condition, INL= -0.14695 LSB and DNL= -0.34594 LSB), it was considered as detectable. A ramp function with 10001 samples from 0 V to 5 V was injected to the CUT. The reference voltage was set to 5 V.

5. RESULTS AND DISCUSSION

The CUT has 351 transistors. Due to space limitation, only selected transistors of are the subject of testing and discussion for this paper.

Through digital modelling test (sample points - 0.300ms and 0.700ms), transistor M278 in Table 2 is categorized as detectable. The fault free signature for the CUT is 01 (MSB) and 00 for the last two bit (include LSB shown in Fig. 5(b). This can be explained by analysing the transistor's operating point. A fault is categorized as detectable by digital modelling test if the faulty transistor would change its operating and the faulty device's parameters (V_{GS} or V_{DS}) must be quite significant as shown in Table 5 and Fig 6. However, they're also some exceptional case in which the fault may not change the operating region of the faulty transistor. Due to poor propagation and observability, fault may not propagate from faulty location to the observation output point.

From the Table 2 – 4, one can observe that fault detection achieved moderate coverage in analogue and digital modules by using digital modelling test, which were used together with power supply voltage control approach. It is easy to expose short fault (resistive short on transistor or power supply/ ground

short faults) compared to narrow open fault in digital module through digital modelling test technique. Digital modelling test like other test technique (e.g. Histogram test and Transient Response Analysis) is not sufficient enough to detect narrow open fault either analogue or digital module due to memory effect induces from transistor open circuit (there is 0% fault coverage for priority encoder module under both digital modelling and Histogram test technique).

In this research work, discrete power supply is controlled and implemented instead of using continuously power supply as recommended in [11]. Besides, there are some faults, which can only be exposed under specified low power supply as mentioned in [11] instead of 5 V or 3 V supply implemented in this work (Table 1).

By inverting the initial stimuli value, digital modelling test technique alone is capable to increase its fault coverage on digital module (priority encoder) for certain undetectable faults (when using logic 0 as initial stimuli) in which majority of them are also detected when tested by with power supply voltage control test technique. However, inverting the initial stimuli value has no effect on analogue modules (resistor string and comparator). Besides, result shows that there is not much different on fault detection between analogue module and digital module in a mixed mode circuit regardless of propagation problem.

Simulation time consumed by digital modelling test for 175 simulated defects (included defects not shown in Table 2 – 4) in this paper is 60 minutes and 22.5 second; whereas it is 415 minutes and 42.75 seconds using histogram test technique. This is one of the obvious advantages of digital modelling, which can complete the test faster than conventional test technique. Digital Modelling test has potential to complement fault detection for histogram test due to some faults (large resistive short, narrow open, Short-to-V_{DD} and, Short-to-V_{GND} faults) were not exposure under this ADC conventional test technique.

Table 7 shows an increment of fault coverage by having 2 extra observation intervals at the pulse transition for those defects that cannot detected by digital modelling test, or used together with power supply voltage control test. The pulse transition is important in ADC test because it covers fault, which can only be exposed at low input voltage. The only trade off is precise and sensitive sampling point is required. However, proper sampling point is not within the research scope and it may vary from one circuit to another.

From the result, it can be summarized that a defect in a flash ADC can be detected by digital modelling test approach if

a) The defect is able to change significantly the magnitude of V_{GS} or V_{DS} of faulty device's (transistor) characteristic far away from its fault free value, and
b) The effect of the defect must be propagated from its faulty location to the observation output point (in this research is primary output). This means that ideally many transistors along the propagation path must also be affected – in terms of change in operating regions as shows in Table 6, and
c) The defect does not cause the transistor to induce memory effect in its faulty location.

6. CONCLUSION

Results on digital modelling suggest that it is possible to unify mixed mode circuit test signature. The nature of the test, which is simple, calls for in depth research work in this area. To increase the fault coverage for analogue module, it is suggested to test the CUT by employing digital modelling and power supply voltage control test together. Another alternative is to sample at the pulse transition and this is true for both digital and analogue modules. In future, the proposed test technique is going to be implemented in a microcontroller based digital tester.

7. REFERENCES

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Table 1: Supply configuration

	I	II	III
REFERENCE VOLTAGE	5 V	5 V	3 V
ANALOGUE INPUT (SQUARE-WAVE)	5 V	5 V	3 V
POWER SUPPLY			
*POSITIVE SUPPLY	+5 V	+5 V	+3 V
*NEGATIVE SUPPLY	0 V	-5 V	-3 V

Table 2: Fault coverage for short fault in resistor string module

No. Transistor		DM		PSVC + DM			Histogram Test
		Initial-0	Initial-5	**I**	**II**	**III**	
M275	D-S	N	N	**Y**	**Y**	**Y**	Y
M276	D-S	**Y**	**	**	**	**	Y
M277	D-S	N	N	N	N	N	Y
M278	D-S	**Y**	**	**	**	**	Y
M279	D-S	N	N	N	N	N	Y
M280	D-S	**Y**	**	**	**	**	Y
M281	D-S	**Y**	**	**	**	**	Y
M282	D-S	N	N	N	**Y**	**Y**	Y
M283	D-S	N	N	N	N	N	Y
M284	D-S	N	N	N	**Y**	**Y**	Y
M285	D-S	N	N	N	**Y**	N	Y
M286	D-S	N	N	**Y**	N	**Y**	Y
M287	D-S	N	N	N	N	N	Y
M288	D-S	**Y**	**	**	**	**	Y

Table 3: Fault coverage for short fault in comparator module

No. Transistor		DM		PSVC + DM			Histogram Test
		Initial-0	Initial-5	**I**	**II**	**III**	
M427	D-S	**Y**	**	**	**	**	Y
M428	D-S	N	N	N	N	N	Y
M429	G-D	**Y**	**	**	**	**	N
	D-S	N	N	N	N	N	Y
M430	G-D	N	N	**Y**	N	**Y**	Y
	G-S	**Y**	**	**	**	**	Y
	D-S	**Y**	**	**	**	**	Y
M431	G-D	**Y**	**	**	**	**	Y
	G-S	**Y**	**	**	**	**	Y
	D-S	**Y**	**	**	**	**	Y
M432	D-S	**Y**	**	**	**	**	Y
M433	G-D	**Y**	**	**	**	**	Y
	D-S	**Y**	**	**	**	**	Y
M434	G-D	**Y**	**	**	**	**	Y
	G-S	**Y**	**	**	**	**	Y
	D-S	**Y**	**	**	**	**	Y
M435	D-S	**Y**	**	**	**	**	Y
M261	G-D	**Y**	**	**	**	**	Y
	D-S	**Y**	**	**	**	**	Y
M262	G-S	**Y**	**	**	**	**	Y
	D-S	**Y**	**	**	**	**	Y

Table 4: Fault coverage for short fault in encoder module

No. Transistor		DM		PSVC + DM			Histogram Test
		Initial-0	Initial-5	**I**	**II**	**III**	
M269	G-D	**Y**	**	**	**	**	Y
	G-S	N	**Y**	**Y**	**Y**	**Y**	Y
	D-S	**Y**	**	**	**	**	Y
M270	G-S	**Y**	**	**	**	**	Y
	D-S	N	**Y**	**Y**	**Y**	**Y**	Y
M225	G-D	**Y**	**	**	**	**	Y
	G-S	**Y**	**	**	**	**	Y
M226	G-S	N	**Y**	**Y**	**Y**	**Y**	Y
M221	G-D	**Y**	**	**	**	**	Y
	G-S	N	N	N	N	N	Y
M222	G-D	**Y**	**	**	**	**	Y
	G-S	N	**Y**	**Y**	**Y**	**Y**	Y
M223	G-S	**Y**	**	**	**	**	Y
	D-S	N	N	N	N	N	Y
M224	G-D	**Y**	**	**	**	**	Y
	G-S	**Y**	**	**	**	**	Y
	D-S	N	**Y**	**Y**	**Y**	**Y**	Y
M213	G-D	**Y**	**	**	**	**	Y
	G-S	**Y**	**	**	**	**	Y
M214	G-D	**Y**	**	**	**	**	Y
	G-S	**Y**	**	**	**	**	Y
M215	G-D	**Y**	**	**	**	**	Y
	G-S	N	N	N	N	N	Y
	D-S	**Y**	**	**	**	**	Y
M216	G-S	N	N	N	N	N	Y
M131	G-D	**Y**	**	**	**	**	Y
	G-S	**Y**	**	**	**	**	Y
	D-S	N	**Y**	**Y**	**Y**	**Y**	Y
M132	G-D	N	**Y**	**Y**	**Y**	**Y**	Y
M133	G-S	N	**Y**	**Y**	**Y**	**Y**	Y
	D-S	**Y**	**	**	**	**	Y
M134	G-D	N	**Y**	**Y**	**Y**	**Y**	Y
	G-S	**Y**	**	**	**	**	Y
M135	G-D	**Y**	**	**	**	**	Y
	D-S	**Y**	**	**	**	**	Y
M136	G-S	**Y**	**	**	**	**	Y
	D-S	N	**Y**	**Y**	**Y**	**Y**	Y
M89	G-D	**Y**	**	**	**	**	Y
	G-S	**Y**	**	**	**	**	Y
	D-S	N	N	N	N	N	Y
M90	G-D	**Y**	**	**	**	**	Y
	G-S	**Y**	**	**	**	**	Y
M91	G-S	N	N	N	N	N	Y
	D-S	**Y**	**	**	**	**	Y
M92	G-D	N	N	N	N	N	Y
	G-S	N	N	N	N	N	Y
	D-S	**Y**	**	**	**	**	Y
M97	G-D	**Y**	**	**	**	**	Y
	D-S	**Y**	**	**	**	**	Y
M98	G-S	**Y**	**	**	**	**	Y
	D-S	N	N	N	N	N	Y
M9	G-D	**Y**	**	**	**	**	Y
	G-S	N	N	N	N	N	Y
M10	G-S	**Y**	**	**	**	**	Y
M19	G-D	N	N	N	**Y**	N	Y
	G-S	**Y**	**	**	**	**	Y
M20	G-S	N	N	N	N	N	Y
	D-S	N	N	N	**Y**	N	Y

Notes: DM- Digital modelling
PSVC- Power Supply Voltage Control test technique
S- Source D- Drain G- Gate
N- Not Detected Y- Detected
**- No repetition for this test (as already detected by Digital modelling with initial 0 simulation set)

Table 5: Change operating region of faulty transistor when fault is introduced

Faulty Transistor	**Bias Point**		**%Vgs (Fault Free - Faulty)**	**%Vds (Fault Free - Faulty)**
	Faulty	**Fault Free**		
M276 (d-s)	Cutoff	Saturate	91.30%	91.30%
M429 (g-d)	Saturate	Linear	23.93%	-532.84%
M433 (g-d)	Saturate	Saturate	-44.63%	53.99%
Node 5 (M430)	Saturate	Saturate	99.99%	-45.00%
Node 22 (M435)	Linear	Linear	48.19%	>-1000%

Table 6: Overall CUT operating points for defects are exposed (by observing at - 0.300ms and 0.700ms)

Fault	**Operating Region**	**Fault occurred at:**					
		Resistor, (%)		**Comparator, (%)**		**Priority Encoder, (%)**	
		@#	&#	@#	&#	@#	&#
Narrow open	Saturate	≥|7.69|	≥|0.38|	-	-	-	-
	Linear /ohmic	≥|7.69|	≥|0.38|	-	-	-	-
	Cutoff	≥|23.08|	≥|0.38|	-	-	-	-
Short (power, ground, large resistive)	Saturate	≥|7.69|	≥|0.38|	≥|7.69|	≥|0.38|	-	≥|0.38|
	Linear /ohmic	≥|7.69|	≥|1.15|	≥|7.69|	≥|1.15|	-	≥|0.38|
	Cutoff	≥|15.38|	≥|0.77|	≥|7.69|	≥|0.77|	-	≥|0.38|

Notes: @# - Analogue modules (resistor and comparator)
&# - Digital module (priority encoder)

Table 7: Fault coverage for each defect at different observing points

Fault			**DM (sampling at 0.300ms and 0.700ms)**	**DM (observing at pulse transition)**
Large Resistive Short	M283	D-S	N	**Y ^$**
	M287	D-S	N	**Y ^**
	M428	D-S	N	**Y ^**
	M429	D-S	N	**Y ^**
	M223	D-S	N	**Y ^$**
	M92	G-S	N	**Y ^**
Narrow Open	M281	D	N	**Y ^$**
	M284	S	N	**Y ^$**
	M431	D	N	**Y ^$**
	M433	S	N	**Y ^$**
Short-to-GND	Node 19		N	**Y ^**
	Node 60		N	**Y ^**
Short-to-VDD	Node 6		N	**Y ^$**
	Node 8		N	**Y ^**
	Node 21		N	**Y ^**

	Node 62	N	Y ^

Notes: All test are introduced with 0 initial stimuli
^ - Fault detected at (500.06-500.24) us
$ - Fault detected at (1.00002-1.00015) ms

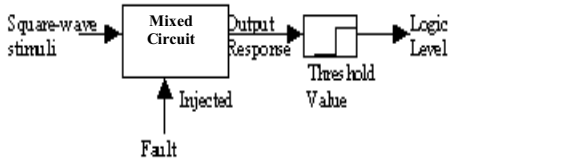


Fig. 1: Idea of Digital modelling

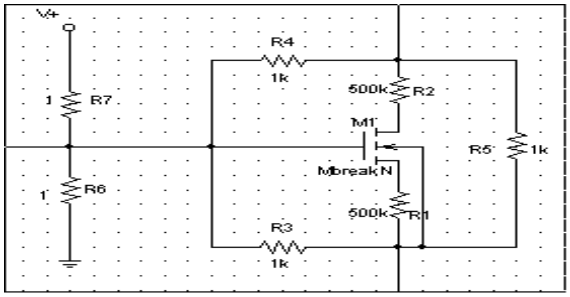


Fig 2: Transistor fault model

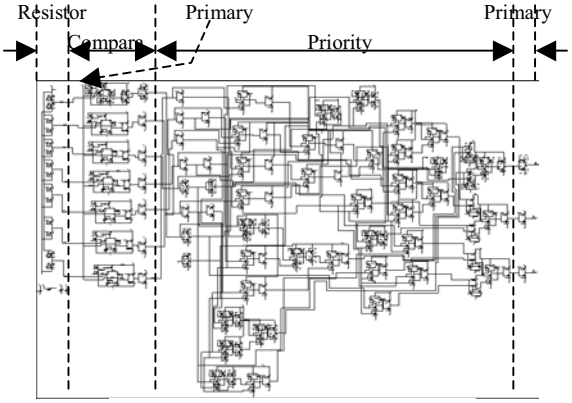


Fig. 3: CMOS level 3-bit Flash ADC

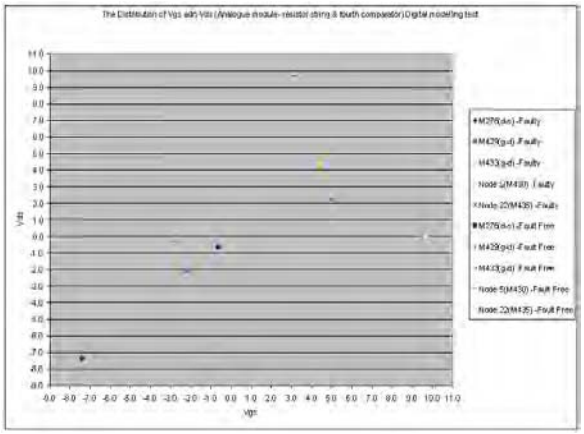
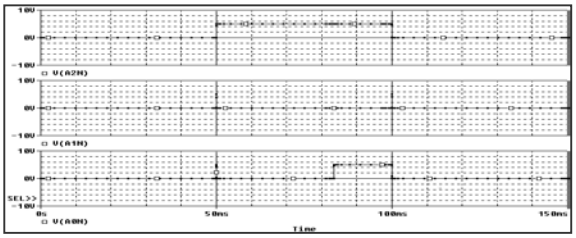
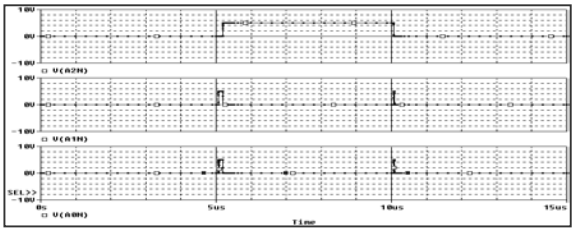


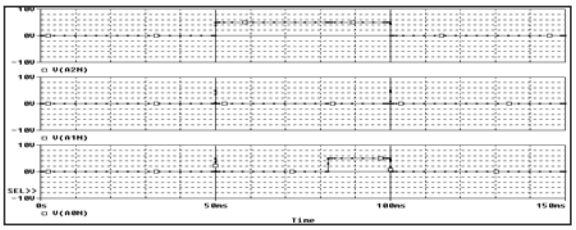
Figure 6: Distribution of Vgs and Vds for Digital modelling test (with initial stimuli logic 0) for faulty transistors



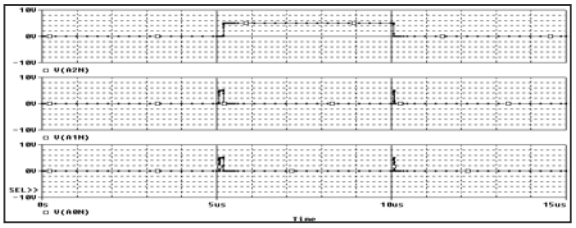
(a) Fault Free [10 Hz]



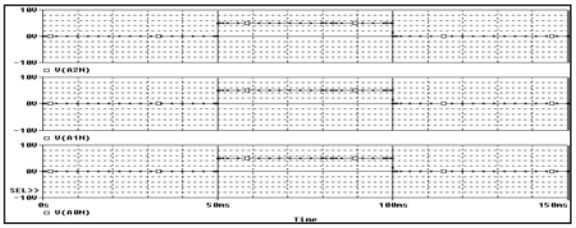
(b) Fault Free [100 kHz]



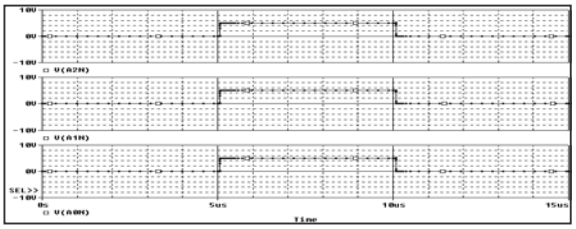
(c) Faulty M275 (D-S) [10 Hz], undetectable



(d) Faulty M275 (D-S) [100k Hz], undetectable

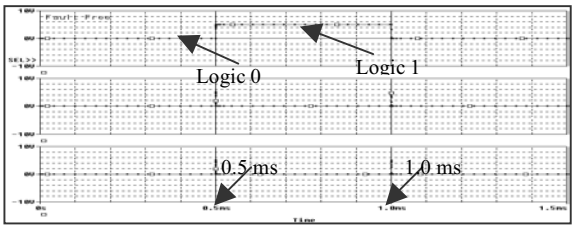


(e) Faulty M276 (D-S) [10 Hz], detectable

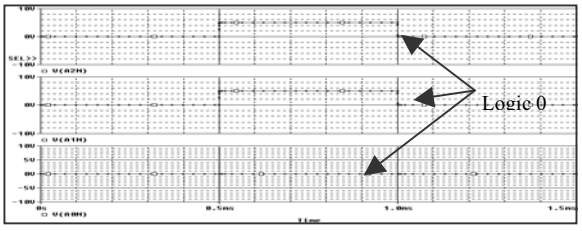


(f) Faulty M276 (D-S) [100k Hz], detectable

Figure 4: Output Response versus test frequency



(a) Fault Free [1 kHz]



(b) Faulty M278 (G-S) [1 kHz], detectable

Fig. 5: Output signature of M278 for fault free and faulty transistor