Design Approach for Tune able CMOS Active Inductor

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Abstract **A design approach for differential CMOS Active Inductor with a self-resonant frequency around 1.58GHz – 3.98GHz is presented. The architecture is based on a differential gyrator-C topology to transform intrinsic capacitance of a MOSFET to the emulated inductance. Due to high power consumption of Active Inductor, only a current source is used. This design has the capability to tune the inductor and Q-factor values from 10nH – 60nH and 20 – 60 respectively. Furthermore, a new technique is proposed to ensure smaller inductance value can be achieved with smaller power consumption and die area.**

I. INTRODUCTION

Active inductor has a major role to play in current situation in which compact designs with high performance are in demands. Furthermore, the capability to tune the inductance value with a moderate Q-factor has been a good advantage to the designer rather than to use passive inductors like spiral and bonding wire as they exhibits fix inductance value, poor Q-factor and require large die area. Therefore, active inductor could be a candidate to save die area and a solution for design reliability.

II. DESIGN OF ACTIVE INDUCTOR

A. Design Architecture

A differential gyrator-C is the key element to provide the inductance. This topology is capable to transform the intrinsic capacitance to the inductive behaviour [1]. A differential gyrator-C structure is depicted in Fig. 1.

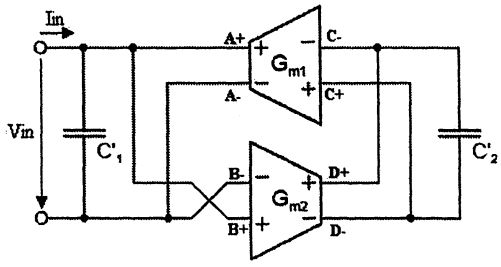

Fig 1: Differential gyrator-C Topology

From this architecture, the inductance value and the frequency response, f_0 are shown below:

$$L = \frac{C'_2}{G_{m1}G_{m2}} \quad (1)$$

$$f_o = \frac{1}{2\pi\sqrt{LC}} = \sqrt{\frac{G_{m1}}{C'_1}\frac{G_{m2}}{C'_2}} \quad (2)$$

where Gm_1 and Gm_2 are the transconductance and C_1' and C_2' are the parasitic capacitance from the circuit.

Based on (1), the inductance value can be tuned by increasing Gm_1 and Gm_2 or by decreasing C_2' to have smaller inductance and vise versa for bigger inductance. From (2), we can see L is very important to control the f_0.

B. Circuit Design

A circuit with bias network is depicted in Fig 2. A gyrator is realized by connecting two differential transconductance amplifiers back to back.

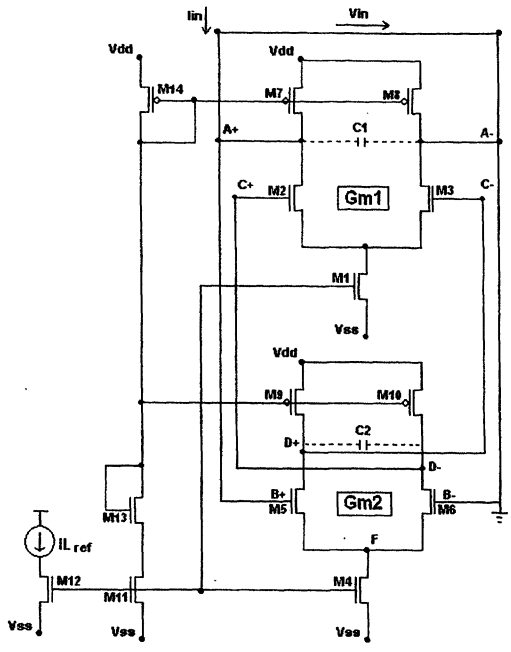

Fig 2: Schematic of the active inductor with bias circuit

The current source, I_L is realized by NMOS and PMOS current mirrors. This circuit is controlled by only 1 external current (I_{Lref}), compared to 3 external currents needed by [3]. This technique introduce smaller power consumption but sacrifice the Q-factor tune ability. Therefore, a good design is needed to make sure the Q-factor is high enough.

Compared to [2], this circuit uses a circuit topology to reduce current consumption in the negative resistance load and uses fewer current sources. This is realized by using PMOS current sources instead of PMOS load transistor. Transistors used as current sources provide lower output conductivity than load transistors. This design approach will lead to higher Q-factor.

C. Circuit Analysis

To analyze the circuit in Fig 2, all the transistors are modeled with equivalent circuit comprising the transconductance, g_m, the output conductivity, g_{ds}, and the capacitors, C_{gs}, C_{gd} and C_{db}. C_{db} is included as it is almost as large as C_{gs} for the short devices, used in this design.

To simplify the calculation, the model is simplified as shows in Fig 3 where $C_{1\&2}$ is the total effective capacitance between drain nodes of the amplifier stage 1&2 and ground. Parameter $g_{1\&2}$ is the effective output conductance at the drain node, the value of the negative conductance is taken into account and $gm_{1\&2}$ is the transconductance of the differential pair transistor in stage 1&2.

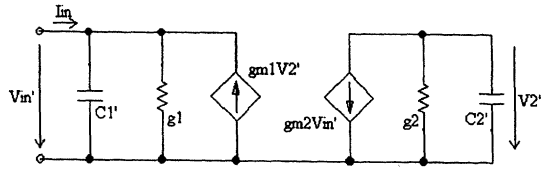

Fig 3: Small signal, half of the differential-mode equivalent circuit

With the equivalent circuit, the differential-mode input impedance is calculated as follows:

$$Zin = 2\frac{Vin'}{Iin}$$

$$= 2\frac{g2 + sC2'}{[\,gm1gm2 + g1g2\,] + s[\,g1C2'\,g2C1'\,] + s^2C1'C2'} \quad (3)$$

From equation (3), a simplified equivalent circuit of active inductor in differential model is shown in Fig 4.

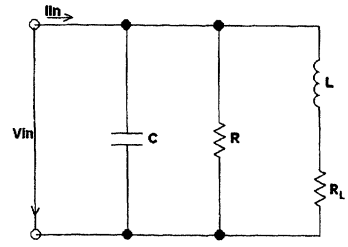

Fig 4: Simplified Active Inductor model

where C, R L and R_L elements represent as follow:

$$L = 2\frac{C2'}{gm1gm2} \quad (4)$$

$$R_L = 2\frac{g2}{gm1gm2} \quad (5)$$

$$R = 1/2(g1) \quad (6)$$

$$C = C1/2 \quad (7)$$

From (4), the inductance can be tuned via gm_1 and gm_2 which is related to the I_{Lref}. The Q-factor can be controlled to be as high as possible by decreasing g_2 and increasing gm_1 and gm_2.

III. DESIGN MOTIVATION

The main design motivation for active inductor is to achieve smaller inductance value with smaller power consumption. Based on (1) and (2), G_{m1} and G_{m2} play the major rule to control the inductance values. Therefore, I_{Lref} and $(W/L)_{2,\ 3,\ 5,\ 6}$ are the key point to have smaller inductance values. This method can be applied by increase the current and ratio of the selected transistor. However, this technique tends to increase power consumption and requires bigger area. Furthermore, it is very difficult to maintain the self-resonant frequency as f_0 is also related to G_{m1} and G_{m2}.

Therefore, a new technique is needed to achieved smaller inductance value with same f_0.

IV. PROPOSED SOLUTION

The simplest solution to the previous problem is by using a parallel active inductor, as depicted in Fig 6.

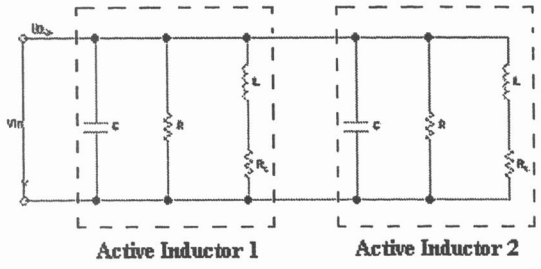

Fig 6 Parallel Active Inductor

$$\text{Parallel Active Inductor} = \frac{\text{Active Inductor 1}}{2} \ *$$

Furthermore, Q-factor and f_0 of the Parallel Active Inductor have the previous values. The analysis is discusses on the next section.

*Is true if Active Inductor 1 = Active Inductor 2

V. ANALYSIS AND RESULT

In this section, the result and analysis is divided into 2 section:

a. Active Inductor
b. Parallel Active Inductor

This analysis was done based on 1.2 μm AMI technology, provided by Mosis.

A. Active Inductor

For the simulation purposes, I_{Lref} is sweep from 600 μA to 2.9 mA to get the inductance and Q-factor values. To get an inductance of 10 nH, I_{Lref} is set to 2.9 mA. The DC current consumption of active inductor is 11.6 mA. Fig 7 shows the simulated impedance for 20 nH where the self resonance frequency of the active inductor is 3.98 GHz with Q=20.

If the current are reduced to I_{Lref} = 600 μA, an inductance value of 60 nH is achieved with a DC current consumption of 2.4 mA. The self-resonant frequency decreases to 1.58 GHz. However, Q-factor is increase to 60. The simulation for 60 nH is shown in Fig 8.

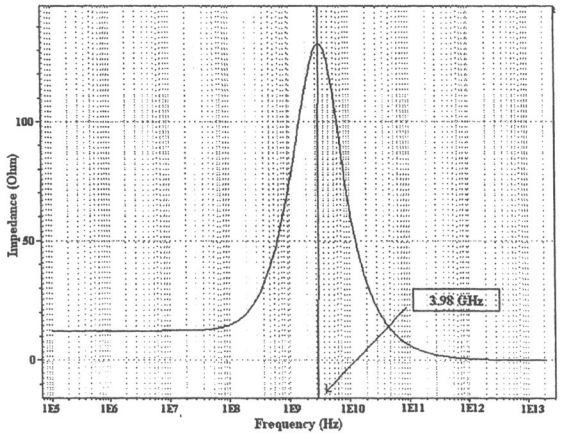

Fig. 7 Simulation result for 10 nH

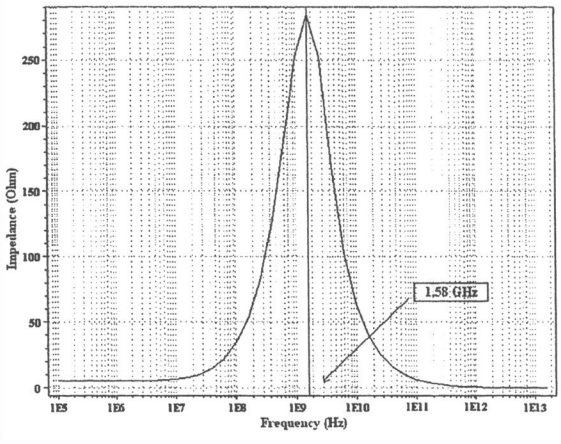

Fig. 8 Simulation result for 60 nH

Q-factor becomes smaller when I_{Lref} is increase, this is because I_{Lref} tend to increase output resistance (g_2). This matter can be proved using (8).

$$Q = \frac{2p\, f_0\, L}{R_L}$$

$$= \frac{2p\, f_0\, C_2}{g_2} \qquad (8)$$

Self-resonant frequency is also related to I_{Lref}. When I_{Lref} is increase, G_{m1} and G_{m2} become bigger and dominant to (2). This will cause increase in f_0. Therefore, it is quite difficult to have smaller inductance value with lower f_0.

The performance of the active inductor based on Fig 2 is shown below.

L-Tuning	10 nH – 60 nH
f_0	3.98 GHz – 1.58 GHz
Q-factor	20 – 60
Layout Area	360 µ x 210µ

B. Parallel Active Inductor

Parallel Active Inductor is a technique to overcome some of the previous problem.

To prove this statement, a 10 nH of Parallel Active Inductor will be designed. Two active inductors will be put in parallel. Each active inductor is powered by I_{Lef} = 1.2 mA, f_0 = 2.51 GHz, Q = 39 and inductance value of 20 nH. The simulation result is depicted below.

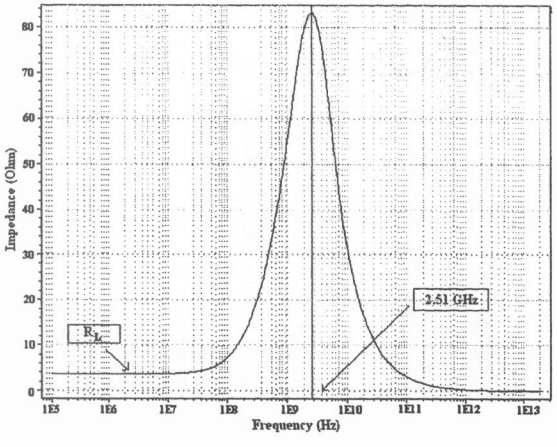

Fig 9 Simulation result for Parallel Active Inductor

From the simulation, we have successfully achieved inductance as small as 10 nH via calculation from the simulation result. Furthermore, it shows that f_0 still have the previous values, R_L is becoming smaller and tend to have better Q-factor = 42.7. The DC current consumption is also smaller, about 9.6 mA. However, this technique sacrifice die area(540µ x 210µ) as we need 2 active inductors.

To have a better comparison, a table to compare the result of Parallel Active Inductor and Active Inductor only is shown below.

	Parallel Active L	Active L
Inductance	10 nH	10 nH
f_0	2.51 GHz	3.98 GHz
Q-factor	42.7	20
DC Current	9.6 mA	11.6 mA
Area	540µx210µ	360µx210µ

A smaller inductance value with smaller power consumption and better Q-factor is achieved using this technique. Furthermore, lower inductance value with lower self-resonant frequency can be achieved.

VI. CONCLUSION

The design approach for CMOS active inductor is presented to achieve inductance tuning from 10 nH – 60 nH with Q= 20 - 60. The self resonant frequency for the active inductor is 1.58 GHz – 3.98 GHz with only 1 external current, I_{Lref}. Instead of discussing on the active inductor design, some design issues and design motivation are discussed briefly to ensure the targeted inductance value is achieved. Parallel Active Inductor is proved to have smaller inductance value, higher Q-factor, lower self-resonant frequency but sacrifice die area.

VII. REFERENCES

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