Single Carrier PWM Scheme for Cascaded Multilevel Voltage Source Inverter

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Abstract— **This work proposes a new switching scheme for the cascaded multilevel inverter. Unlike other schemes, the proposed method is based on the symmetric regular sampling PWM with a single carrier and multiple modulating signals. Non-transcendental trigonometric equations that define the switching instants of the multilevel inverter are derived. This algorithm is implemented by a low-cost fixed-point microcontroller on an experimental five-level cascaded inverter test-rig.**

Keywords—**modulation, multilevel inverter**

I. INTRODUCTION

The modulation control of multilevel inverter is quite challenging due to the complexity to cater for the transitions between the voltage levels (or steps).

The most popular method is based on the intersection of a single sinusoidal reference with N-1 triangular carriers, originally proposed by Carrara et.al [1]. Three alternative carrier disposition schemes are suggested, namely phase disposition (PD), alternative phase opposition disposition (APOD) and phase opposition disposition (POD).

Each of these variations has particular harmonic benefits, which have been argued elsewhere [2, 3]. While the literature on the modulation techniques for multilevel inverter can be considered extensive, it appears that no attempt is made to use a single carrier waveform.

This paper attempts to fill this gap by proposing a symmetric regular sampling PWM using a single carrier with multiple modulating signals. It outlines the principle of the modulation scheme and followed by the derivation trigonometric equations that define the PWM switching instants.

To validate the scheme, a prototype 5-level cascaded inverter is built where the proposed modulation scheme is implemented using a low-cost microcontroller.

II. THE PROPOSED MODULATION SCHEME

Fig. 1 shows an N-level, single-phase cascaded inverter. It consists of several single-phase H-bridge inverter modules with separate dc sources. The number of H-bridge module (M), depends on the number of levels (N) required and can be written as:

$$M=\frac{N-1}{2} \quad ; \text{N odd} \qquad (1)$$

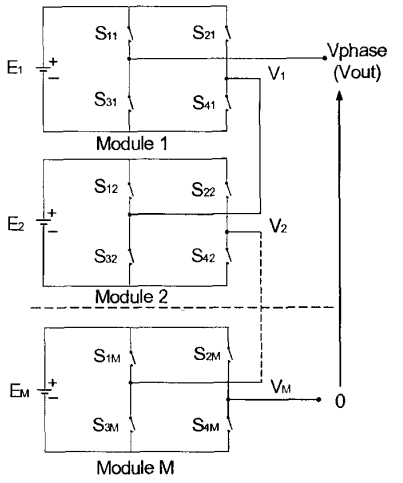


Fig. 1: Single-phase structure of a cascaded inverter.

By different combinations of S_{1M} through S_{4M}, each module can generate three different voltage outputs, i.e. +E, –E, and 0. The total output voltage is then constructed by the sum of the output voltage from each module. A five level inverter would have an output levels of +2E, +E, 0, –E, and –2E.

The proposed modulation scheme is based on the unipolar, symmetric PWM switching technique. It compares several modified sinusoidal modulation signals $s_u(k)$ with a single triangular carrier signal $c(k)$ as shown in Fig. 2. These modified modulation signals have the same frequency (f_o) and amplitude (A_m). Since the modulation is symmetric, the sinusoidal modulation signals are sampled by the triangular carrier signal once in every carrier cycle. The carrier signal is a train of triangular waveform with frequency f_c and amplitude A_c

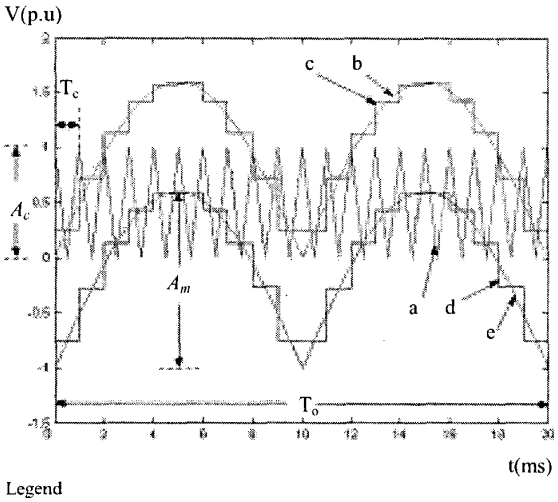
Intersection between the sampled modulation signals and the carrier signal defines the switching instant of the PWM pulses. In order to ensure quarter wave symmetry PWM output waveform, the starting point of the modulation signals ought to be phase shifted by one period of the carrier wave. Furthermore the modulation ratio must be even number. The number of modulation signals needed is equal to the number of modules (M) in the cascaded inverter.

Equations (2) and (3) define the modulation index and ratio, respectively for N-level inverter with M number of modules [1]:

$$m_i = \frac{A_m}{A_c} \cdot \frac{1}{\frac{(N-1)}{2}} = \frac{A_m}{MA_c} \quad (2)$$

$$m_f = f_c / f_o \quad (3)$$

The variable k represents a position of each modulated width pulses, initiated from k=1,2,3…m_f /2. Variable u=1,2..M represents which H–bridge module is being referred to.

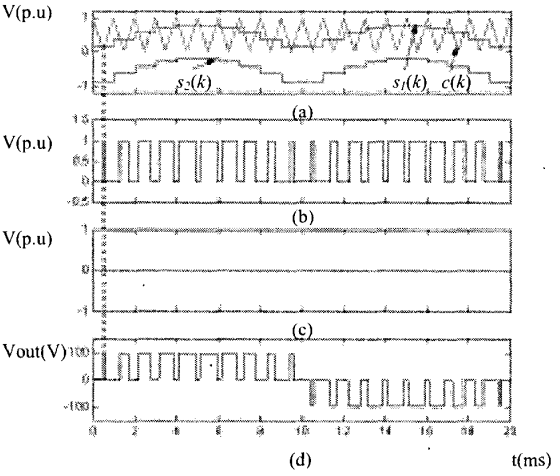


Legend
(a) Carrier signal $c(k)$, (b) Absolute sinusoidal modulation signal m_1 (t), (c) Modified sinusoidal modulation signal $s_1(k)$ of m_1 (t), (d) Shifted absolute sinusoidal modulation signal m_2 (t), (e) Modified sinusoidal modulation signal $s_2(k)$ of m_2 (t).

Fig. 2: The modified sinusoidal modulation signals and a single carrier signal.

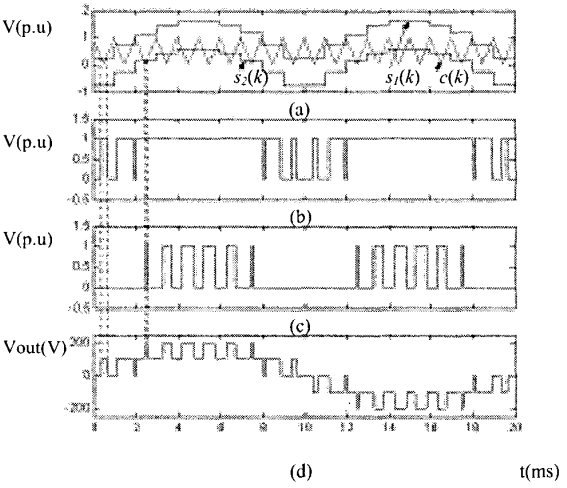
To illustrate the principle of the proposed scheme, a five-level inverter at m_i = 0.4 and m_i = 0.8 is shown in Fig. 3(a) and 3(b), respectively. For a five level output, u=2; hence two modulation signals namely $s_1(k)$ and $s_2(k)$ and single triangular carrier $c(k)$ are involved in the modulation process. The PWM pulses $V_1(k)$ is generated from the comparison between $s_1(k)$ and $c(k)$, while $V_2(k)$ is obtained from the comparison between $s_2(k)$ and $c(k)$. The comparison is designed such that if $s_1(k)$ is greater than $c(k)$, a pulse-width $V_1(k)$ is generated; if $s_2(k)$ is greater than $c(k)$, $V_2(k)$ is generated.

On the other hand if there is no intersection, then $V_1(k)$ and $V_2(k)$ remain at 0. It can be seen in Figure 3(a) that for $m_i \leq 0.5$, only $s_1(k)$ intersects with $c(k)$; no intersection occurs for $s_2(k)$. Therefore, $V_2(k)$ is zero. The output voltage V_{out}, which is the sum of $V_1(k)$ and $V_2(k)$, is then similar to the conventional three-level unipolar PWM case. For $m_i > 0.5$, as depicted in Figure 3(b), both modulating signal, i.e. $s_1(k)$ and $s_2(k)$ intersect the carrier and therefore $V_1(k)$ and $V_2(k)$ pulses are generated. As a result, a multilevel output voltage V_{out} is formed.



Legend
(a) Modulation signals and carrier signal; (b) PWM pulses produced from comparison between $s_1(k)$ and c(k), $V_1(k)$; (c) PWM pulses produced from comparison between $s_2(k)$ and $c(k)$, $V_2(k)$; (d) PWM output waveform, V_{out}.

Fig. 3(a): Principle of the proposed modulation scheme for m_i = 0.4, m_f = 20.



Legend
(a) Modulation signals and carrier signal; (b) PWM pulses produced from comparison between $s_1(k)$ and c(k), $V_1(k)$; (c) PWM pulses produced from comparison between $s_2(k)$ and $c(k)$, $V_2(k)$; (d) PWM output waveform, V_{out}.

Fig. 3(b): Principle of the proposed modulation scheme for m_i = 0.8 m_f = 20.

III. DERIVATION OF SWITCHING ANGLES

It is desirable to obtain mathematical expressions that define the switching instants for the inverter switches.

From the simulation carried out, it was found that simple equations could be developed from the proposed modulation scheme. The equations could be use to generate the PWM pulses on-line using digital technique.

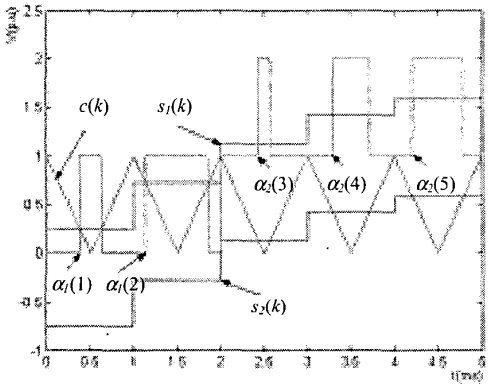


Fig. 4: Intersection between single carrier and modified sinusoidal modulation signals

The idea of mathematical derivation is to determine the point of intersection between single carrier and the sampled modulation signals. Referring to Fig. 4, the single carrier and two set of sampled modulation signals in generating five-level inverter output voltage for m_a = 0.8, m_f = 20. Due to symmetrical nature of the proposed PWM scheme, the intersection between the positive slope carrier $c_k^+(t)$ and the modulating signals is not required in the derivation. It can be deduced from the rising edge equation. While, the straight-line equation for the carrier wave is denoted by $c_k^-(t)$ for the negative slope. It can be expressed as:

$$c_k^-(t) = \left(\frac{-A_c}{\frac{T_c}{2}} \right) \alpha_k + hA_c \qquad k = 1,2,3.... \text{ and } h = 1,3,5.... \quad (4)$$

The modulation signals can be described as

$$s_{1k}(t) = A_m \sin\left[\omega(i) + \frac{\pi}{m_f} \right]; \quad s_{2k}(t) = A_m \sin\left[\omega(i) + \frac{\pi}{m_f} \right] - A_c \quad (5)$$

$i = 0,1,2,3.... \rightarrow$ when intersect with $c_k^-(t)$

Where the angular frequency ω, in (5) is

$$\omega = 2\pi f_o \times \frac{T_o}{m_f} = \frac{2\pi}{m_f} \quad (6)$$

After some mathematical manipulation and simplification, a generalized equation that describes the switching instants produces, i.e.:

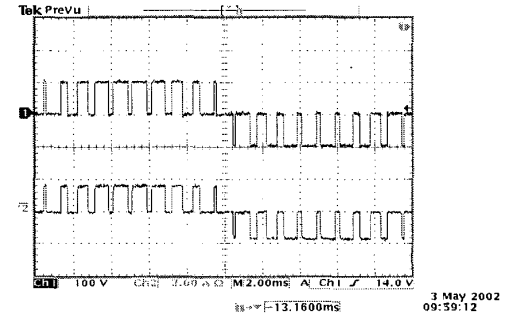
$$\alpha_u(k) = \frac{T_c}{2}\left[(2k+u-2) - \frac{A_m}{A_c} \sin\left(\omega(k-1) + \frac{\pi}{m_f} \right) \right] \quad (4)$$

Equation (4) can be used to generate the k^{th} PWM pulses for a cascaded inverter of any level N.

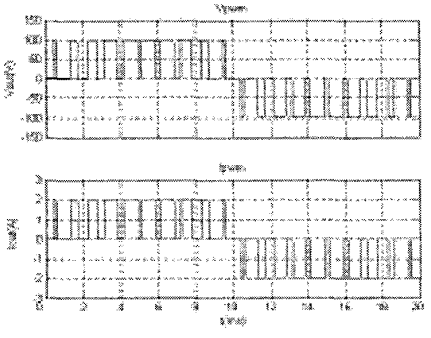
IV RESULTS

A five-level experimental rig is built to implement the proposed modulation technique. The inverter input voltages are fixed at 100V dc for each H-bridge module and the load is a purely resistive. The generation of the PWM pulses is implemented using a relatively simple, 16-bit fixed-point microcontroller (SIEMENS SAB-C167CR-LM). A MATLAB-Simulink block simulation is also carried out to substantiate the results.

Fig. 5 shows the oscillogram of the output voltage and current of the inverter for m_i = 0.4 and m_f = 20. As can be observed, the output voltage is similar to a three-level inverter, because $m_i \leq 0.5$. For the case of m_i = 0.8 and m_f = 20 shown in Fig. 6, the five-level PWM waveform is obtained. These results are consistent with the theoretical predictions shown by the MATLAB simulation plots.



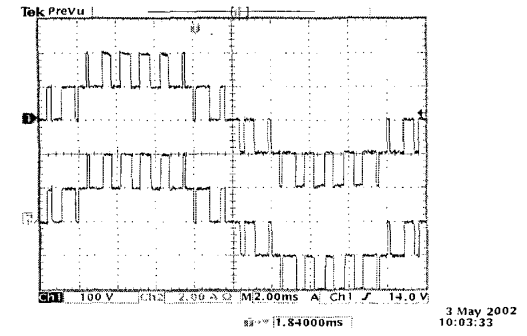
(a)



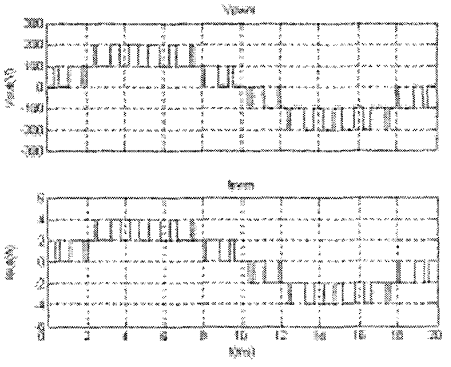
(b)

Top trace: Output voltage. Vertical scale 100V/div.
Bottom trace: Output current. Vertical scale 2A/div.Horizontal scale 2ms/div.

Figure 5 (a): Practical result for m_i = 0.4; m_f = 20. (b) Simulation



(a)



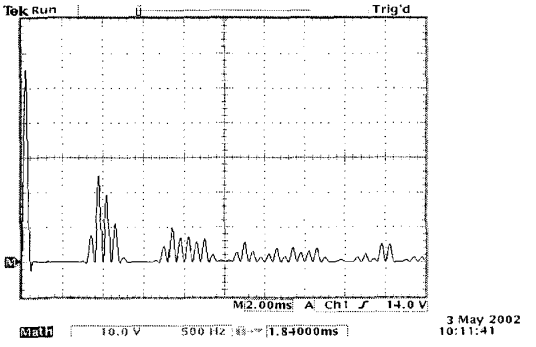
(b)

Top trace: Output voltage. Vertical scale 100V/div.
Bottom trace: Output current. Vertical scale 2A/div.Horizontal scale 2ms/div.

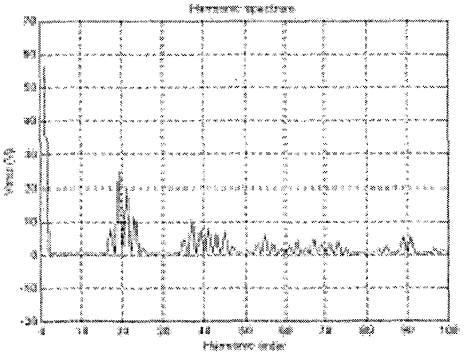
Figure 6 (a): Practical result for m_i = 0.8; m_f = 20. (b) Simulation

For the case of m_f = 20 and m_i = 0.4, the practical result of output voltage harmonic spectrum are shown in Fig. 7(a). The theoretical spectrum for the similar case is shown in Fig. 7(b). By comparing Fig. 7(a) and Fig. 7(b), it can be clearly observed that the harmonics incidences for $m_i \leq 0.5$ agree closely with theoretical predictions. The proposed modulation scheme produces only odd harmonics for even modulation ratio. Furthermore, harmonics at the carrier and the multiples of carrier frequency do not exist at all.

The practical and simulation output voltage harmonic spectrum for the case of m_f = 20; m_i = 0.8 are illustrated in Fig. 8(a) and 8(b), respectively. Note that for five-level inverter, m_i = 0.4 is "equivalent" to m_i = 0.8 for a three-level inverter. For an equivalent modulation index, the significant harmonic of a five-level is half compared to a three-level inverter.



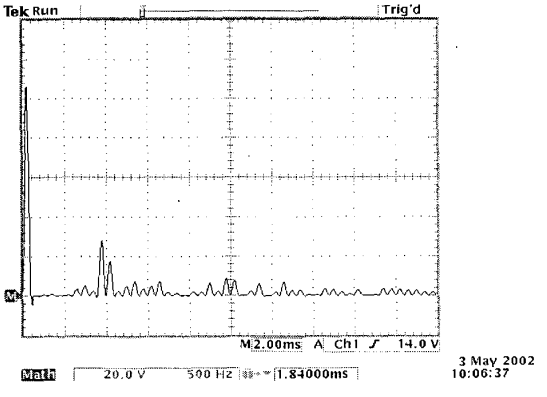
(a)



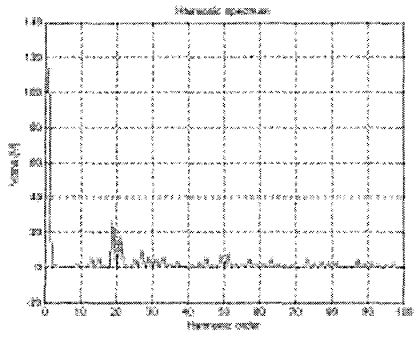
(b)

Vertical scale 10V/div.
Horizontal scale 500Hz/div.

Figure 7 (a): Practical harmonic spectrum of output voltage for m_i = 0.4; m_f = 20. (b) Simulation.



(a)



(b)

Vertical scale 10V/div.
Horizontal scale 500Hz/div.

Figure 8 (a): Theoretical harmonic spectrum of output voltage for m_i = 0.8; m_f = 20. (b) Simulation.

Figure 9 shows the comparison the harmonic profile of the proposed modulation technique with the POD scheme (using symmetrical regular sampling PWM). It can be observed that the proposed technique produces an identical spectrum to the POD scheme for all major harmonics. It can be suggested that both strategies produce harmonic components of the same magnitudes and frequencies despite the obvious difference between the two modulation principles.

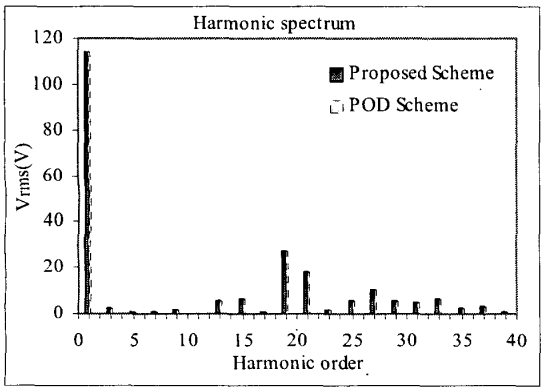


Figure 9: Comparison of harmonic spectrum between the proposed scheme and POD scheme.

V CONCLUSION

This paper presents a new switching scheme for a cascaded inverter. The proposed scheme is based on symmetric regular sampled unipolar PWM, with multiple modulating waveforms and a single carrier. Mathematical equations that define the PWM switching instants is derived and verified by hardware test rig. The derived equations are implemented by a low-cost fixed-point microcontroller. Several tests to quantify the performance of the inverter under the proposed modulation scheme. From the results it can be concluded that the harmonics performance of the proposed scheme is very identical to the POD scheme.

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