Study on the Performance of the Boost Power Factor Correction (PFC) circuit with Variable Inductor Current Sense Resistor values

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Abstract—**A Power Factor Correction (PFC) circuit using Boost converter for low power applications are developed and analyzed in this work. Simulation is done on the Boost PFC circuit using average current mode control to validate the designed parameters. The experimental circuit is developed so that the results can be verified and compared with the simulation results. The effect of the inductor current sense resistor to the performances of the circuit in terms of efficiency, power factor and input current THD are highlighted. In addition, the dynamic response of the output voltage and input current are presented**

Keywords—**Boost PFC, sense resistor, margins**

I. INTRODUCTION

Nowadays, power electronics circuits has become one of the most important design part in most commonly used electrical equipments namely the computers, televisions, motor drives, electronics ballast and power amplifiers. It is a well known fact that most of the equipments require AC to DC conversions from the AC mains. The DC voltage from the conversion must contain low ripple voltage and thus a bulk capacitor is used as a filter. As a consequence, the input current waveform from the mains is non-sinusoidal with high peak pulsating current and contains low order harmonic currents [1]. These harmonic currents cause several problems such as voltage distortion and fluctuation at point of common coupling (PCC), overheating, and noise as well as reduce the capability of the line to provide energy [2].

To cope with these problems the most suitable and reliable solutions for low power applications is the active power factor corrections (PFC) circuit. For most PFC circuit topologies as presented in [3,4], the Boost type PFC performs much better than other circuits in terms of efficiency, power factor and the simplicity of gate drive circuit. Besides that, the inductor that is located at the front of the circuit would give a smooth input current.

Several control techniques that are commonly used as feedback control circuitries are presented in [5,6]. Among them, the average current mode control is typically selected to control the PFC circuit due to several advantages namely constant switching frequency, less sensitive to commutation noise and simple inductor current sensing [5]. Fig. 1 shows the circuit diagram of the Boost PFC circuit using average current mode control. Several previous papers have presented some analysis on the Boost PFC circuit but none mentioned the appropriate value of the sense resistor that must be utilized in the Boost PFC circuit design.

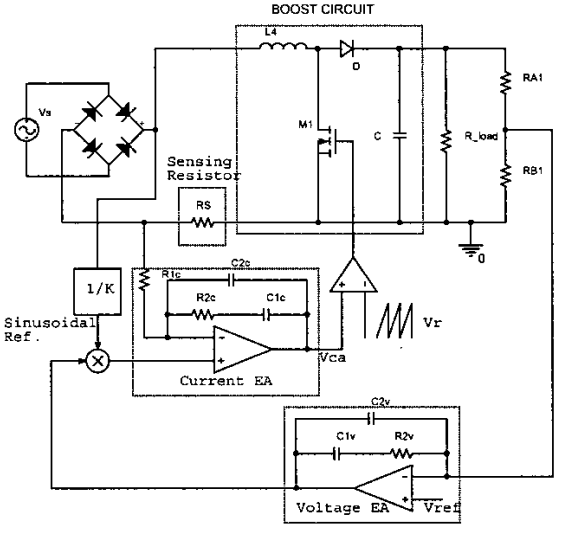

Fig. 1: Boost PFC circuit with average current mode control

This paper presents an analysis on a PFC circuit performance in terms of power factor, efficiency, input current THD and dynamic response by varying the sense resistor values. A simulation using PSpice is conducted for the averaged and switch model to initially study the behavior of the circuit. The designed parameters and simulation results are verified and compared with the results from the experimental circuit. The efficiency, power factor and input current THD are analyzed by varying the inductor current sensing resistor for different loads conditions. A set of sense resistor value is recommended depending on the requirement of the circuit.

II. ANALYSIS

The design procedures of average current mode control as mentioned in [8, 9, 10] is discussed briefly here especially for the current loop. One of the most important parts in designing a PFC circuit using average current mode control is the placement of the pole and zero for the

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current and voltage error amplifier. The transfer function of the error amplifier with the compensator presented in Fig. 2 is as follows,

$$G(s)=\frac{1}{R_1C_2}\cdot\frac{s+\omega_Z}{s(s+\omega_P)} \quad (1)$$

where, $\omega_Z=\frac{1}{R_2C_1}$; and $\omega_P=\frac{C_1+C_2}{R_2C_1C_2}$.

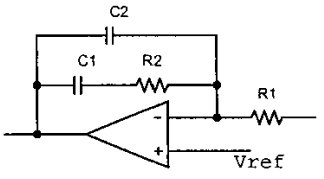

Fig. 2: Error amplifier with compensator

Referring to (1), it is clearly stated that the error amplifier circuit consist of an integrator (1/s), one zero at ω_Z and one pole at ω_P. Although the current and voltage error amplifier circuit implements the same type of error amplifier, the requirement for each pole and zero placement is totally different. The integrator normally eliminates the steady state error. The zero that is placed before the frequency of the power stage filter (actually lower than half of the switching frequency) ensures the stability of the current loop. The pole eliminates the high frequency noise.

Furthermore, the current error amplifier must be set to operate at large bandwidth [7] so that the dynamic response of the input current is better and faster. The cutoff frequency of the current loop is determined by the current error amplifier gain and the control to input gain derived in [9]. The maximum current error amplifier gain is,

$$G_{CA}=\frac{V_S f_S L}{V_O R_S} \quad (2)$$

The control to input gain is,

$$G_{CI}=\frac{R_S V_O}{V_S sL} \quad (3)$$

where, V_S is the switching ramp peak voltage, f_S is the switching frequency, L is the inductor, V_O is the output voltage and R_S is the sense resistor. It is known that at cutoff frequency the overall gain is zero, which is presented as

$$20\log(G_{CA}G_{CI})=0 \quad (4)$$

Solving for $G_{CA}G_{CI}$,

$$G_{CA}G_{CI}=1 \quad (5)$$

To obtain the overall gain of the circuit, equation (2) and (3) is substituted to (5). By equating $s = 2\pi f_C$ in (3), the cutoff frequency, f_C is set to $f_S/2\pi$.

As can be seen in (2), the current error amplifier gain, G_{CA}, is inversely proportional to the sense resistor, R_S, but the control to output gain, G_{CI}, is proportional to R_S. Thus, when R_S is small, G_{CA} is large. The disadvantage of this is that the noise signal would be amplified and consequently distorts the error signal. As a result, the gate signal too contains the noise signal and thus affects the wave shape of the inductor current. On the other hand, when R_S is small, the gain G_{CA} is also small and the effect on the noise signal is not significant to the error signal and the gate signal. Therefore, a better input current waveform is obtained. This effect is significant especially when the input current is relatively small (low output power) in a range of a few hundred mA.

III. Simulation And Experimental Results

The circuit is analyzed according to several conditions and characteristics, which are:

i. Simulations with average and switch model
ii. Experimental results for 100W and 400W load
iii. Performance in terms of efficiency, power factor and current THD
iv. Dynamic response

In this circuit, the parameters used are V_{IN}=240Vrms, V_O=380Vdc, f_S=60kHz, L=450μH, C=330μF. The parameters are selected based on the requirement of the output voltage value and ripple, inductor current ripple using appropriate equations and design procedures made by previous papers [8]-[10].

Firstly, the designed parameters of the Boost PFC circuit are validated with simulation using the average and switch model. The results for the simulation part are presented in the form of waveforms for input voltage, input current and output voltage. Fig. 3 shows the simulation results using the average and switch model with a load of 400W. The simulation results using both methods show reasonable relation and thus it can validate the parameters used in the circuit.

In Fig. 4, the input voltage and input current waveforms for a 100W load is presented. It can be seen that the sinusoidal wave shape of the input current is better when R_S is 0.3Ω compared to when R_S is 0.05Ω. The difference between the input current waveform for both cases is very significant. The input current for R_S = 0.3Ω is highly distorted compared with R_S = 0.05Ω. When the load is increased to 400W, the input current wave shape for R_S = 0.3Ω is still better than when R_S = 0.05Ω as shown in Fig. 5.

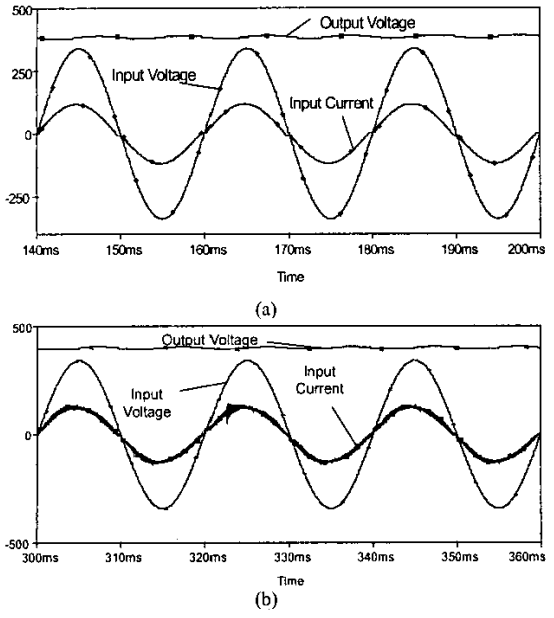

Fig. 3: The waveforms for input voltage, input current and output voltage based on simulation (a) averaged model (b) switch model.

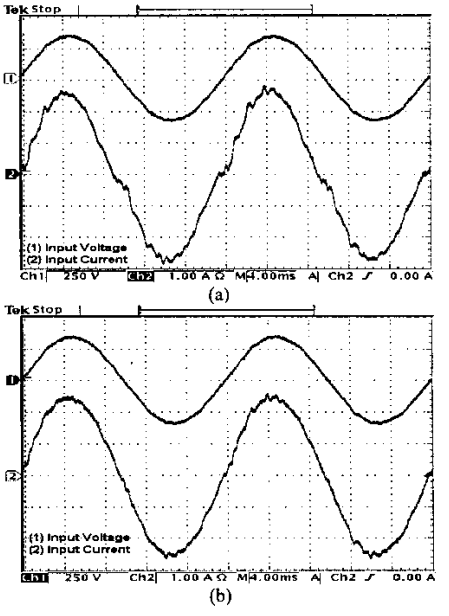

Fig. 5: Input voltage (250V/div) and input current (1A/div) waveforms for a 400W load, (a) $R_S = 0.05\Omega$, (b) $R_S = 0.3\Omega$

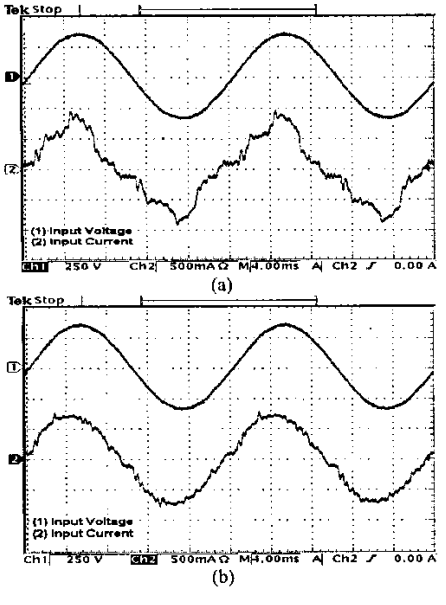

Fig. 4: Input voltage (250V/div) and input current (0.5A/div) waveforms for a 100W load, (a) $R_S = 0.05\Omega$, (b) $R_S = 0.3\Omega$

The dynamic response of the input current and output voltage are shown in Figure 6. With the same setting of the voltage and current loop, it can be clearly seen that the dynamic response for $R_S = 0.3\Omega$ is much better than $R_S = 0.05\Omega$. In Fig. 6(a); when $R_S = 0.05\Omega$, the output voltage attempts to maintain at 380V DC when the load is changed from 200W to 400W and due to noise signal, the dynamic response is quite severe. The same situation occurs with the input current that attempts to maintain the sinusoidal waveform but unfortunately a few high peak current is generated for a few cycles. The input current takes about a few hundred milliseconds to recover and become stable with the required sinusoidal waveform. In Fig. 6(b); when $R_S = 0.3\Omega$, the output voltage and input current waveform change smoothly and quickly for the same step load change.

The efficiency of the PFC circuit is the best when R_S is chosen between 0.2Ω and 0.25Ω as shown in Fig. 7. The efficiency for the 300W load seems to decrease when $R_S = 0.3\Omega$. On the other hand, in order to obtain a better power factor, $R_S = 0.3\Omega$ is the best choice as shown in Fig. 8. The input current THD is the lowest for all load conditions when $R_S = 0.3\Omega$ as shown in Fig. 9.

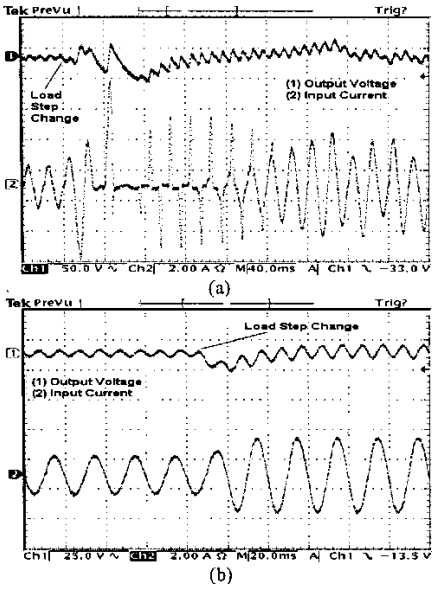

Fig. 6: Output voltage and input current dynamic response (200W to 400W), (a) $R_S = 0.05\Omega$, (b) $R_S = 0.3\Omega$.

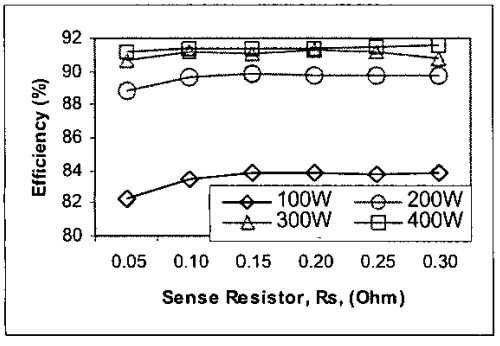

Fig. 7: The efficiency of the circuit with respect to the sense resistor value

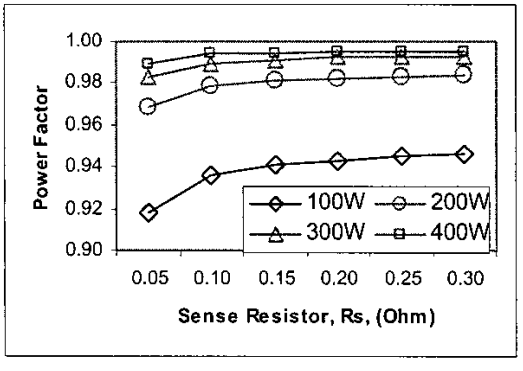

Fig. 8: Power factor of the circuit with respect to the sense resistor value

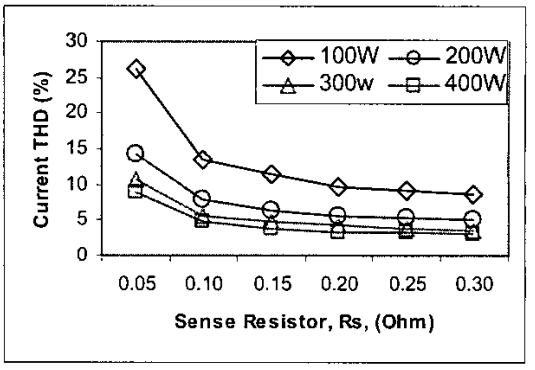

Fig. 9: The percentage of the input current total harmonic distortion (THD) of the circuit with respect to the sense resistor value

IV. Conclusion

The effects of several sense resistor values to the efficiency, power factor, and current THD of a Boost PFC circuit are analyzed. A suitable value of sense resistor is identified and utilized in order to obtain better circuit performance. From the results that have been analyzed, the recommended value of the sense resistor, R_S, is between 0.2Ω and 0.3Ω for better performance. Choosing a bigger value of R_S will result in the demeaning of the circuit efficiency.

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