An Alternative PWM Scheme for Multilevel Voltage Source Inverter

J. Aziz and Z. Salam

Abstract--**This work proposes an alternative PWM scheme for cascaded multilevel inverter. The scheme is based on symmetric regular sampled unipolar PWM, with multiple modulating waveforms and a single carrier. Mathematical equations that define the PWM switching instants are derived and implemented digitally using a low-cost microcontroller. A five-level cascaded multilevel inverter test-rig is built to prove viability of the proposed algorithm.**

Keywords--**Harmonics, Modulation strategies, Multilevel Inverter, Renewable energy systems.**

I. Introduction

Multilevel voltage source inverter offers several advantages that make it preferable over the conventional (two-level) voltage source inverter (VSI). These include the possible utilisation of higher DC link voltage, improved harmonics performance and reduced power devices stress.

The development of multilevel inverter began in the early 1980's when Nabae et al. [1] proposed the neutral-point clamped (NPC) PWM inverter. Since then several multilevel topologies, namely the diode-clamped, the flying capacitors, the cascaded multilevel and recently hybrid multilevel inverter [2], have evolved and applied in adjustable speed drives, electric utility and renewable energy systems.

Although multilevel inverter offers several advantages, the modulation control of multilevel inverter is quite challenging due to the complexity to cater for the transitions between the voltage levels (or steps).

The most popular method is based on the intersection of a single sinusoidal reference with N-1 triangular carriers, originally proposed by Carrara et.al [3]. Three alternative carrier disposition schemes are suggested, namely phase disposition (PD), alternative phase opposition disposition (APOD) and phase opposition disposition (POD). Each of these variations has particular harmonic benefits, which have been argued elsewhere [4, 5].

While the literature on the modulation techniques for multilevel inverter can be considered extensive. It seems to be inadequate description on how a particular modulation can be implemented effectively on a digital system, except for the work published by Dell'Aquilla et.al. [6]. The authors implement asymmetrical regular sampling PWM on a DCMI topology using the APOD scheme. However it was discovered that this PWM strategy results in inherent "jump" in more than one level of the output voltage during the level transition.

These level jumps seriously distorts the output voltage waveform and hence its harmonics. The same authors proposed software solutions to avoid these unnecessary conditions but the proposed correction is quite complicated and its implementation is cumbersome.

Furthermore, it appears that no attempt is made to use multiple modulating waveform modulated with a single carrier. This paper attempts to fill this gap by proposing a symmetric regular sampling PWM using a single carrier with multiple modulating signals. It outlines the principle of the modulation scheme and followed by the derivation trigonometric equations that define the PWM switching instants. To validate the scheme, a prototype 5-level cascaded inverter is built where the proposed modulation scheme is implemented using a low-cost microcontroller.

II. The Proposed Modulation Scheme

Fig. 1 shows an N-level, single-phase cascaded inverter. It consists of several single-phase H-bridge inverter modules with separate dc sources. The number of H-bridge module (M), depends on the number of levels (N) required and can be written as:

$$M=\frac{N-1}{2};\ N \text{ odd} \qquad (1)$$

By different combinations of S_{1M} through S_{4M}, each module can generate three different voltage outputs, i.e. +E, −E, and 0. The total output voltage is then constructed by the sum of the output voltage from each module. A five level inverter would have an output levels of +2E, +E, 0, −E, and −2E.

The proposed modulation scheme is based on the unipolar, symmetric PWM switching technique. It compares several modified sinusoidal modulation signals $s_u(k)$ with a single triangular carrier signal $c(k)$ as shown in Fig. 2. These modified modulation signals have the same frequency (f_o) and amplitude (A_m). Since the modulation is symmetric, the sinusoidal modulation signals are sampled by the triangular carrier signal once in every carrier cycle. The carrier signal is a train of triangular waveform with frequency f_c and amplitude A_c.

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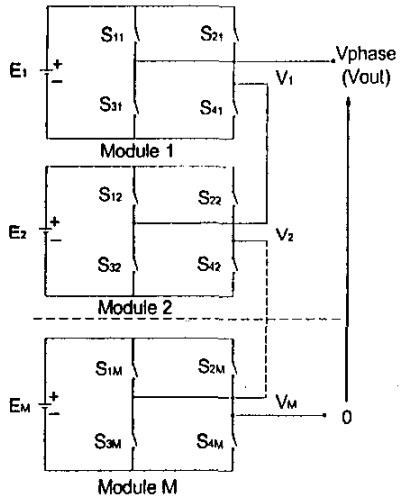


Fig. 1: Single-phase structure of a cascaded inverter.

Intersection between the sampled modulation signals and the carrier signal defines the switching instant of the PWM pulses. In order to ensure quarter wave symmetry PWM output waveform, the starting point of the modulation signals ought to be phase shifted by one period of the carrier wave. Furthermore the modulation ratio must be even number. The number of modulation signals needed is equal to the number of modules (M) in the cascaded inverter.

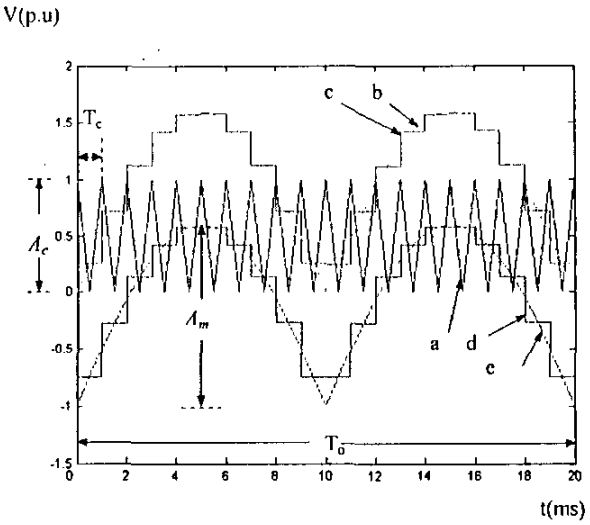
Equations (2) and (3) define the modulation index and ratio, respectively for N-level inverter with M number of modules [1]:

$$m_i = \frac{A_m}{A_c} \cdot \frac{1}{\frac{(N-1)}{2}} = \frac{A_m}{MA_c} \tag{2}$$

$$m_f = f_c / f_o \tag{3}$$

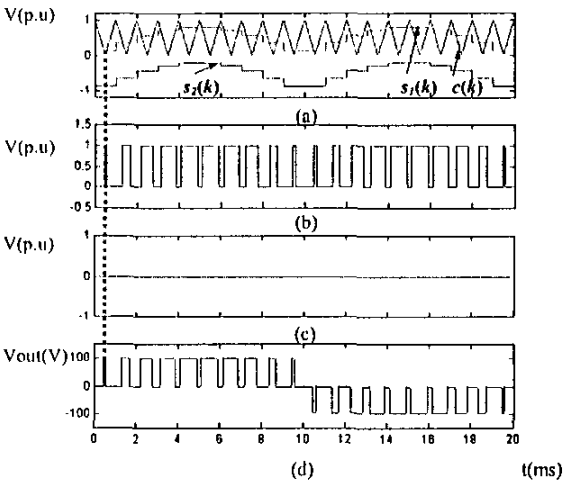
The variable k represents a position of each modulated width pulses, initiated from k=1,2,3…m_f /2. Variable u=1,2..M represents which H–bridge module is being referred to.

To illustrate the principle of the proposed scheme, a five-level inverter at m_i = 0.4 and m_i = 0.8 is shown in Fig. 3(a) and 3(b), respectively. For a five level output, u=2; hence two modulation signals namely $s_1(k)$ and $s_2(k)$ and single triangular carrier $c(k)$ are involved in the modulation process. The PWM pulses $V_1(k)$ is generated from the comparison between $s_1(k)$ and $c(k)$, while $V_2(k)$ is obtained from the comparison between $s_2(k)$ and $c(k)$. The comparison is designed such that if $s_1(k)$ is greater than $c(k)$, a pulse-width $V_1(k)$ is generated; if $s_2(k)$ is greater than $c(k)$, $V_2(k)$ is generated.



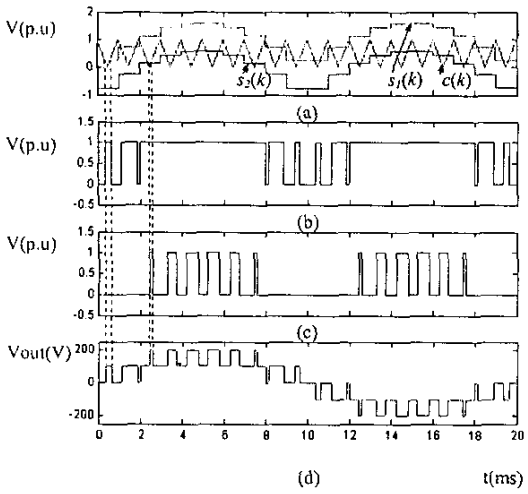
Legend
(a) Carrier signal $c(k)$; (b) Absolute sinusoidal modulation signal m_1 (t); (c) Modified sinusoidal modulation signal $s_1(k)$ of m_1 (t); (d) Shifted absolute sinusoidal modulation signal m_2 (t); (e) Modified sinusoidal modulation signal $s_2(k)$ of m_2 (t).

Fig. 2: The modified sinusoidal modulation signals and a single carrier signal.



Legend
(a) Modulation signals and carrier signal; (b) PWM pulses produced from comparison between $s_1(k)$ and c(k), $V_1(k)$; (c) PWM pulses produced from comparison between $s_2(k)$ and $c(k)$, $V_2(k)$; (d) PWM output waveform, V_{out}.

Fig. 3 (a): Principle of the proposed modulation scheme for m_i = 0.4, m_f = 20.



Legend
(a) Modulation signals and carrier signal; (b) PWM pulses produced from comparison between $s_1(k)$ and c(k), $V_1(k)$; (c) PWM pulses produced from comparison between $s_2(k)$ and $c(k)$, $V_2(k)$; (d) PWM output waveform, V_{out}.

Fig. 3 (b): Principle of the proposed modulation scheme for $m_i = 0.8$ $m_f = 20$.

On the other hand if there is no intersection, then $V_1(k)$ and $V_2(k)$ remain at 0. It can be seen in Figure 3(a) that for $m_i \leq 0.5$, only $s_1(k)$ intersects with $c(k)$; no intersection occurs for $s_2(k)$. Therefore, $V_2(k)$ is zero. The output voltage V_{out}, which is the sum of $V_1(k)$ and $V_2(k)$, is then similar to the conventional three-level unipolar PWM case. For $m_i > 0.5$, as depicted in Figure 3(b), both modulating signal, i.e. $s_1(k)$ and $s_2(k)$ intersect the carrier and therefore $V_1(k)$ and $V_2(k)$ pulses are generated. As a result, a multilevel output voltage V_{out} is formed.

In general, for a N-level inverter there are M modulating waveform, which corresponds to M number of H-bridge modules. The transition level (or the inverter output voltage step) is determined by the modulation index in the following manner: For a N-level inverter, the nth level transitions occur at:

$$m_i = \frac{n}{M} \quad (4)$$

where n=1...M-1.

For example for a 9 level inverter, N=9; therefore M=4. The transition occurs when the modulation index m_i reaches 0.25, 0.5 and 0.75. Note that the definition of modulation index used in this discussion is given by (2).

The expression for the kth switching instants, i.e the intersections of the carrier and the modulating signals for any number of N level cascaded inverter can be described as:

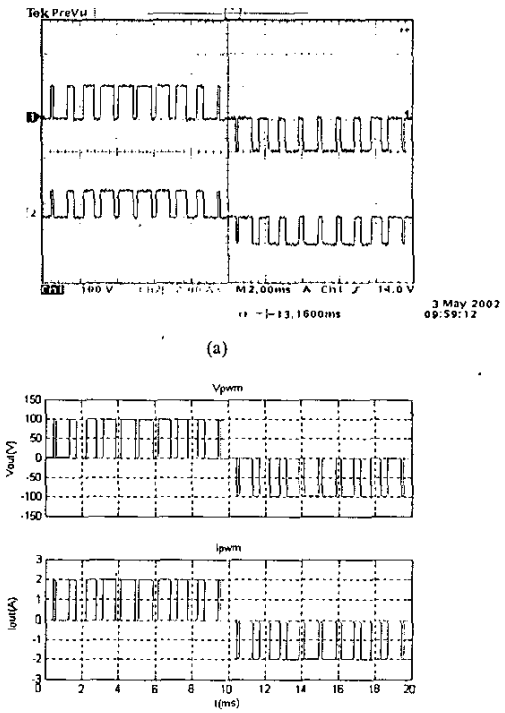
$$\alpha_u(k) = \frac{T_c}{2}\left[(2k+u-2) - \frac{A_m}{A_c}\sin\left(\omega(k-1) + \frac{\pi}{m_f}\right)\right] \quad (5)$$

Where u=1,2..M. Equation (5) can be used to generate the kth PWM pulses for a cascaded inverter of any level N. Note that the variable u correspond to the particular H-bridge module that the switching will be subjected on. It follows that α_u is the switching angle for the kth pulse of a particular bridge module. It can also be noted that this general equation is non-transcendental and its practical implementation using a simple microcontroller is therefore possible.

III. Results

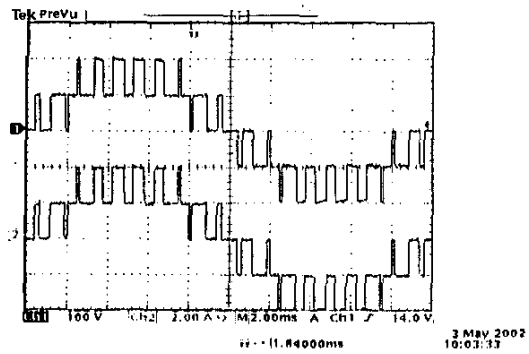
A five-level experimental rig is built to implement the proposed modulation technique. The inverter input voltages are fixed at 100V dc for each H-bridge module and the load is a purely resistive. The generation of the PWM pulses is implemented using a relatively simple, 16-bit fixed-point microcontroller (SIEMENS SAB-C167CR-LM). A MATLAB-Simulink block simulation is also carried out to substantiate the results.

Fig. 4 shows the oscillogram of the output voltage and current of the inverter for $m_i = 0.4$ and $m_f = 20$. As can be observed, the output voltage is similar to a three-level inverter, because $m_i \leq 0.5$. For the case of $m_i = 0.8$ and $m_f = 20$ shown in Fig. 5, the five-level PWM waveform is obtained. These results are consistent with the theoretical predictions shown by the MATLAB simulation plots.

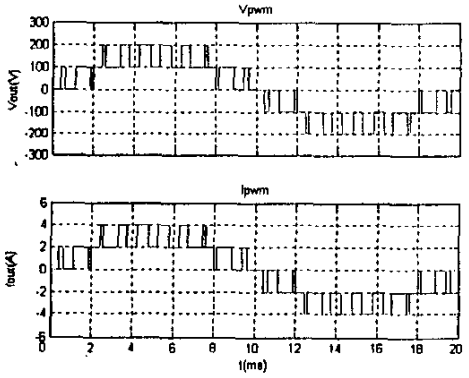


Top trace: Output voltage. Vertical scale 100V/div.
Bottom trace: Output current. Vertical scale 2A/div.Horizontal scale 2ms/div.

Fig. 4 (a): Practical result for $m_i = 0.4$; $m_f = 20$. (b) Simulation



(a)

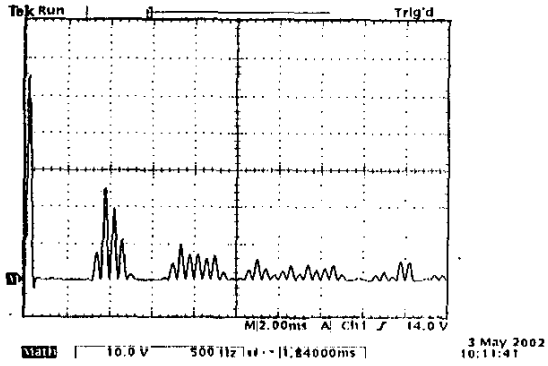


(b)

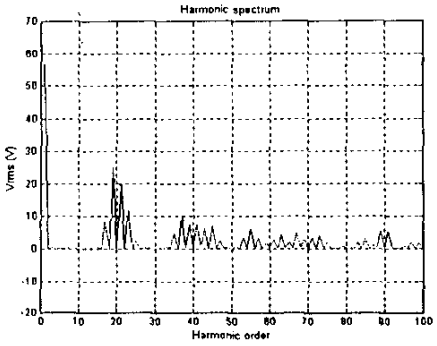
Top trace: Output voltage. Vertical scale 100V/div.
Bottom trace: Output current. Vertical scale 2A/div.Horizontal scale 2ms/div.

Fig. 5 (a): Practical result for $m_i = 0.8$; $m_f = 20$. (b) Simulation

For the case of $m_f = 20$ and $m_i = 0.4$, the practical result of output voltage harmonic spectrum are shown in Fig. 6(a). The theoretical spectrum for the similar case is shown in Fig. 6(b). By comparing both figures, it can be clearly observed that the harmonics incidences for $m_i \leq 0.5$ agree closely with theoretical predictions. The proposed modulation scheme produces only odd harmonics for even modulation ratio. Furthermore, harmonics at the carrier and the multiples of carrier frequency do not exist at all.



(a)

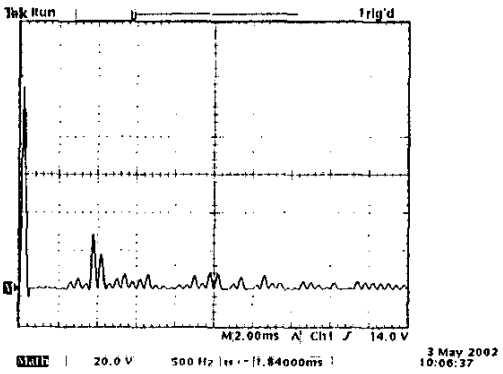


(b)

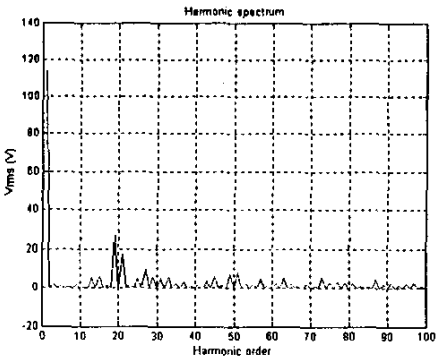
Vertical scale 10V/div.
Horizontal scale 500Hz/div.

Fig. 6 (a): Practical harmonic spectrum of output voltage for $m_i = 0.4$; $m_f = 20$. (b) Simulation.

The practical and simulation output voltage harmonic spectrum for the case of $m_f = 20$; $m_i = 0.8$ are illustrated in Fig. 7(a) and 7(b), respectively. Note that for five-level inverter, $m_i = 0.4$ is "equivalent" to $m_i = 0.8$ for a three-level inverter. For an equivalent modulation index, the significant harmonic of a five-level is half compared to a three-level inverter.



(a)



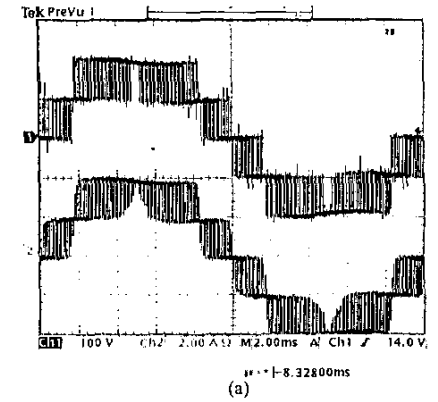
(b)

Vertical scale 10V/div.
Horizontal scale 500Hz/div.

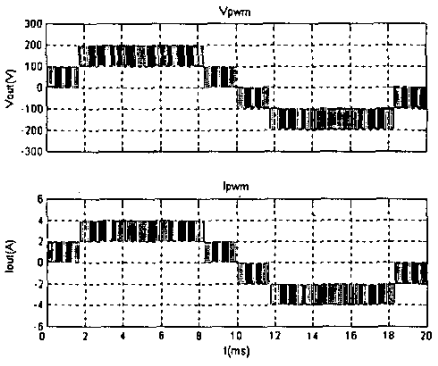
Fig. 7 (a): Theoretical harmonic spectrum of output voltage for $m_i = 0.8$; $m_f = 20$. (b) Simulation.

To evaluate the modulation scheme performance at higher frequency, test at modulation ratio equal to 200 is carried

out. This ratio corresponds to switching frequency of 10 kHz. The practical and simulation results for this case when modulation index equals 1.0 is shown in Fig. 8(a) and 8(b), respectively. It can be seen that at high switching frequency, the practical result in a good agreement with the simulation result. The respective harmonic spectrum, as illustrated in Fig. 9(a) and 9(b), are also consistent with each other.



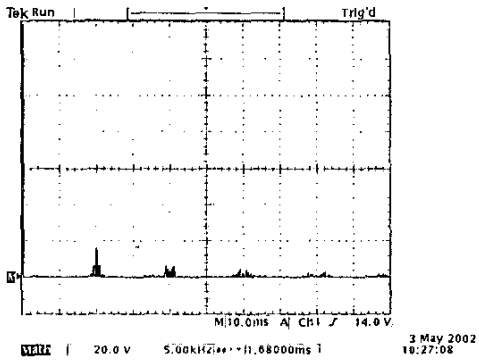
(a)



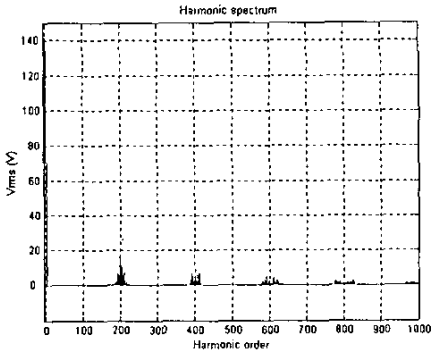
(b)

Top trace: Output voltage. Vertical scale 100V/div.
Bottom trace: Output current. Vertical scale 2A/div.
Horizontal scale 2ms/div.

Fig. 8 (a): Practical harmonic spectrum of output voltage for $m_i = 1.0$; $m_f = 200$. (b) Simulation.



(a)



(b)

Vertical scale 20V/div.
Horizontal scale 5kHz/div.

Fig. 9 (a): Theoretical harmonic spectrum of output voltage for $m_i = 1.0$; $m_f = 200$. (b) Simulation.

IV. SUMMARY

This paper presents a new switching scheme for a cascaded inverter. The proposed scheme is based on symmetric regular sampled unipolar PWM, with multiple modulating waveforms and a single carrier. Mathematical equations that define the PWM switching instants are verified by hardware test rig. The derived equations are implemented by a low-cost fixed-point microcontroller. It can be concluded that the hardware results in a good agreement with simulation results.

VI. ACKNOWLEDGEMENT

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VI. REFERENCES

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