An Approach to PSpice-aided Control Loop Design of DC-DC Converter Systems

Nik Din Muhamad and Abd Jaafar Shafie

Abstract--**A new approach to using Pspice in designing feedback for dc-dc converter systems is introduced in this paper. In this new approach, the feedback design procedures are programmed and made as a subcircuit in Pspice. For this purpose, an option available in Pspice called Analog Behavioral Modeling (ABM) is used. By using the subcircuit, the component values of the errror amplifier can be easily obtained by means of Pspice DC analysis. The methodology of development is presented in detail. Application examples are included to demonstrate the effectiveness of the proposed approach in designing feedbacks for dc-dc converters.**

Keywords--**DC-DC Converter, Computer-aided design, Pspice, Control loop design, Small-signal model**

I. Introduction

In recent years, there are many SPICE-based models developed for simulating dc-dc converters. In general, three types of model can be identified: the detailed model, the large-signal averaged model, and the small-signal model. All three models are valuable in analysis and design of dc-dc converter systems. The small-signal model is required to design the control system of a dc-dc converter. There are a number of well-documented techniques and guidelines for designing the control system of a dc-dc converter [1-6]. Nevertheless, the design of a feedback compensator is still not a simple task, especially for a new designer. The task involves the tedious, mechanical and human error prone computation of the transfer functions, and repetitive fine-tuning of compensation network component values. Moreover, the designer's judgment and experience are often required in the design process.

In this paper we demonstrate that the design procedures can be programmed in compact form in Pspice. For this purpose, an option available in Pspice called Analog Behavioral Modeling (ABM) is used. We choose to program the control loop design procedure [4] due to its generic, systematic and a widely adopted procedure [7-10]. The chosen design procedure is made as a subcircuit model and stored in Pspice's library. In this manner, the design procedure is treat as a library component, which makes it easy to use. The methodology of development is presented in detail. The presence of the design guideline's subcircuit model along with the existing models makes a new approach to using Pspice simulator in the design process. The proposed approach includes both design as well as simulation tools thus making extensive use of the SPICE in dc-dc converter design cycle. Moreover, both the flexibility and capability of SPICE as a stand-alone program can be enhanced. Using SPICE-aided design approach in dc-dc converter development can reduce the time and cost. Throughout this paper, a buck converter with voltage mode control is used as an example to develop and verify the control loop design procedure. The general procedure, however, can still be readily extended to include other converters with different control schemes provided that their transfer functions and design guidelines are available.

The authors are with the Department of Energy Conversion, Fakulti Kejuruteraan Elektrik, Universiti Teknologi Malaysia, 81310 Skudai, Johor. E-mail: nikd@fke.utm.my

0-7803-8208-0/03/$17.00 ©2003 IEEE.

II. Design Process Based On Small Signal Model

A. Buck Converter Power Stage

The buck converter power stage with PWM modulator of this study is depicted in Fig. 1. We assume that the converter is operated in continuous conduction mode. Using the averaging and linearization techniques, the control-to-output transfer function of the buck converter including PWM modulator, can be obtained as

$$\frac{\hat{v}_o}{\hat{v}_c} = g_{co}\frac{\left(1+\dfrac{s}{\omega_{zESR}}\right)}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}} \qquad (1)$$

where

$$g_{co}=\frac{V_g}{V_p},\ \omega_o=\frac{1}{\sqrt{LC}},\ \omega_{zESR}=\frac{1}{rC},\ \text{and}\ Q=\frac{R}{\omega_o L}$$

It can be seen from (1) that the control-to-output transfer function is dependent on the operating point. As the operating point of the converter is wide, the conventional way of designing the controller involves selecting the worst case operating point that is under the minimum line voltage (minimum V_g) and maximum load current (minimum R) conditions.

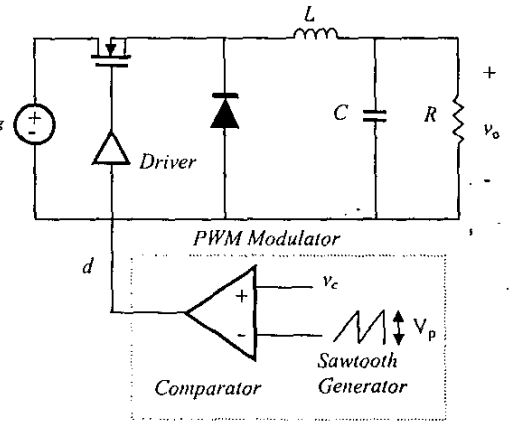


Fig. 1: Buck converter with PWM modulator

B. K-factor Approach

The loop shaping approach is simple and effective for dealing with the plants having complex dynamic behavior. Among popular loop shaping method in power electronic applications is K-factor approach, introduced by [4]. The main feature of K-factor approach is that the pole-zero placement and resultant circuit component values can be obtained without trial-and-error. That is one of the reasons why the k-factor approach widely accepted by many researchers [6-10]. The type-3 K-factor compensator is frequently used for compensation of buck, boost and buck-boost circuits due to its ability to provide the phase boost, $\emptyset_{boost}$.

$$0 \le \phi_{boost} \le 180^{\circ} \qquad (2)$$

The transfer function of the type-3 K-factor compensator is given by

$$G_c(s) = \frac{\frac{\omega_{co}}{A_{co}K}\left(\frac{\sqrt{K}}{\omega_{co}}s+1\right)^2}{s\left(\frac{s}{\sqrt{K}\omega_{co}}+1\right)^2} \qquad (3)$$

where ω_{co} is the desired crossover frequency, K is the pole frequency and zero frequency control factor. The value of K can be adjusted depending on the phase boost ($\emptyset_{boost}$) required to make the phase compensation.

Given the desired phase margin, PM, and the crossover frequency, ω_{co}, the phase boost that the compensator should be provided is

$$\phi_{boost} = PM - 90^{\circ} - \phi_{co} \qquad (4)$$

and the K-factor is calculated from equations 2 and 3 as:

$$K = \tan^2\left(\frac{\phi_{boost}}{4}+45^{\circ}\right) \qquad (5)$$

It is important to point out that this design procedure is general in the sense that it can be used to any suitable application. For specific application, this design procedure must be suited for the requirements of those applications. In the case of buck converter, an important constraint is that the crossover frequency must be less than one-fourth of the switching frequency. This constraint is required to avoid the large signal instability [1].

C. Type-3 K-factor Error amplifier

Fig. 2 shows the circuit diagram of the type-3 K-factor error amplifier or compensation network. The compensation network consists of the circuit elements as follows: C1, C2, C3, R1, R2, R3, and R_{bias}. This network has three poles and two zeros.

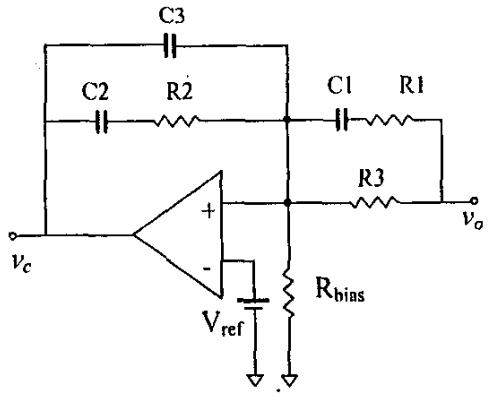


Fig. 2: Type-3 K-factor compensation network

The small-signal transfer function for the compensation network is given by

$$\frac{v_o}{v_c} = (-1)\frac{1}{s(C_2+C_3)R_3} \times \frac{(1+s(R_1+R_3)C_1)(1+sR_2C_2)}{(1+sR_1C_1)\left(1+sR_2\left(\frac{C_2C_3}{C_2+C_3}\right)\right)} \qquad (5a)$$

or

$$\frac{v_o}{v_c} = (-1)\frac{\omega_i}{s}\frac{(1+s/\omega_{z1})(1+s/\omega_{z2})}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \qquad (5b)$$

By matching (5a) and (5b) we can obtain

$$\omega_i = \frac{1}{R_3(C_2+C_3)} \qquad (6)$$

$$\omega_{z1} = \frac{1}{(R_1+R_3)C_1} \qquad (7)$$

$$\omega_{z2} = \frac{1}{(R_2C_2)} \qquad (8)$$

$$\omega_{p1} = \frac{1}{R_1C_1} \qquad (9)$$

$$\omega_{p2} = \frac{C_2+C_3}{R_2C_2C_3} \qquad (10)$$

III. PROPOSED APPROACH

Fig. 2 shows the flowchart of the overall procedure to determine component values of the error amplifier. The flowchart consists of three computational blocks: power stage, K-factor, and compensator. The computation is, therefore, performed in three steps:

1. The first step is to determine the magnitude, A_{co}, and phase, $\emptyset_{co}$, of the power stage $G_p(s)$ at the crossover frequency, f_{co}, which are executed in the block of power stage. The inputs to this block are: the input voltage, v_g, the value of L, the value of C, the load equivalent resistance R, the ESR capacitor, r. Besides, the user must also supply to the block the value of crossover frequency, f_{co}.

2. By knowing A_{co} and $\varnothing_{co}$, and specifying the desired phase margin, PM, the block of K-factor can be employed to systematically find the location poles and zeros of the compensation networks. The outputs of this block are: ω_i, ω_{p12} and ω_{z12}.
3. The block of compensator converts the location of poles and zeros of compensator to component values of the error amplifier.

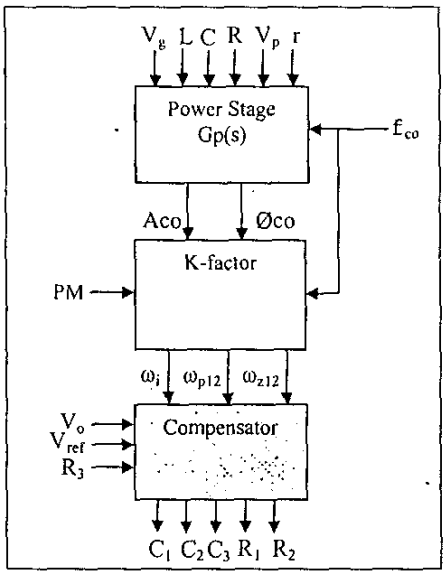


Fig. 2. Flowchart for the proposed approach

IV. PSPICE IMPLEMENTATION

The Pspice simulator is provided with an extension called Analog Behavioral Modeling (ABM). With ABM the simulator can be used like a programming language and to solve general mathematical problems by translating them to an electrical circuit. ABM in Pspice is able to evaluate expressions that are functions of circuit variables (voltages, currents, and simulation time) using the controlled current and voltage sources (G and E devices). ABM can also be used to solve system of linear and nonlinear algebraic equations as well as systems of complex, transcendent and ordinary, differential equations in their implicit or explicit form. In each case, the equations are converted into electrical circuits and solved by Pspice with a DC analysis for only algebraic equations or a transient analysis for systems of algebraic and differential equations. Editing the input file of Pspice is relatively more comfortable than programming in MATLAB, C or other program languages.

To implement the equations in Pspice, all variables are coded into voltages. The relevant equations are represented by dependent sources that are function of the coded variables and constants. In this section, we describe how the computation based on the results of Section III and IV can be implemented using ABM in Pspice.

A. Power Stage Block

The function of this block is to compute the magnitude and phase of the control-to-output transfer function, $G_p(s)$. The control-to-output transfer function for the buck converter has one zero and one complex pole-pair. The equation of the transfer function was previously given in (1). With $s = j\omega$, we see that transfer function is a complex number containing a real part and an imaginary part. The magnitude of a complex number is the square root of the sum of the squares of the real and imaginary parts. The phase is the inverse tangent (arctan) of the ratio of the imaginary part to the real part. Therefore, the magnitude of the control-to-output transfer function can be calculated as

$$\left|\frac{v_o}{v_c}\right| = A = \frac{G_{co}\sqrt{1+\left(\frac{\omega}{\omega_{zesr}}\right)^2}}{\sqrt{\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)+\left(\frac{\omega}{Q\omega_o}\right)^2}} \qquad (11)$$

The phase of the control-to-output transfer function can be calculated as

$$\phi = \tan^{-1}\frac{\omega}{\omega_{zesr}} - \tan^{-1}\frac{\frac{\omega}{Q\omega_o}}{1-\left(\frac{\omega}{\omega_o}\right)^2} \qquad (12)$$

To implement (12) and (13) in Pspice, the frequency is assigned as a variable, and other parameters are assigned as constants. The .PARAM statement is used for this purpose. By using the .PARAM statement we can create parameters and assign algebraic mathematical expressions to it.

B. K-factor Block

This block is used to implement K-factor approach in designing feedback compensator in Pspice. The inputs to this block are gain, A_{co}, and phase, $\varnothing_{co}$, of the control-to-output transfer function at the crossover frequency, f_{co} (or ω_{co}). By knowing A_{co} and $\varnothing_{co}$, and speciying the phase margin, PM, the phase boost required can be calculated as

$$\phi_{boost} = PM - 90^\circ - \phi_{co} \qquad (13)$$

Then, K-factor is calculated as

$$K = \tan^2\left(\frac{\phi_{boost}}{4} + 45^\circ\right) \qquad (14)$$

The two poles of the compensator are located at

$$\omega_{p12} = \frac{\omega_{co}}{\sqrt{K}} \qquad (15)$$

The two zeros of the compensator are located at

$$\omega_{z12} = \sqrt{K}\,\omega_{co} \qquad (16)$$

The integrator gain of the compensator is

$$\omega_i = \frac{\omega_{co}}{A_{co}K} \qquad (17)$$

(14)-(17) are also implemented in Pspice by using the .PARAM statement.

C. Compensator Block

The function of this block is to convert the values of poles and zeros to component values of the error amplifier. The inputs to this block are ω_{p12}, ω_{z12}, and ω_i that were obtained earlier from K-factor block. Besides, the user must provide

reference voltage, V_{ref}, and R_{bias}. The conversions occur as follows:

$$C_3 = \frac{f_{z12}}{(\omega_i R_3 f_{p12})} \quad (18)$$

$$C_2 = C_3\left(\frac{f_{p12}}{f_{z12}} - 1\right) \quad (19)$$

$$R_2 = \frac{1}{2\pi f_{z12} C_2} \quad (20)$$

$$R_1 = \frac{R_3}{\left(\frac{f_{p12}}{f_{z12}} - 1\right)} \quad (21)$$

$$C_1 = \frac{1}{2\pi f_{p12} R_1} \quad (22)$$

$$R_{bias} = \frac{V_{ref}}{V_o - V_{ref}} R_3 \quad (23)$$

(18)-(23) are also implemented in Pspice by using the .PARAM statement. To make the values of C3, C2, C1, R1, R2, and Rbias available in the schematic after the simulation finished, the relevant parameters are represented by dependent voltage sources.

The three blocks above were implemented in a single subcircuit. The Pspice netlist of the subcircuit and its symbol are shown in Appedix.

V. Application Examples

Two examples are included in this section to demonstrate the effectiveness of the proposed approach in designing feedback for dc-dc converters. The first example is a buck converter operated at the switching frequency of 100kHz. The second example is a similar buck converter, but the switching frequency is doubled and the inductor is halved.

A. 100kHz Buck Converter

The buck converter is designed to operate in continuous conduction mode. Following are the parameters of the converter: V_g= 10V to 15V, V_o = 5V, L = 30□H, R = 1.25Ω, fs = 100 kHz, Vp = 3V, Vref = 2.5V, Rbias = 10k. By knowing the converter parameters, the design of feedback compensator can be performed by using the developed subcircuit in Pspice. Before doing the design, two parameters should be chosen. The first is to choose the crossover frequency, f_{co}. This parameter determines how quickly the system responds to transient. In practice, f_{co} lies between fs/10 and fs/3. In our design we choose fs = fs/6, as a compromise. Another parameter to choose is the phase margin, PM, desired in the overall loop. Typical PMs range 45° to 75°. Lower PM, like 45°, give good transient response at the expense of peaking of the closed loop transfer function and output impedance. Higher PMs, like 75°, give flat closed-loop transfer function and minimum peaking of output impedance, but at the expense of speed and settling time. A good compromise is 60°.

Using the above parameters, the developed subcircuit was tested using the DC analysis in Pspice. The result is shown in Fig. 4. The time required to finish the simulation was just 0.13s, using Pspice Version 9.2.

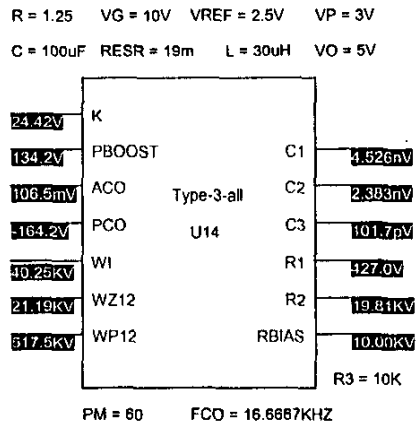


Fig.4. The result of DC analysis to give component values of the compensator.

To check the developed subcircuit working properly or not, the obtained component values of the compensator were used in the average model. Frequency response of loop-gain was simulated by Pspice AC analysis. Bode plot of loop-gain is shown in Fig. 5. From the bode plot, we can see that the crossover phase is –119.6°, indicating stable operation with PM of 60.4°. The crossover frequency is 16.623 kHz. The small differences between the desired values (PM = 60.0° and fco = 16.667kHz) and the results of Pspice are due to numerical errors

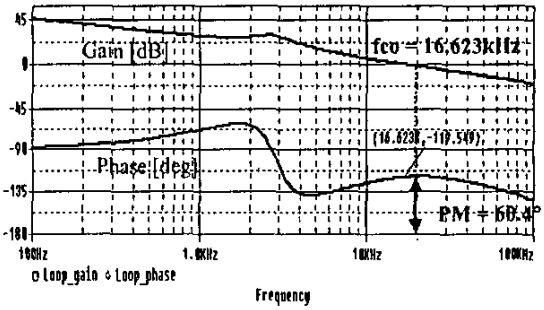


Fig. 5. Bode plot of loop-gain (gain in dB and phase in degree)

B. 200kHz Buck Converter

The parameters of this converter are the same as the previous example, except the switching frequency is doubled (f_s = 200kHz) and the inductor is halved (L = 15μH). It would be expected that the transient response of this converter is faster than the previous one. Without the developed subcircuit design procedure, any changes in the parameters made the whole system must be redesigned. With the developed subcircuit in hand, the process of redesign doesn't make any problem; the simulator can do it for us and give the result as shown in Fig.6. The time taken to simulate the whole process of redesign was 0.13s.

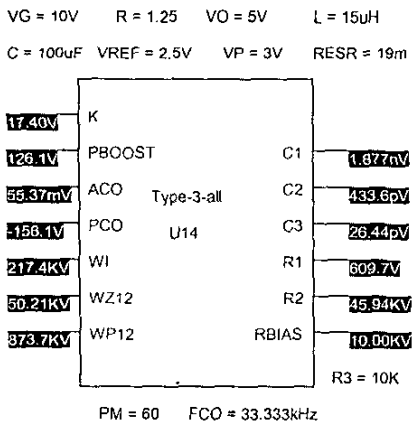


Fig.6. Compensator's parameters for 200 kHz buck converter.

For comparison between the two examples for a transient response, the switch model simulation (cycle-by-cycle) for a load step was performed. The load steps were made to occur at 8.0 ms (from 4A to 1A) and 8.3 ms (from 1A to 4A). The result is shown in Fig. 7.

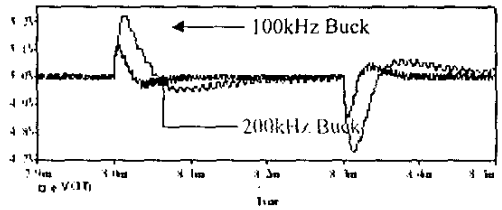


Fig. 7. Load steps response

As expected, the 200kHz buck converter has a faster transient response due to the higher f_{co} and the smaller inductor value.

V. Conclusion

A new approach to using Pspice in designing feedback of dc-dc converter system has been introduced. In this new approach, the feedback design procedures are programmed and made as a subcircuit in Pspice. The component values of the errror amplifier have been easily obtained by means of Pspice DC analysis. The extension of this approach to other converters and control schemes like peak current mode (PCM), Average current control (ACC) and power factor correction (PFC) is straightforward provided that there exist small-signal models and design procedures.

VI. Acknowledgement

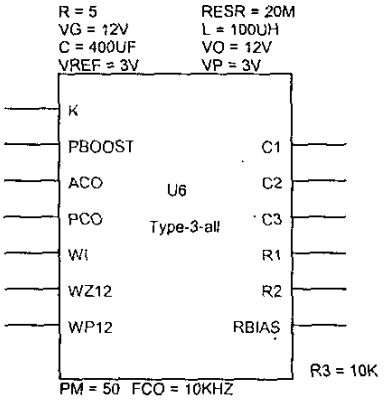
This work was partially supported by the RMC GRANT, VOT NO: 74305.

Appendix

Subcircuit:

```
**************************************************
* source ERROR-AMP
.SUBCKT Type-3-all Aco C1 C2 C3 k Pboost Pco R1 R2
+ Rbias wi wp12 wz12 PARAMS:
+ Vg=12 Resr=20m R3=10k Vo=12V Vp=3V Vref=3V L=100uH
fco=10kHz
+ PM=50 C=400uF R=5
.PARAM C2={C3*((wp12/wz12)-1)} w={2*pi*fco} R1={R3/(k-
1)} C3=
+                                {wz12/(wi*R3*wp12)}
mag1={SQRT((1+(w*w)/(wzesr*wzesr)))} R2=
+ {1/(wz12*C2)} Pboost={PM-90-Pco} wi={w/(Aco*k)}
wz12={w/sqrt(k)} Rbias=
+ {Vref*R3/(Vo-Vref)} k=
+ {(Tan(((Pboost/4)+45)*pi/180))*(Tan(((Pboost/4)+45)*pi/180))}
phase=
+                {-atan((w/(Q*wo))/(1-(w*w)/(wo*wo)))*180/pi}
Mcomp={(1/mag)} Pco={Pcomp+phase1}
+ phase1={atan(w/wzesr)*180/pi} wo={1/SQRT(L*C)} Aco=
+          {Mcomp*mag1*Vg/Vp}                Pcomp={IF((1-
((w*w)/(wo*wo)))<0,phase-180,phase)}
+       pi=3.14159   wp12={w*sqrt(k)}       wzesr={1/(Resr*C)}
Q={R/(wo*L)}
+   mag={SQRT(((w/(Q*w))*(w/(Q*w)))+(1-(w*w/(wo*wo)))*(1-
(w*w/(wo*wo))))}
+ C1={1/(wp12*R1)}
E_ABM5      R1 0 VALUE { R1   }
E_ABM3B1    R2 0 VALUE { R2   }
E_ABM5B1    C1 0 VALUE { C1   }
E_ABM9B1    RBIAS 0 VALUE { Rbias   }
E_ABM6      PBOOST 0 VALUE { Pboost   }
E_ABM6B1    WI 0 VALUE { wi   }
E_ABM7B1    WZ12 0 VALUE { wz12   }
E_ABM1B1    C3 0 VALUE { C3   }
E_ABM1X     K 0 VALUE { k   }
E_ABM4A1    ACO 0 VALUE { Aco   }
E_ABM2B1    C2 0 VALUE { C2   }
E_ABM8B1    WP12 0 VALUE { wp12   }
E_ABM5A1    PCO 0 VALUE { Pco   }
.ENDS Type-3-all
**************************************************
```

Symbol:



VII. References

[1] Lloyd H. Dixon, "Closing the feedback loop," *Unitrode Power Supply Design Seminar Handbook: SEM 700A*, 1990.

[2] W. Tang, F. C. Lee and R. B. Ridley, "Small-Signal Modeling of Average Current-Mode Control," *IEEE Trans. Power Electronics*, Vol. 8, no. 2, Apr. 1993, pp. 112-119.

[3] B. Holland, "Modeling, Analysis and Compensation of the Current-Mode Converter," *Proceeding of the Powercon* 11, 1984, pp. I-2-1-I-2-6.

[4] H. Dean Venable, "The k-factor: A New mathematical Tool for Stability, Analysis, and Synthesis," *Proceeding of Powercon 10*, San Diego, CA, March 22-24, 1983.

[5] Lloyd H. Dixon, "Average Current Mode Control of Switching Power Supplies," *Unitrode Application Note*, 1999.
[6] J. Sun, R. M. Bass, "Modeling and Practical design issues for Average Current Control," *Proc. of APEC*, Vol. 2, pp. 980-986,1999.
[7] S.A. Chickamenahalli *et. al.*, "Effect of target impedance and control loop design on VRM stability," *Proc. Of APEC, 2002*, Vol. 1.
[8] Abraham I. Pressman, *Switching Power Supply Design*, McGrawHill, 1998.
[9] N. Mohan, T. M. Undeland, W. P. Robins, *Power Electronics: Converters, Applications and Design*, John Wiley, 1995.
[10] C. M. Liaw, T. H. Chen, W.L. Lin, "Dynamic modelling and control of a step up/down switching-mode rectifier," *IEE Proc. - Electric Power Applications*, Vol. 146 Issue: 3, May 1999, pp. 317–324.