SYSTEM-ON-CHIP (SOC) TESTING USING ADHOC HIGH-LEVEL DESIGN-FOR-TESTABILITY METHOD

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ABSTRACT

The design of System-on-Chip (SoC) is becoming more complex and number of transistors in a chip has increased from millions of gates to billions of gates nowadays but the number of Input/Output pins still remains about the same. In this case, design-for-test (DFT) becomes so important in order to make the chip more easily testable. By increasing the DFT features into a chip, this will definitely increase the overhead of the chip. In this project, an alternative DFT method is used to minimize the overhead of the chip resulted from DFT without affecting the fault coverage.

A case study is conducted by applying the proposal ad-hoc DFT method on GCD calculator. Area overhead and test application clock cycles are evaluated and compared to those parameters resulted from the conventional DFT method called full scan. The case study showed that the area overhead was smaller and the test application clock cycles were less when GCD was augmented with proposed DFT method.

ABSTRAK

Perekaan “system-atas-chip” (Soc) telah menjadi semakin kompleks dan bilangan transistor dalam satu chip telah meningkat secara dramatic tetapi bilangan pin untuk “Input-Output” (IO) masih kekal lebih kurang sama. Dengan ini, reka-untuk-ujian (DFT) menjadi amat penting dalam pengujian chip. Dengan menambahkan fungsi DFT dalam satu chip akan meningkat bahagian-tanpa-guna (overhed). Dalam project ini, satu kaedah DFT yang alernatif akan digunakan to mengurangkan “overhead” dalam chip dan tanpa menjejaskan liputan kesalahan.

Satu kajian kes telah dijalankan dengan menggunakan cadangan kaedah DFT “adhoc” pada kalkulator GCD. Overhed dan kitaran jam ujian adalah dinilai dan berbanding dengan parameter itu didapati daripada kaedah DFT konvensional. Kajian kes ini menunjukkan overhed adalah lebih kecil dan kitaran jam ujian adalah lebih pendek apabila GCD ditingkatkan dengan kaedah DFT “adhoc” yang dicadangkan.

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CHAPTER 1

INTRODUCTION

System-on-Chip (SoC) testing using P1500 induces large area overhead coming from additional bus of test access mechanism and test wrapper. Each core in the System-on-Chip (SoC) is equipped with Design-For-Testability (DFT) like scan technique. To reduce the area overhead, some research on testing System-on-Chip (SoC) using existing functional buses have been done. However, the Design-For-Testability (DFT) for each core is still scan design [1]. In this project, a new testing method is proposed. This testing method is using existing functional buses, which is same as previous work but Design-For-Testability (DFT) is introduced to each core before synthesis of the core. In other words, the Design-For-Testability (DFT) is introduced at high level. In this project, case study using a simple System-on-Chip (SoC) consisting of a processor and a Greatest Common Divisor (GCD) core will be done by comparing the area of the System-on-Chip (SoC) augmented with P1500 & full scan and that of the System-on-Chip (SoC) augmented with high-level design-for-testability.

1.1 Background

The increasing of standard DFT overhead in SoC design stimulates new research on DFT in order to reduce the overhead of the DFT design in SoC. This project involves GCD design with P1500 and alternative high-level DFT.

1.2 Objective

The goal of this project is to compare two systems: SoC with P1500 wrapper & full scan and SoC with Adhoc High Level DFT in term of testing time and number of gates. Greatest Common Divisor (GCD) is used as the case study. To achieve the goal, the following objective are set.

- To design a SoC system with P1500 wrapper & full scan.
- To design a SoC system with Adhoc High Level DFT.
- To Implement both systems in Altera DE2-70 board.
- To make comparison between two systems in term of number of gates and testing clock cycle.

1.3 Project Environment

This project was implemented in hardware manner.

- Hardware:
  - Altera DE2-70 Board

- Software/Tools:
  - Altera Quartus II 9.0 Web Edition

Scope of the project includes:

i. Implemention of High-Level DFT on GCD.
ii. Write a test program that reads the test vectors from memory.
iii. Write a test program that compares the test responses with the expected test response in the memory.
iv. Design a test wrapper for GCD with scan-flops.
v. Compare the testing time and area between the conventional full scan method and the proposed high-level DFT method.

1.4 The Organization of Thesis

Chapter 1 briefs the introduction of SoC DFT design challenges, application background overview, purpose of thesis and project objectives and development environment.

Chapter 2 covers P1500 system overview including the building blocks of the P1500 system.

Chapter 3 discusses the design methodology using RTL coding.

Chapter 4 describes two actual SoC systems developed, covering components and sub-blocks on the system.

Chapter 5 covers the simulation of the system, the experimental results and results analysis.

Finally in Chapter 6, conclusions are made for the project based on the system. Future works are discussed too.

CHAPTER 6

CONCLUSION AND FUTURE WORK

The project met its primary purpose to compare two SoC designs in term of testing speed and gate count. From the result analysis in Section 5.3, SoC design with Adhoc HL DFT is the better choice because:

- Less overhead
- Faster testing time.
- Simpler testing pattern.
- Testing algorithm is controlled by software (more flexible).

For future works, more complex designs can be used in the case study and more tests to be tested. This will give higher justification to the result comparison.