Growth Parameters of Indium Arsenide Quantum Dots Using Metal Organic Vapour Phase Epitaxy

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To my beloved mother, father, sisters and brother
Who's supporting me in pursuing higher learning of knowledge

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Abstract

Metal-organic vapour phase epitaxy (MOVPE) is a versatile system that is capable of growing various materials especially the II-VI and III-V semiconductor materials. However, growth conditions for each individual system are different from the other and need to be individually calibrated. The work presented in this thesis is to calibrate and determine the growth parameters for the growth of indium arsenide (InAs) quantum dots on gallium arsenide (GaAs) substrates via Stranski-Krastanov self-assembled growth mode. The experiment was done in the cleanroom using a newly installed MOVPE system at Ibnu Sina Institute for Fundamental Science Studies, UTM. The effect of various growth parameters on the dot nucleation have been studied using atomic force microscopy (AFM) for structural information and photoluminescence (PL) for optical characterization. The growth parameters studied include growth rate, temperature, and V/III ratio. A total of 15 samples have been grown with five samples represent each selected parameter. The surface morphology of each samples for each parameter was observed using AFM. Graphs of dots height and width were plotted and the optimal growth parameters were obtained. The result shows that optimal parameters for the InAs quantum dots growth were temperature of 550 ^{o}C, V/III ratio of 10 and growth time of 4 seconds. Three more samples with optimal parameters were then grown for the PL and energy dispersive X-ray (EDX) characterization. The results show strong confinement quantum dots have been successfully grown in this experiment. The results of this study can be used for further improvement of the indium arsenide quantum dots growth.

Abstrak

Metal-organic vapour phase epitaxy (MOVPE) merupakan satu sistem yang serba boleh berkeupayaan menumbuhkan pelbagai bahan terutamanya bahan-bahan semikonduktor kumpulan II-VI dan III-V. Walaubagaimanapun keadaan pertumbuhan untuk setiap sistem adalah berbeza antara satu sama lainnya dan perlu ditentukurkan secara individu. Kerja yang dibentangkan di dalam tesis ini adalah untuk proses tentukuran dan penentuan parameter optimum bagi pertumbuhan bintik kuantum indium arsenida (InAs) di atas substrat gallium arsenida (GaAs) melalui mod pengumpulan-kendiri Stranski-Krastanov. Eksperimen dilakukan di Bilik Bersih, Institut Kajian Sains Fundamental Ibnu Sina, UTM menggunakan alat MOVPE yang baru dipasang. Maklumat struktur bagi kesan pelbagai parameter pertumbuhan ke atas penukleusan bintik dikaji menggunakan *atomic force microscope* (AFM) manakala fotoluminesens (PL) pula digunakan bagi pencirian optik. Parameter pertumbuhan yang dikaji termasuklah kadar pertumbuhan, suhu dan nisbah V/III. Sebanyak 15 sampel telah ditumbuhkan dengan lima sampel mewakili tiap parameter. Morfologi permukaan setiap sampel untuk setiap parameter dilihat menggunakan AFM. Graf dari ketinggian dan kelebaran bintik diplotkan dan parameter optimum diperolehi. Hasil kajian menunjukkan dot terbaik diperolehi pada suhu optimum 550 ^{o}C, nisbah V/III adalah 10 dan masa pertumbuhan 4 saat. Tiga lagi sampel dengan parameter optimal kemudiannya ditumbuhkan untuk pencirian PL dan *energy dispersive X-ray* (EDX). Hasilnya menunjukkan bintik kuantum yang terkurung kuat telah berjaya ditumbuhkan dalam eksperimen ini berasaskan parameter optimum. Hasil dari kajian ini boleh digunakan untuk memperbaiki lagi pertumbuhan bintik kuantum indium arsenida.

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LIST OF SYMBOLS

%	Percentage
ϕ	Height of tunneling barrier
μ	Micro (10^{-6} meter)
a_B	Exciton's Bohr radius
c	The speed of light = 299 792 458 m / s
D	Structure's diameter
d	Width of tunneling barrier
E	Energy band-gap
eV	Electron Volt Energy
h	Planck's constant = 6.626068×10^{-34} m^2 kg / s
n	Nano (10^{-9} meter)
^oC	Temperature Celsius
s	second
sccm	Standard centi-cubic meter
λ	Wavelength

LIST OF ABBREVIATIONS

2D	2- Dimensional
3D	3- Dimensional
AFM	Atomic Force Microscopy
AsH_3	Arsine
CMOS	Complementary- metal–oxide–semiconductor
EDX	Energy Dispersive X-ray
FESEM	Field Emission Scanning Electron Microscope
GaAs	Gallium Arsenide
HRXRD	High Resolution X-Ray Diffraction
IIS	Institute Ibnu Sina
InAs	Indium Arsenide
InGaAs	Indium Gallium Arsenide
MO	Metal Organic
MOSFETs	Metal–oxide–semiconductor field-effect transistors
MOVPE	Metal-Organic Chemical Vapour Epitaxy
PL	Photoluminescence
QDs	Quantum Dots
R&D	Research and Development
RHEED	Reflection high energy electron diffraction
SET	Single Electron Transistor
SLCI	Extra Large Scale Circuit Integration
STM	Scanning Tunneling Microscopy
TEM	Tunneling Electron Microscopy
TMGa	Tri-Methyl Gallium
TMIn	Tri-methyl Indium
UPM	Universiti Putra Malaysia
UTM	Universiti Teknologi Malaysia

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CHAPTER I

INTRODUCTION

1.1 Background of the Research

The modern lives we enjoy today are mostly contributed by the dramatic development in the microelectronic field. From the history of the semiconductor development starting 60 years ago, starting with the invention of the first transistor in 1947 by John Bardeen and Walter Brattain and following with the development of Integrated circuits in 1958 by Jack Kilby until now, the size of the integrated circuits have been shrunk in size and increased in number of transistors per area.

As predict by Gordon Moore, the size of the transistor will reduce half every 1.5 years. It have been 45 years since the introduction of the Moore's law, the development of the semiconductor technology until today still following this law. Pioneer by the Intel Corp, the size of the transistor are predicted to have gate length of 25nm in year 2013 using nano-lithography (Intel Corp, 2008). There are also researches for higher efficiency laser diode, this interest brought up by researchers in order to achieve smaller size, lower power consumption, and lower cost, semiconductor lasers used as optical transmitters in optical networks and high-speed optical LANs to replace the strained quantum-well lasers which optical output is sensitive to changes in ambient temperature (Fujitsu Corp, 2007), the researchers are focus on higher dots density, higher uniformity among the dots, smaller dots size and control of dots growth array which cannot use the conventionally lithography technique due to technology limitation of minimization.

1.2 Problem with Future Minimization

Smaller transistor will offer smaller operating power and faster operating speed. The exponential growth of information technology over the past few decades has been largely enabled by scaling of metal–oxide–semiconductor field-effect transistors (MOSFETs) and complementary- metal–oxide–semiconductor (CMOS) into the nanometer regime (Chen Q et. al., 2004). Individual transistors with gate length as small as 15nm have been fabricated using gallium arsenide (Gordon et. al., 1997), but further miniaturization became a question when the size of the transistor entering the quantum region.

1.2.1 Technology Limitation

The fabrication of semiconductor wafer heavily relied on the lithography technique. New lithography technique such as the electron-beam lithography, X-ray lithography and plasma etching offer high resolution of etching result. The best resolution can be obtained is 15nm for electron-beam lithography, 20nm for X-ray lithography and 15nm for plasma etching. Obviously we cannot meet the challenges for future miniaturization for transistor such as MOSFETs and CMOS. With leading edge lithography technique, it is still difficult for transistors to be made sufficiently uniform and reliable to build into a densely integrated computer containing a billion or more of them.

To produce a ELSCI (Extra Large Scale Circuit Integration), billions of smaller and faster transistors get packed into a single piece of silicon about an square inch size, it power consumption and heat generated in the processor core becomes a significant technical challenge. Intel® comes out with new depleted substrate transistor; it was fabricated on an ultra-thin silicon layer to reduce current tunneling leakage. However, the leakage through this ultra-thin insulator layer becomes one of the largest sources of power consumption of chips. Intel® then replaced this silicon layers with other high dielectric material which grow atomically layer by layer, however such complicated process will increase the cost and the semiconductor material within the transistor will lost it bulk properties when further scaling and this meets another dead end.

1.2.2 Semiconductor Bulk Properties Limitation

The transistors widely use today are MOSFETs and CMOS which working on semiconductor bulk properties, when the further minimization of the integrated circuit, the transistor size will follow the same path and now the bulk properties of the semiconductor devices had meet the end of the road. Some of the characteristic of the limitation for down scaling of the semiconductor devices or transistor are as below: (Gordon et. al., 1997)

- High electrical field – Bias voltage apply over the short length of the gate can cause the "Avalanche Breakdown". Majority of the electrons will be excited out from the semiconductor at high energy and causes the circuits to surge.

- Heat problem – Further miniaturization means more transistors per area in the integrated circuit, the structure of the transistors and other components become more compact. With the same materials applied with same thermal efficiency, extra heats from the devices which will cause overheat and malfunction to the devices.

- Lost of bulk material properties – Doping in small scale will result in non-uniformity; this will require the doping atoms to form a regular array.

- Shrinkage of depletion regions – The depletion regions will become too thin and quantum tunneling of electron from the source to the drain will occur and interrupt the transistor function.

- Shrinkage of Insulator layer – The insulator layer will also becomes thinner following the down size of the transistor and when the thickness become too thin, electrons will escape through tunneling.

1.3 Quantum Effect on Quantum Confinement

When the dimension of the semiconductor structure scaling down to nano region, two noticeable effects i.e. the energy quantization and the electron tunneling will start to occur. When the semiconductor structures reduce to a certain dimension, the bulk properties will start to disappear.

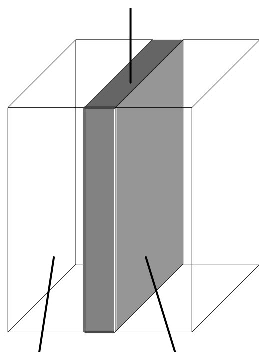
1.3.1 Quantum Confinement

The scaling of the material to nano region is called quantum confinement, in term of low dimensional semiconductor; it was describe as *confinement of the exciton within the physical boundaries of the semiconductor* (Strouse, 2003). The confinement regimes refer to the size in semiconductor quantum structures that comparing the Bohr radius (a_B) to the diameter of the nano-crystal (D),

Strongly-confined regime: $D < 2a_B$
Intermediate confinement regime: $D \sim 2a_B$
Weakly-confined regime: $D > 2a_B$

The exciton Bohr radius ($a_B \sim 5.0$ - 5.5 nm) is the distance between the electron and the hole within an exciton. The exactions here are referring to coulomb correlated electron/hole pair in a semiconductor. It is the elementary excitation state in a semiconductor. This phenomenal happen when a photon collides into a semiconductor, which is then excites an electron from valence band into the conduction band and the missing electron in the valence band leaves a hole of opposite electric charge behind it, and consequently to which it is attracted by Coulomb force. The exciton results as the binding of the electron with its hole. For good quantum properties, one will need strong confinement around 10 nm. All materials have three-dimensional surfaces and in semiconductor material were no exceptional either. The confinement for the semiconductor material's structure can be one-dimensional confinement, two-dimensional confinements or three-dimensional confinements.

One-Dimensional Confinement



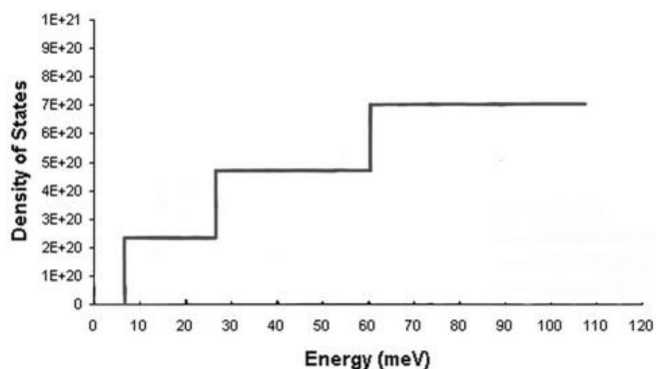
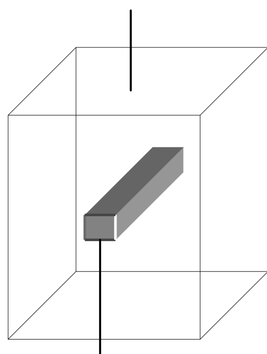


Figure 1.1a: Thin film

Figure 1.1b: Thin film density of state

One-dimensional confinement semiconductor structure is called the quantum well; the quantum well is a higher band-gap material sandwich between two lower band-gap materials to form an energy threshold as shown in Figure 1.1a. It energy will quantized due to the confined one dimensional resulting step-like density of states as shown in Figure 1.1b.

Two-Dimensional Confinement



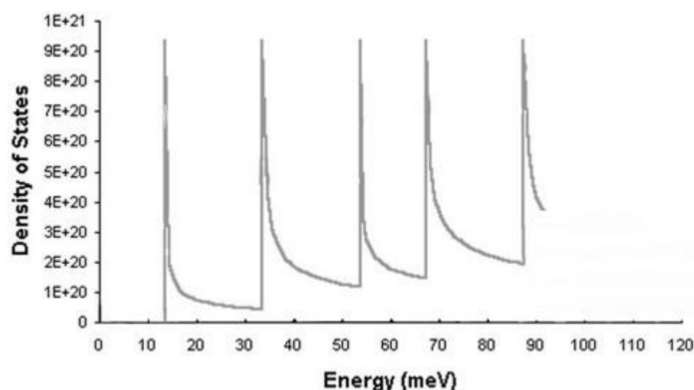


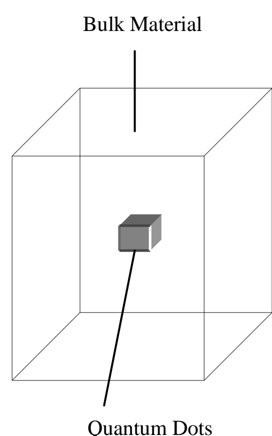
Figure 1.2a: Quantum wire

Figure 1.2b: Quantum wire density of state

Two-dimensional confinement semiconductor structures is called quantum wire, a rod like shape which allow electron mobility in one-dimension as shown in

Figure 1.2a. It energy will quantized in two-dimensional space resulting the density of states as shown in Figure 1.2b.

Three-Dimensional Confinement



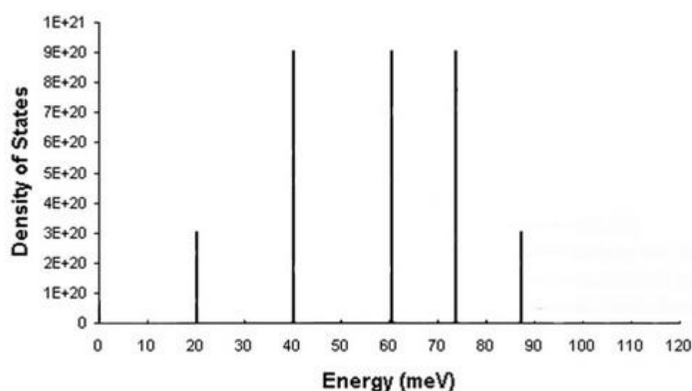


Figure 1.3a: Quantum dot Figure 1.3b: Quantum dot density of state

Finally the three-dimensional confinement semiconductor structures is called quantum dot. The quantum dot as its name indicates is confined in three-dimensional space into a sphere or cube shape such as in Figure 1.3a. The electron movement is restricted in all three dimensions resulting a discrete energy as shown in Figure 1.3b.

1.3.2 Tunneling Effect

The dimension of the semiconductor structures while scaling down into nano region, will reach a critical dimension when electron not longer flow normally but tunneling into the other layers of materials. Quantum tunneling is a quantum mechanical phenomenon, where wave can penetrate through barrier materials which are not possible classically. In quantum mechanic, the electron either can be a particle or wave function, and since the electron is a wave function, it will have probability to tunneling through barrier material (Gerhard et. al., 1994). Few parameters that related to tunneling are:

- mass of particle: reduces tunneling exponentially
- height of barrier: reduces tunneling exponentially
- width of barrier: reduces tunneling exponentially
- dissipation: reduces tunneling, perhaps to zero

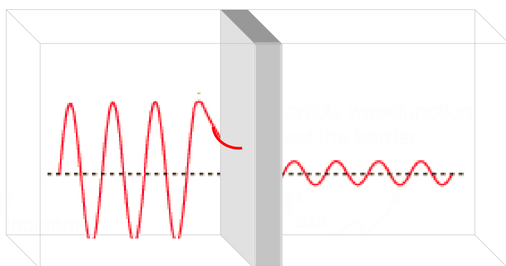


Figure 1.4a: Tunneling effect

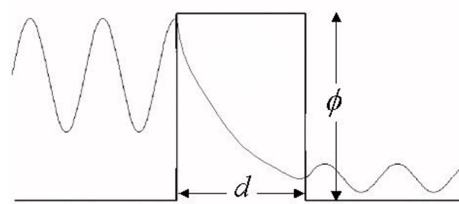


Figure 1.4b: Tunneling barrier

The tunneling in semiconductor can be described in Figure 1.4a, where an electron wave function is tunneling through the high band-gap barrier. The tunneling coefficient largely affected by the width d and the height ϕ of the barrier as shown in Figure 1.4b. The tunneling effect in nano region in semiconductor will be one of the main limitations on future scaling of transistor size. For this reason, instead of avoiding this tunneling effect, scientists around the world are researching a new type of semiconductor operating using the tunneling effect. One such device is single-electron transistor or SET.

1.4 Application of Quantum Dots

Single-electron transistors operating in the principle as one electron tunneling through the island dot located in the middle of the transistor as shown in Figure 1.5a and 1.5b. Figure 1.5a is a single-electron transistor fabricated using etching technique while the selective area growth single-electron transistor in Figure 1.5b is fabricated by Hokkaido University of Japan (Motohisa et. al., 1996)

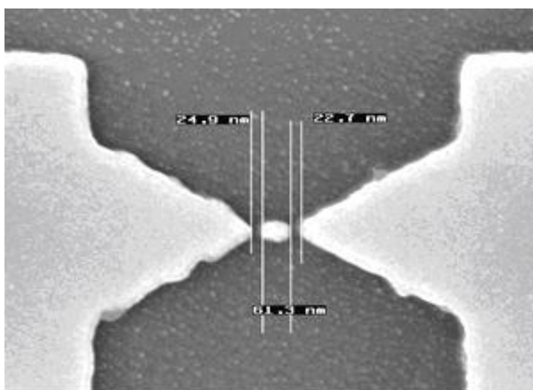


Figure 1.5a: Lithography etched SET

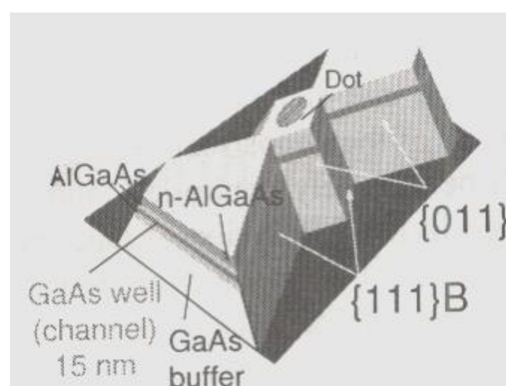


Figure 1.5b: Self-assembled SET

In 1982 it was first theorized that quantum dot (QD) lasers would have better temperature stabilities (Arakawa et. al., 1982). Since then other improvements have also been predicted for QD lasers (Asada et. al., 1986]. A quantum dots laser operating in the principle as photons emitter at high energy band gap as shown in Figure 1.6a. Generation of high power and high efficiency laser is possible using smaller quantum dots (Figure 1.6b) which will produce shorter light wavelength and thus increase the laser power.

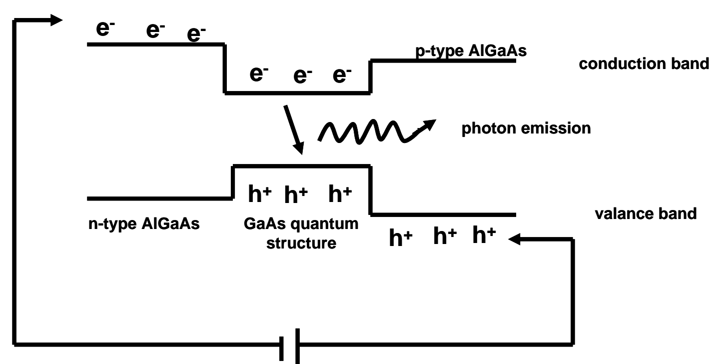


Figure 1.6a: Diagram of photon emission from quantum laser

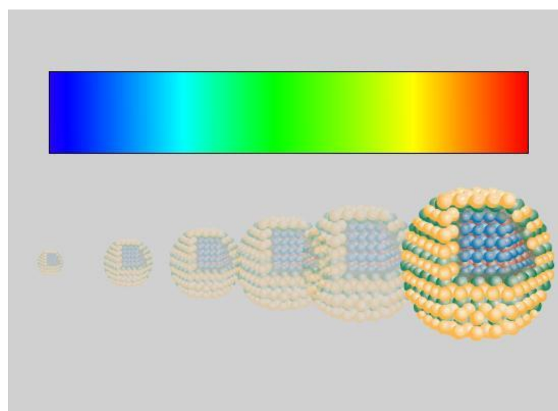


Figure 1.6b: Quantum dots size effect on emission photon wavelength.

The first quantum dot lasers were based on a single layer of dots and lased at 77K (Kirstaedter et. al., 1996; Ledentsov et. al., 2000). These early lasers were found to have high characteristic temperatures and low threshold currents, as predicted by theory (Arakawa et. al., 1982; Asada et. al., 1986; Lott et. al., 2000). In order to obtain room temperature lasing several layers of dots were grown (Ledentsov et. al.,

2000). Improvements to the threshold current densities were made by embedding the dots into a well structure and including AlGaAs in the barrier layers (Ledentsov et. al., 2000). Lasers based on several layers of dots, operating at room temperature, were reported soon afterwards (Heinrichsdorff et. al., 1997). Quantum dot VCSELs, emitting at 1.3 ɫn, have been demonstrated (Lott et. al., 2000). Other devices have been predicted to improve with the use of quantum dots in their active regions. There are now many reports of quantum dot infrared photodetectors that show signs of improved performance over quantum well infrared photodetectors (Liu et. al., 2001; Tang et. al., 2001; Stiff-Roberts et. al., 2002)

1.5 Research Problem

1. This study was done using a new MOVPE machine assembled at Nanophysics Laboratory, Ibn Sina Institute for Fundamnetal Science, UTM with unknown growth parameters

2. Growth parameters are vary from one chamber to the other based on the design and source flow

3. Limited growth technique or recipe to achieve thesis objectives, a little different growth design, recipe and chamber can produce a far different result.

1.6 Research Objectives

This work is based on the following research objectives:

a) To grow the Indium Arsenide quantum dots using Metal-Organic Chemical Vapour Epitaxy (MOVPE) under three different parameters:

    - Temperature
    - V/III ratio
    - Source Rate

b) To obtain the best growth parameter for all three parameters studies for Indium Arsenide quantum dots

1.7 Research Scope

- Fabrication of the indium arsenide (InAs) quantum dots using metal organic vapour phase epitaxy (MOVPE), on gallium arsenide (GaAs) wafers. Three parameters studies are growth temperature, source rate and V/III ratio to get the optimal dot formation.

- Observe the indium arsenide quantum dots formation trend under the atomic force microscopy and photoluminesence. This observation will provide information and understanding about the optimal condition to get the confined dots size, height, density and distribution.

1.8 Thesis Summary

This thesis is divided into five chapters. Chapter I Introduces the limitation of current technology in Solid State Nanotechnology and the advantage of the quantum dots behind the quantum confinement energy and quantum tunneling. Research objectives and scopes of this thesis are also explained in this chapter.

Chapter II summarizes all the theory related to this study by reviewing related literatures. This includes the theory and experiments about the self assembly quantum dots formation.

Chapter III explains the experimental set-up and procedures for growing of quantum dots using MOVPE. Including in this chapter is the calibration of the MOVPE system and samples characterization. The experimental results are then discussed in Chapter IV and Chapter V presents the conclusion of this study and suggestion for future improvement.

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