A COMPUTER-AIDED DESIGN SOFTWARE MODULE FOR CLOCK TREE SYNTHESIS IN VERY LARGE SCALE INTEGRATION DESIGN

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Specially dedicated to
my beloved family

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ABSTRACT

With the evolution of Very Large Scale Integration (VLSI) fabrication technology, circuit size has grown and line width has decreased. In effect, the transistor transit time and the time to drive signal lines across chips have also decreased. Thus, interconnections have become the dominating factor in determining circuit performance and reliability in the design of a VLSI circuit. Clock distribution network, which is one of the biggest and most important nets in any synchronous VLSI chip, is sensitive to these variations. The increased line resistance is one of the primary reasons for the increasing significance of clock distribution networks on synchronous performance. Furthermore, failing to control the clock skew can also severely limit the maximum performance of the entire system and create catastrophic race conditions in which an incorrect data signal may be latched by register. This thesis proposes a Computer Aided-Design (CAD) software module for useful-skew tree synthesis in deep-sub-micron VLSI design. Building the proposed CAD software module involves the implementations of the abstract topology generation algorithm, skew constraints scheduling algorithm and clock tree construction algorithm. Due to the lack of availability of circuit data and necessary software tools, we introduced a different test methodology to test the reliability of the proposed CAD software module. Two different test data have been used to verify the functionality of the CAD software module. Tests on the random input data show that our CAD software module successfully synthesizes clock trees that satisfy the entire clock skew constraints, and at the same time, achieve a shorter wire-length. Tests on benchmark circuit's data show that our CAD software module successfully synthesizes clock trees that not only satisfy the skew constraint value, but also further reduced the computed applicable clock period of the circuit.

ABSTRAK

Evolusi perkembangan teknologi fabrikasi "*Very Large Scale Integraion*" (*VLSI*) telah menyebabkan saiz litar semakin besar dan saiz lebar pengalir mengecil. Keadaan ini menyebabkan masa melintasi transistor telah berkurangan dan seterusnya masa memandu isyarat melintasi cip turut berkurangan. Oleh itu, penyambung-penyambung dalaman cip menjadi faktor utama menentukan prestasi dan kebolehpercayaan rekabentuk litar *VLSI* sekarang. Rangkaian pengagihan isyarat jam, merupakan salah satu rangkaian terluas dan terpenting bagi cip segerak *VLSI*, amatlah sensitif kepada perubahan perkembangan ini. Penambahan rintangan akibat daripada pengurangan saiz lebar pengalir merupakan salah satu sebab utama penambahan kepentingan oleh rangkaian isyarat jam dalam menentukan prestasi kesegerakan litar. Tambahan pula, kegagalan mengawal pencongan jam menghadkan lagi maksima prestasi keseluruhan sistem dan boleh mewujudkan keadaan pelarian data, iaitu data-data yang salah akan diselak oleh pendaftar. Tesis ini mencadangkan satu modul perisian Rekabentuk Bantuan Komputer (*CAD*) yang dapat mensintesiskan "*useful-skew tree*" untuk rekabentuk *VLSI* sub-mikro-dalam. Pembangunan modul perisisian yang dicadangan tersebut melibatkan implementasi algoritma penjanaan topologi abstrak, penjadualan pencongan jam dan pembinaan pepohon jam. Disebabkan kekurangan data-data litar dan perisian-perisian yang penting, kami memperkenalkan metodologi ujian yang berbeza untuk menguji kebolehpercayaan modul perisian *CAD* yang dicadangkan. Terdapat dua data ujian yang berbeza telah digunakan untuk mengenalpasti kewibawaan modul perisisan CAD tersebut. Keputusan ujian pada data-data rawak masukan menunjukkan pepohon jam yang disintesiskan oleh modul perisisan *CAD* dapat memuaskan semua kekangan pencongan jam, dan pada masa yang sama dapat mencapai panjangan wayar yang lebih pendek. Keputusan ujian pada data-data litar tanda aras menunjukkan modul perisian CAD kami berjaya mensintesiskan pepohon jam yang bukan sahaja dapat memuaskan semua kekangan pencongan jam, bahkan juga dapat mengurangkan tempoh jam litar.

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LIST OF SYMBOLS

VLSI	-	Very Large Scale Integration
CAD	-	Computer Aided-Design
EDA	-	Electronic Design Automation
IC	-	Integrated Circuit
PC	-	Personal Computer
GHz	-	Giga Hertz
UST	-	Useful-Skew Tree
ZST	-	Zero-Skew Tree
DME	-	Deferred-Merge Embedding
BB	-	Balanced Bipartition
SDR	-	Shortest Distance Region
FSR	-	Feasible Skew Range
ISCAS	-	International Symposium on Circuit and System
FF	-	Flip-Flop
Perl	-	Practical Extraction and Report Language
GUI	-	Graphics User Interface

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CHAPTER 1

INTRODUCTION

The thesis proposes a Computer Aided-Design (CAD) software module for useful-skew tree (UST) synthesis in deep-sub-micron VLSI integrated circuit design. The CAD software module is coded in *C* and *Perl*, and runs in a Microsoft Windows 2000 PC environment. In this chapter the project background, problem statement, research objectives, scope of work, and thesis organization are presented.

1.1 Background

The last few decades brought explosive growth in the electronics industry due to the rapid advances in integration technologies and the different benefits of large scale system design. The manufacturing capability and complexity, combined with the economic benefits of large electronic systems, are forcing a revolution in the design of these systems and challenging system designers who are involved in the design of integrated circuits. Integrated circuits today consist of hundreds of millions of transistors. Due to the tremendous increase in complexity, automating the design process has become a crucial issue.

The phase associated with the task of automatically designing a circuit using Computer Aided Design (CAD) tools is called Electronic Design Automation (EDA). The objective of the EDA research field is to fully automate the tasks for nearly every aspect of the development cycle, from the circuit specification and design entry

to the performance analysis, layout generation and verification. A large subset of problems in VLSI EDA is computationally intensive, and future EDA tools will require even more accuracy and computational capabilities. For a complicated problem in the modern VLSI design, an appropriate approach is to use a "divide-and-conquer" strategy, in which the whole design task is broken down into several sub-tasks (Sherwani, 1996). These sub-tasks are then more manageable to be solved using mathematical and heuristic techniques.

Due to the large number of components and the details required by the fabrication process, the physical design needs the help of computers. As a result, almost all phases of physical design extensively use CAD tools and many phases have already been partially or fully automated. The design is carried out in stages. The final circuit of such an IC can have up to a billion of components; it is delivered in a step-by-step manner. This is accomplished in several stages such as partitioning, floorplanning, placement, routing, and compaction. The different stages of physical design cycle are shown in Figure 1.1. A fully tested and error-free design at the switch level can be the starting point for a physical design. It is to be realized as the final circuit using (typically) a million components in the foundry's library.

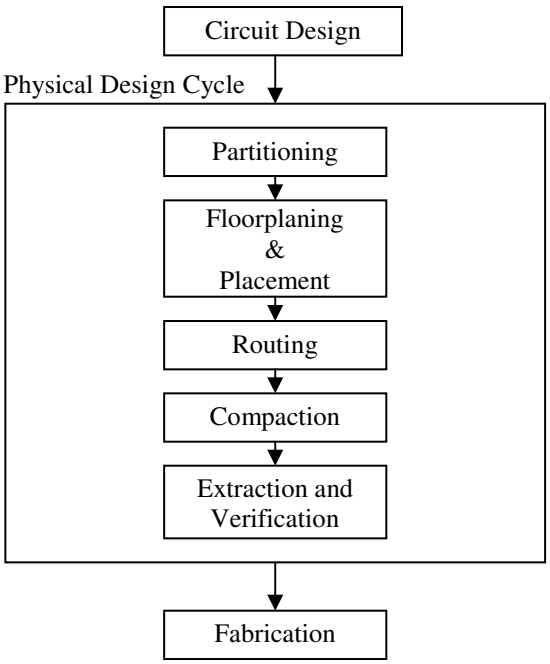

Figure 1.1: Physical design cycle

Among all the stages, routing is a difficult problem, and much research has been performed on this subject. This is because almost all problems in routing are computationally complex. Essentially, the task of routing stage is to complete the interconnections between blocks according to a specified netlist. The goal of a router is to complete all these circuit connections using the shortest possible wire length, routing with least number of layers and achieving timing optimization. This is usually performed in three phases, referred to as the Global Routing, Detailed Routing and Specialized Routing.

In physical design of VLSI system, there are two types of nets that need special attention in routing: Clock nets and Power/Ground nets. Clock nets need to be routed with great precision, since the actual length of the path of a net from its entry point to its terminals determines the maximum clock frequency on which a chip may operate. In a synchronous system, chip performance is directly proportional to its clock frequency. A clock router needs to take several factors into account, including the resistance and capacitance of the metal layers, noise and cross talk in wires, and the type of load to be driven. In addition, the clock signal must arrive simultaneously at all functional units with little or no waveform distortion. The clock is also known as major power-consuming net. The clock net is only about 4% of the total routing length of the entire interconnects, but power consumption of clock net is not minor (Magen *et al.*, 2004). In addition, compared to power and ground routing, clock routing is relatively more complex.

As a result, designing a clock distribution network has thus become critical not only for correct synchronization of data, but also can improve circuit performance and reduces power dissipation. Consequently, one of the challenges that EDA engineers have to face is to develop a new modeling capability and synthesis techniques that help to control the clock distribution network routing effectively.

1.2 Problem Statement

When the VLSI feature size becomes progressively smaller, moving into the Deep Submicron or Ultra-Deep Submicron Technology (sometimes, referred as nanometer VLSI) era, previously negligible variation effects start to affect circuit performance and yield significantly. Clock skew, is one of the variation effects that is always eliminated by previous clock distribution network design, where conventional clock designs have placed emphasis on seeking zero clock skew. Due to deep-sub-micron below 0.25 μm process, the long global interconnect lines become highly resistive as line dimensions are decreased. This increased line resistance is one of the primary reasons for the increasing significance of interconnection delay and now is of greater importance than the device delays. The interconnection delays eventually contribute to a large part of the clock signal delay. This leads to new problem to arise, as achieving a near-zero skew design is more and more difficult. Thus, the clock skew cannot longer be ignored. The control of clock skew can also severely limit the maximum performance of the entire system and create catastrophic race conditions in which an incorrect data signal may latch within a register.

As a result, in the modern high speed VLSI design era, clock design plays a crucial role in determining chip performance and facilitating timing and design convergence. Clock routing is important in the layout design of a synchronous digital system as it influences correctness, area, speed, power dissipation, power/ground supply noise, process variations and thermal issues of the synthesized system. Consequently, the automatic synthesis of the clock tree network has gained considerable attention in the design community.

The clock net is usually one of the first nets to be routed, and consequently block own routing areas for nets routed subsequently. As it is one of the largest nets, the area occupied is also a concern. Also, the clock net accounts for a significant fraction of the system power dissipation as it switches most frequently and is a large net. Carrying the heaviest load and switching at a high frequency, the clock typically dissipates about 40% of the total interconnect power in a synchronous digital system (Magen *et al.*, 2004).

In short, drastically increased requirements for high performance and high speed VLSI circuits have posed challenges to the clock routing design, where clock distribution network with elaborated timing characteristics and minimal wire-length is crucial for multi-GHz VLSI designs. However, today's CAD systems do not help much with the problems of time and often leave the final analysis to the designer. High performance clock design is indeed and area of active research.

Responding to the problem stated above, a CAD software module specifically for clock tree synthesis is proposed. By providing as inputs, the post-placement layout data, together with the data paths propagation delay and the clock pins' coordination and loading capacitance, a Useful-skew Tree (UST) is synthesized. The output clock tree data is written in a netlist file, which will contain the information on how the entire clock sinks are routed toward the clock source.

1.3 Objective

The objective of this thesis is to propose the development of a Computer Aided-Design (CAD) software module for Useful-skew Tree (UST) synthesis in deep-sub-micron VLSI integrated circuit design. The design of this CAD software module applies several routing algorithms, including the UST/DME algorithm for useful-skew tree generation, Balanced Bipartition (BB) method for abstract topology generation, and Deoker's graph-theoretic approach for clock skew scheduling.

1.4 Scope of Work

(i) A demonstration application prototype is developed to be used in the system validation of the proposed CAD software module.

(ii) Ideally, the clock tree synthesis should be performed on the post-placement layout data. Due to lack of availability of actual circuit data and necessary

software tools, the performance evaluation to our CAD software module is restricted to:-

(a) Actual circuit data, is applied with International Symposium on Circuits and Systems (ISCAS89) benchmark circuits which are re-created manually with Tanner Tools.

(b) The required data such as data path delays, coordination and loading capacitance of each clock pin is extracted, and then transformed manually to our CAD software module readable format.

(c) The reliability of synthesized clock tree is verified by manually comparing the computed skew value with the prescribed skew constraints.(as applying the synthesized clock tree to actual circuit layout is impossible to be performed in current stage)

1.5 Project Approach and Tools

Figure 1.2 illustrates the overview of project workflow to the development of the proposed CAD software module. On completing of the software sub-modules, the sub-modules are integrated and tested. The tests are conducted using (i) 3 randomized input data and (ii) actual circuit data of ISCAS89 benchmark circuit. A front-end GUI program is developed using *Perl* for use in demonstration of the results. Satisfactory outcomes from the performance evaluation successfully conclude the research.

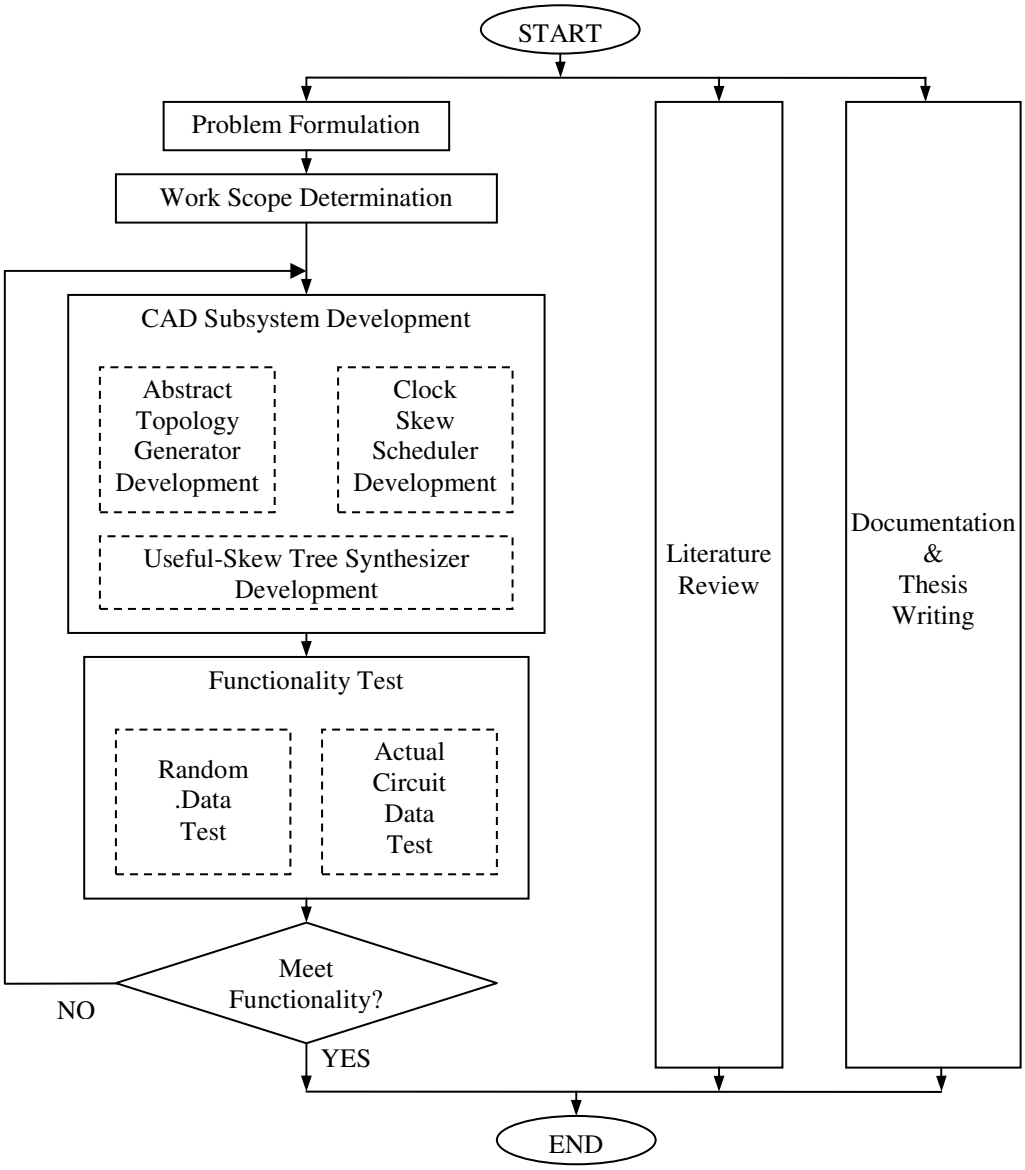

Figure 1.2: Project workflow of CAD software module development

The following software tools are used in this work.

i. Microsoft Visual C++ 6.0 – used to develop the entire core program of proposed CAD software module.

ii. *Perl* scripting – used to develop the netlist parsers and the front-end prototyping program.

iii. Tanner Tools – used to re-produce ISCAS89 benchmark circuit in layout drawing design.

1.6 Research Contribution

i. Investigation on the clock distribution network routing issue in deep submicron technology VLSI design, and systematic study on the clock skew scheduling and clock tree routing technique for an efficient implementation.

ii. Delivering a CAD software module for useful-skew tree synthesis where the synthesized clock tree layout is not only minimized in term of wire-length, but also fulfills the prescribed skew constraint values.

1.7 Thesis Organization

This thesis is organized into seven chapters. First chapter is the introduction chapter. It covers the background of the research, the problem statement, research objectives, scope of work, project approach and tools, and the significance of the research.

The second chapter reviews the fundamental concept of clock distribution network design research. It consists of some previous related research work and background theory.

Chapter three describes the algorithm of the abstract topology generation and clock skew scheduling algorithm. Both of the algorithms are used to pre-process the post-placement layout data so as to transform it to the required input data of UST/DME algorithm.

Chapter four focuses on the description of our main clock tree construction algorithm, UST/DME algorithm. The architecture design of the proposed CAD

software module is presented where the UST/DME algorithm is applied as the main engine of the useful-skew tree synthesis.

Chapter five delivers the detailed implementation work of the proposed CAD software module which is integrated from the useful-skew tree construction sub-module, abstract topology generation sub-module and clock skew scheduling sub-module.

In Chapter Six, the testing methodology is presented. We discuss on how the test platform is set-up and how the skew values of synthesized clock tree can be computed.

Chapter Seven shows the experimental results of the functionality test to the developed CAD software module. Part of *ISCAS89* benchmark circuits is used in the experiments.

The final chapter summarizes the research findings and suggests potential future work.

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