Design and Modeling of On-Chip Planar Capacitor for Radio Frequency Application

Mariyatul Qibthiyah Mohd Noor and **Mazlina Esa***

Microwave/RF and Antenna Research Group, Department of Radio Communication Engineering,
Faculty of Electrical Engineering, Universiti Teknologi Malaysia,
81310 UTM Skudai, Johor Darul Takzim, Malaysia.
Tel: +60-7-5535262, Fax: +60-7-5566272, Email: mazlina@fke.utm.my

Abstract

The on-chip RF capacitor is one of the key components for RF integrated circuit designs such as filters and oscillators. This paper presents the investigations performed on the design of an interdigital capacitor configuration for RFICs. Geometry design variables include number of finger, finger length, finger width, finger gap, end gap, terminal width, strip thickness, substrate height, metal types and dielectric constant. Quality factor is the essential parameter as it is an index for the efficiency of a capacitor's performance. The physical model of an interdigital capacitor is first determined. Then, its equivalent lumped circuit is simulated. The effects of parameter variations on quality factor and capacitance value are discussed and shown. An optimised interdigital capacitor can be obtained through their performances.

Keywords:

Interdigital Capacitor, Quality Factor, Capacitance, Radio Frequency

1. Introduction

Many research activities are focusing on the possibilities to migrate the radio frequency (RF) circuit to CMOS technology. The on-chip planar capacitor is one of the major areas of such investigations. Advances in CMOS fabrications have resulted in deep submicron transistors with higher transit frequencies and lower noise figure. The advanced performance of MOSFET is attractive for high frequency circuit design in view of a system on-chip realization, where digital, mixed signal baseband and high frequency transceiver blocks would be integrated on a single chip. The ability to integrate RF circuit with other analog and logic circuits provides great demand in the future applications. Capacitors have become ubiquitous in analog integrated circuits particularly owing to the switched capacitor technique for realization of analog to digital and digital to analog data converters and discrete time filters. [1]-[4] This paper investigates the design of interdigital capacitor. Geometry design variables include number of finger, finger length, finger width, finger gap, finger end gap, terminal width, substrate height, metal types and dielectric constant.

Corresponding Author. E-mail: mazlina@fke. utm.my
Tel: +60-7-5535262, Fax: +60-7-5566272

The optimum design of interdigital capacitor can be identified through the development of *Q*-factor contour plots. The research involves mathematical computation using MathCAD [5] and electromagnetic simulation using SonnetLite Plus [6]. Previous work are available in [7]-[18].

2. Computations Using MathCAD

The suitable geometry parameter value can be obtained from the mathematical analysis.

2.1 Solving of Formulation

From the desired design specification, the relevant formulations can be solved.

Firstly, from the formulation of quality factor, Q, set the desired Q of 240. Then, quality factor due to the conductor losses, Q_c, can be obtain as

$$Q_c = \frac{QQ_d}{Q_d \quad Q} = 6000 \tag{1}$$

Hence, the quality factor due to dielectric losses, Q_d, can be obtain from

$$Q_d = \frac{1}{\tan\delta} = 250 \tag{2}$$

where $tan\ \delta$ is the dielectric loss tangent. Then, the equation of Q_c is given by [7]

$$Q_c = \frac{1}{\omega CR} \tag{3}$$

From equation (3), with C = 0.2 pF and f = 5 GHz, the value of R is computed to be 0.0265. The equation of series resistance, R is given by the formulation [7]

$$R = \frac{4lR_s}{3w} \tag{4}$$

where R_s is surface resistivity and is given by [7]

$$R_s = \sqrt{\rho\pi\mu_o f} \tag{5}$$

A value of resistivity of the interconnect material, ρ, is set as 1.7x10^{-8} Ωm [8]. The permeability, μ_0, is 4π x 10^{-7} H/m. Therefore surface resistivity, R_s becomes 2.5906 x 10^{-7} Ω. From equation (4), the relationship between finger length, l, and capacitor width, w, can be expressed as

$$\frac{l}{w} = 1.08 \tag{6}$$

with w given by:

$$w = xn + s(n - 1) \tag{7}$$

Substituting equation (7) into (8) gives :

$$l = 1.08[n(x + s) - s] \tag{8}$$

The next step is to determine the dimensions of the interdigital capacitor.

2.2 Graphical Approximation Method

The graphical approximation method has been chosen in setting the suitable values for the design variables parameter. For the first analysis, l and s are fixed to 0.28 mm and 0.02 mm, respectively. From equation (8), suitable combination values for finger width, x, and number of finger, n, have been obtain as shown in Figure 1 and Table 1.

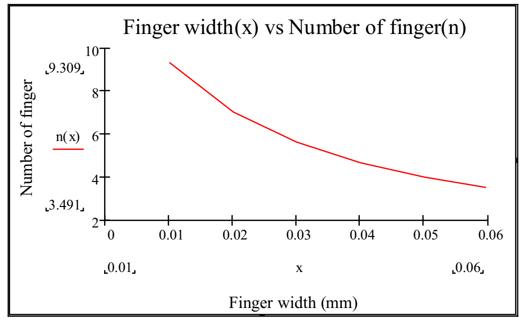

*Figure 1: **x** versus **n** when **l** and **s** are fixed*

*Table 1: Suitable combination values of **x** and **n***

Geometry Variable	Parameter Value			
x, mm	0.01	0.02	0.03	0.04
N	9.31	6.98	5.68	4.65

For the second analysis, the finger width, x, is fixed to 0.02 mm while the value of l remains. Therefore, suitable combination values for finger spacing, s, and number of finger, n, have been produced as shown in Figure 2 and Table 2.

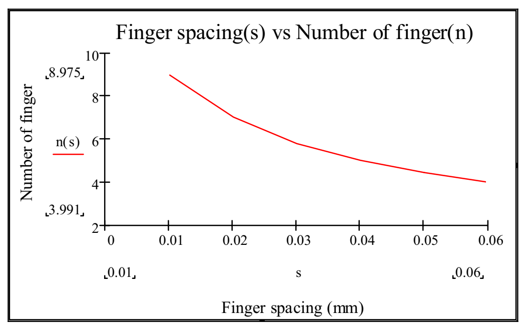

*Figure 2: **s** versus **n** when **l** and **x** are fixed*

*Table 2: Suitable combination values for **s** and **n***

Geometry Variable	Parameter Value			
s, mm	0.01	0.02	0.03	0.04
n	8.98	6.98	5.78	4.98

This third analysis is to determine the suitable combination values for n and l when both x and s are fixed to 0.02 mm. The behaviour is shown in Figure 3 and Table 3.

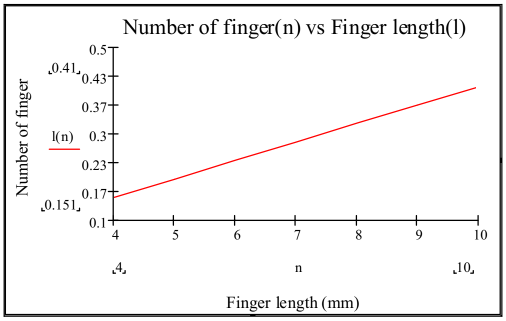

*Figure 3: **n** versus **l** when **s** and **x** are fixed*

*Table 3: Suitable combination values for **n** and **l***

Geometry Variable	Parameter Value		
n	6	7	8
l , mm	0.23	0.28	0.32

From the mathematical analysis, five interdigital capacitor designs have been created. All related variable parameters for these designs are shown in Table 4. Design 1 is set as the reference design.

Table 4: Design geometries of the interdigital capacitor

	x, mm	*s*, mm	*l*, mm	*n*, mm
Design 1	0.02	0.02	0.28	7
Design 2	0.04	0.02	0.28	5
Design 3	0.02	0.04	0.28	5
Design 4	0.02	0.02	0.24	6
Design 5	0.02	0.01	0.28	9

3. Simulation Result

3.1 SonnetLite Plus

By using an electromagnetic simulation software, the characterization of interdigital capacitor permits more flexibility during the design process. The effect of interdigital capacitor's geometry variations can be more easily analyzed.

3.2 Effect on Quality Factor and Capacitance

3.2.1 Design Comparison

For this analysis, Design 4 which has the smallest dimension produces the highest Q_{max} of 249.7868 and lowest capacitance value of 0.06065 pF. However, Design 1 is chosen as the basic design because the design fulfills the desired specification such as *Q* factor of more than 240, capacitance between 0.08 and 0.2 pF, and operating frequency from 2 to 5 GHz.

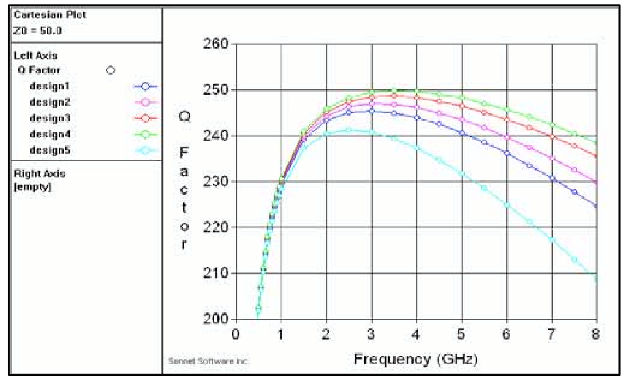

Figure 4: Effect on Q_{max} for different designs of interdigital capacitor

3.2.2. Number of Fingers

For the second analysis, several designs were created with different number of fingers i.e. 4, 5, 6, 8, 9 and 10, compared to Design 1 which has 7 fingers. The capacitance value increases with increasing number of fingers as shown in Figure 5. However, the *Q* factor is inversely proportional to *n*. As shown in Figure 6, smallest number of finger produces highest *Q* factor value. Approximately 1.73 % decrement of Q_{max} occurs when *n* increases from 7 to 10.

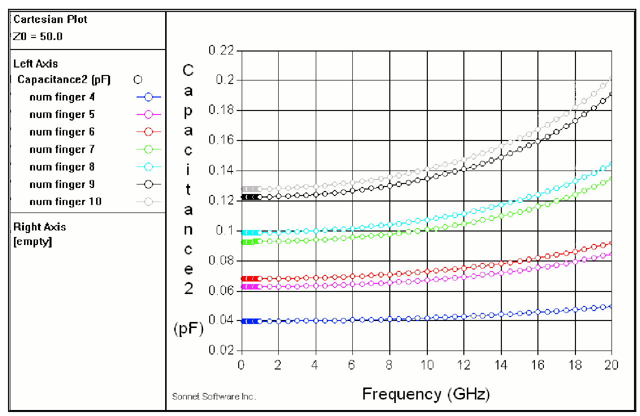

Figure 5: Effect on capacitance, C, value for different n.

3.2.3 Types of Metal

Several designs have been created using different metals to compare with Design 1 which uses copper as the metal layer. When better conductors are used, or metals with higher conductivity, the metallization loss is reduced but increased the *Q* factor value as shown in Figure 7 and Table 5. Different types of metals give low impact to the capacitance curve.

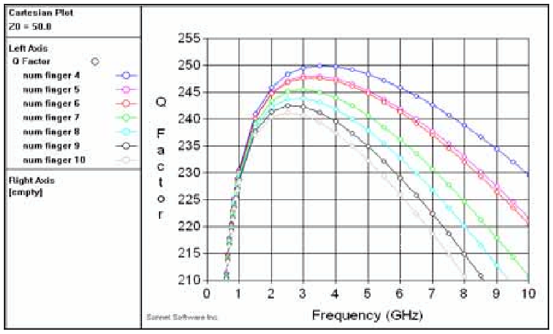

Figure 6: Effect on capacitance, C value for different n.

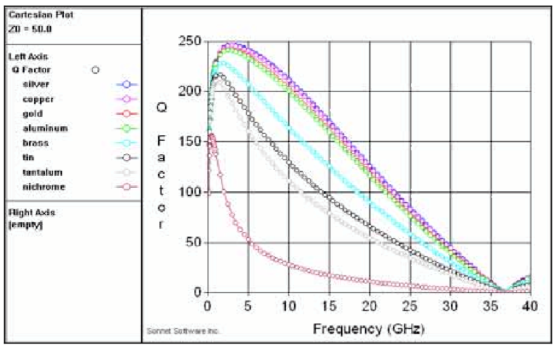

Figure 7: Effect on Q_{max} value for different types of metal

3.2.4 Finger length

Several designs using l = 0.06 mm, 0.10 mm, 0.20 mm, 0.34 mm and 0.40 mm were created to compare with Design 1 which uses l = 0.28 mm. Capacitance value increases when finger length increases. The design with l = 0.06 mm

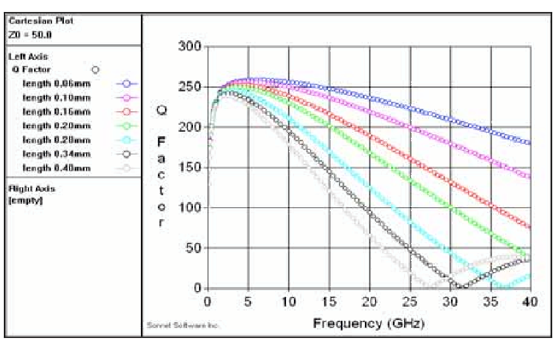

Figure 8: Effect on Q_{max} value for different l.

produces highest Q_{max} of 258.4685 which is approximately 5.32 % increment compared to Design 1. The results are shown in Figures 8 and 9. Shorter finger length reduces the series resistance that eventually leads to higher Q factor.

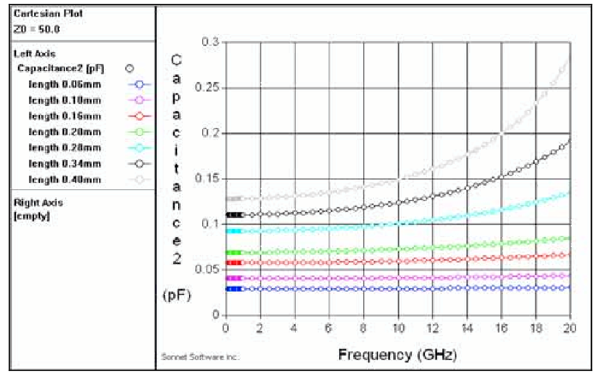

Figure 9: Effect on capacitance, C value for different l.

Table 5: Q_{max} value of different types of metal [8]

Metal Type	Conductivity, S/m	Q_{max}	Frequency at Q_{max}, GHz
Silver	6.17 x 107	245.94	3.0
Copper	5.8 x 107	245.40	3.0
Gold	4.09 x 107	241.90	2.5
Aluminum	3.72 x 107	240.85	2.5
Brass	1.57 x 107	228.03	2.0
Tin	8.7 x 106	216.60	1.5
Tantalum	6.45 x 106	209.82	1.0
Nichrome	1 x 106	156.52	0.45

4. Further Discussion and Conclusion

From the analysis, it can be summarized that Q_{max} increases with decreasing number of fingers, smaller finger length and higher metal's conductivity. In order to achieve high Q_{max}, finger length plays an important role because it affects more compared to other parameters. By using a small finger length of 0.06 mm, approximately 5.32 % increment of Q_{max} is observed. However, designs of small finger length produce low capacitances. As a result, a 0.28 mm finger length is an ideal value as the Q_{max} can reach 245.4057 at 3 GHz and at the same time produces capacitance, C of 0.093380 pF, which is considered as medium capacitance value.

The capacitance, C increases with increasing number of fingers and larger finger length. The metal's conductivity gives low impact to the capacitance. From the analysis, Design 5 with nine number of fingers, 0.28 mm finger length, 0.02 mm finger width and 0.01 mm finger spacing, produces the highest capacitance, C of 0.159 pF. The capacitance, C, value increases by approximately 70 % compared to the original design. However, larger finger length and more number of fingers will consume larger cost to the RFIC design.

From the investigations performed, it can be concluded that interdigital capacitor produces high quality factor in the range of 240 and medium capacitance value. The material properties and geometrical parameters for an interdigital capacitor are very important in order to optimize the quality factor and capacitance. The full investigation is reported in [19].

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