High-Frequency Transformer-Link Inverter with Regenerative Snubber

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***Abstract*—This work proposes a bidirectional high-frequency link inverter using center-tapped high-frequency transformer. The topology also incorporates a regenerative snubber to clamp the high voltage spikes due to the leakage inductance of the transformer. The closed-loop control method used is Deadbeat control, which provides fast response and low harmonic distortion, even under nonlinear loads. A 1kVA prototype inverter is built and the workability of the system is experimentally verified.**

***Keywords*—Bidirectional; Deadbeat control; HF transformer; Inverter; Pulse width modulation.**

I. INTRODUCTION

High-frequency link inverter is frequently used in dc/ac power conversion in which compactness and light-weight are of important considerations. For this type of inverter, the high-frequency transformer is used, resulting in a significant reduction in size and weight compared to the conventional 50Hz transformer inverter. However, it is well known that high-frequency link inverter has the problem of voltage spike at the transformer secondary. This is due to the presence of leakage inductance at the transformer secondary. When the current through the switch is turned off very quickly, the di/dt is very high, resulting in high voltage spike to appear across the switch. If not properly controlled, the spikes may result in the switch destruction.

In our previous paper [1], we have described a high-frequency link inverter using the center-tapped transformer. We have shown that this circuit utilizes fewer switches compared to the topologies proposed by [2] and [3]. However using the center-tapped transformer has one major drawback: the voltage across the switch at the transformer secondary is double relative to the noncenter-tapped type. As the voltage stress across the switch is already high, additional voltage spike can make the power switch vulnerable. The normal method to dampen the spike is to use a RCD snubber network, as shown in Fig. 1. However, for adequate spike suppression, the required snubber capacitor, C_s can be quite large. Consequently high discharge energy will be dissipated in the snubber resistor, R_s when the switch turns back on. This mandates for the use of high power R_s, which can lead to further loss of the inverter's efficiency.

High-frequency link inverters are now commonly used in uninterruptible power supply and renewable energy source systems. In these applications, the types of loads connected to the inverter are rather uncertain. Nonlinear loads such as rectifier in computer systems could cause intense distortion in the output current and voltage waveform. It is desirable that the inverter be able to maintain a sinusoidal output voltage waveform over all loading conditions. This can only be achieved by employing closed-loop control. Commonly, the Proportional-Integral-Derivative (PID) control method [4], [5] is used for closed-loop regulation of inverters. Although digital controllers using microprocessors and Digital Signal Processors (DSPs) have become more prevalent over analog based controllers, the discrete PID control is still adopted. Despite its simple structure, the PID controller is known to have a slow response.

In this paper, we propose an improvement to our previous work. We introduce a regenerative snubber network for the active rectifier that effectively reduces the spike to a very low value. Owing to the lossless nature (in the ideal case) of the snubber, the energy contained in the voltage spike is pumped back to the main power circuit. Besides, we also propose a fast Deadbeat controller for the inverter. As such, the system can handle critical loads such as rectifier load and triac load.

This paper is organized as follows: Section II describes the circuit configuration of the proposed inverter and regenerative snubber network, and the structure of the Deadbeat controller. Section III shows the hardware construction of the system. Section IV depicts the experimental results and discussions. Section V concludes the entire work.

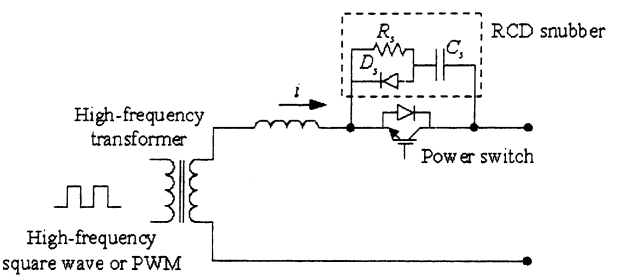

Figure 1. RCD snubber.

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II. SYSTEM DESCRIPTION

A. Power Circuit

The proposed bidirectional high-frequency link inverter is shown in Fig. 2. The timing diagram for the key waveforms of the power stage is illustrated in Fig. 3. At the first stage, the high-frequency PWM bridge converts the dc voltage to a 50Hz modulated Sinusoidal Pulse Width Modulation (SPWM) high-frequency ac voltage. Then, this voltage is isolated and stepped-up using a center-tapped high-frequency transformer. In the next stage, the high-frequency SPWM waveform is rectified using a center-tapped active rectifier. The active rectifier, which consists of power switches and anti-parallel diodes, enables bidirectional power flow. For transfer of power from the source, the diodes are utilised. For reverse power flow, the power switches $S3$ and $\overline{S3}$ are turned on. The rectified PWM waveform is then low-pass filtered to obtain the rectified fundamental component. Finally, using a polarity-reversing bridge, the second half of the rectified sinusoidal voltage waveform is unfolded at zero-crossing, and the sinusoidal output voltage waveform is obtained. By using center-tapped rectifier circuit, the number of bidirectional switches is reduced. Furthermore the polarity-reversing bridge utilizes only line-frequency (50Hz) switches.

B. Regenerative Snubber Network

Due to the leakage inductance and high di/dt, appreciable amplitude of voltage spike will be developed across the active rectifier switches during switching transitions. The normal practice to suppress this voltage spike is to place a RCD snubber across the switches. For effective damping, a relatively large snubber capacitor and a high power resistor is required. As a result, efficiency of the inverter will be reduced. In this work, we propose a regenerative snubber network as denoted by the dashed box in Fig. 2. The aim of the snubber circuit is to reduce the voltage spike across the active rectifier's switches ($S3$ and $\overline{S3}$) to a safe level. It comprises of a snubber capacitor, snubber diode and a transistor. Fig. 4 details the snubber network and its associated timing diagram.

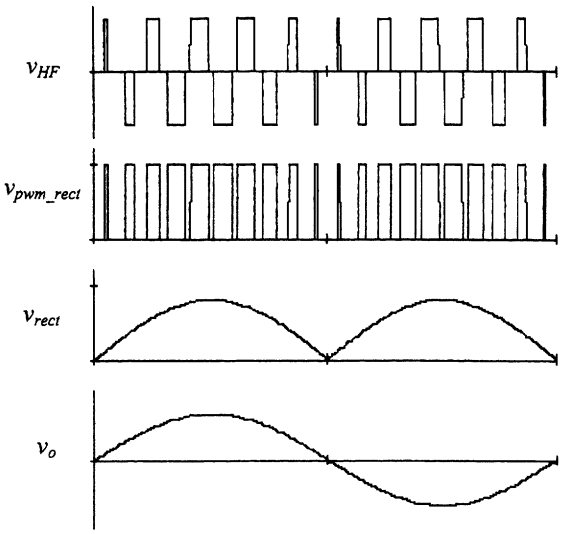


Figure 3. Key waveforms at different stages of the dc/ac conversion.

When the gate signal is applied to any of the rectifier's switch, voltage spike will appear on the adjacent (off) switch. This can be attributed to the energy stored in the leakage inductance of the transformer that appears as voltage spike with a sudden current turn-off. Assume the snubber diode (D_s) and snubber switch (S_s) are ideal, the voltage across snubber capacitor (C_s) without spike is v_1. When spike occurs, v_{pwm_HF} increases, thus causing D_s to be forward biased and charges C_s. The capacitor C_s dampens the voltage spike by reducing its di/dt. The charging process that takes place from t_1 to t_2 causes the capacitor voltage v_{cs} to rise. When v_{cs} equals v_2, i.e. when the capacitor voltage equals to v_{pwm_HF}, the charging process stops. Snubber diode D_s is reverse biased and C_s starts to discharge its energy into the power circuit via S_s. The discharging process continues until end of the PWM pulse. When the PWM pulse has ended, S_s is turned off, and the discharging process stops. Voltage v_{cs} is maintain at its equilibrium level (v_1) until the next charging process occurs.

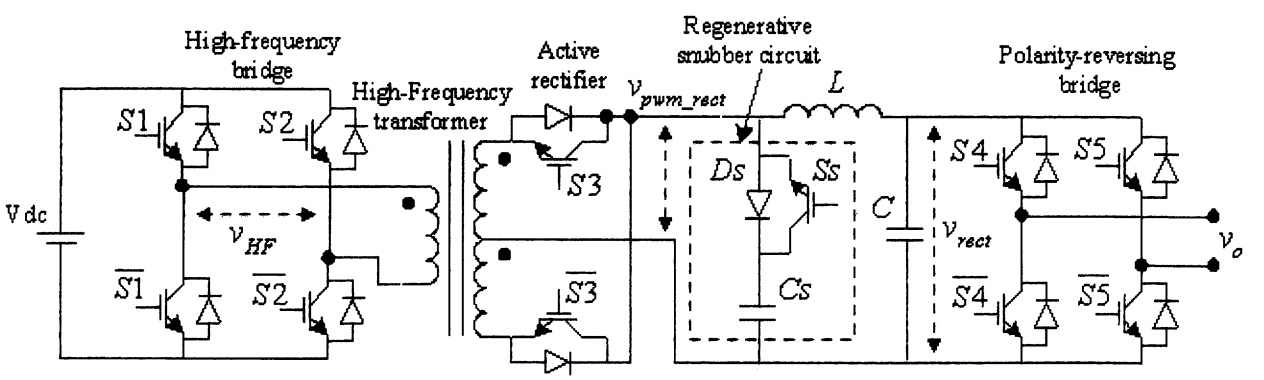


Figure 2. Block diagram of the proposed inverter.

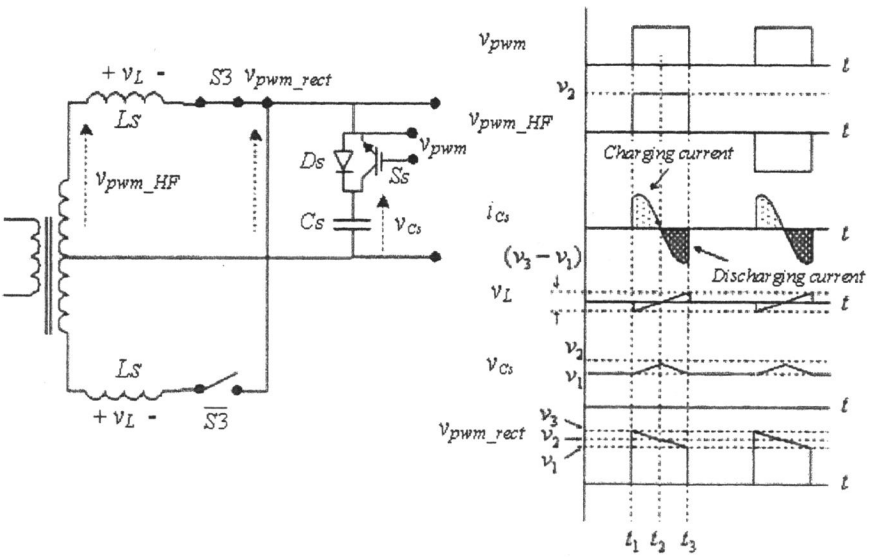


Figure 4. Circuit of regenerative snubber network and the associated timing diagram.

C. *Deadbeat Controller*

Deadbeat control is a discrete-time control technique that provides fast dynamic response [6], [7]. In Deadbeat control, any nonzero error vector will be driven to zero in at most n sampling periods, where n is the order of the closed-loop system [8]. In this work, a multirate Deadbeat controller is used for closed-loop regulation of the high-frequency link inverter.

Referring to Fig. 2, it is assumed that the V_{dc} is constant. The switching frequency is considered to be high enough compared to the modulating frequency. The high-frequency transformer is assumed to be operating in the linear area. Therefore, the PWM bridge and the transformer can be modeled as constant gains. The polarity-reversing bridge is only operated at 50Hz, thus can be ignored. With these assumptions, the dynamics of the system can be simplified to a LC low-pass filter connected to the load. Choosing v_{pwm_rect} as the input voltage of the system, filter inductor current i_L and filter capacitor voltage v_{rect} as the state variables, the state-space model of the system is derived:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{rect}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_{rect} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{pwm\_rect} + \begin{bmatrix} 0 \\ -\frac{1}{C} \end{bmatrix} i_{or} \quad (1)$$

$$v_{or} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_{rect} \end{bmatrix} \quad (2)$$

where v_{or} is the rectified sinusoidal output voltage.

The controller is designed based on the state-space model, as shown in Fig. 5. It consists of current and voltage loop with decoupling networks. The decoupling networks are used to compensate disturbances and improve robustness of the overall system.

Fig. 6 shows the current loop controller. The output voltage decoupling network is used to compensate the disturbances caused by the output voltage. With further simplification and discretization, the closed-loop transfer function of the current loop is obtained:

$$C_i(z) = \frac{i_L}{i_{ref}} = \frac{K_i\left(\frac{T_i}{L}\right)z^{-1}}{\left[K_i\left(\frac{T_i}{L}\right)-1\right]z^{-1}+1} \quad (3)$$

To achieve Deadbeat response, where $i_L = z^{-1} i_{ref}$, the current loop gain, K_i is designed as:

$$K_i = \frac{L}{T_i} \quad (4)$$

Fig. 7 shows the voltage loop controller. The load current decoupling network is used to compensate the disturbances induced by the load current. This improves the robustness of the system towards load variations, allowing different types of loads to be connected. The design procedure of the voltage loop controller is similar to the current loop controller. The closed-loop transfer function of the voltage loop is:

$$C_v(z) = \frac{v_{or}}{v_{ref}} = \frac{K_v\left(\frac{T_v}{C}\right)z^{-1}}{\left[K_v\left(\frac{T_v}{C}\right)-1\right]z^{-1}+1} \quad (5)$$

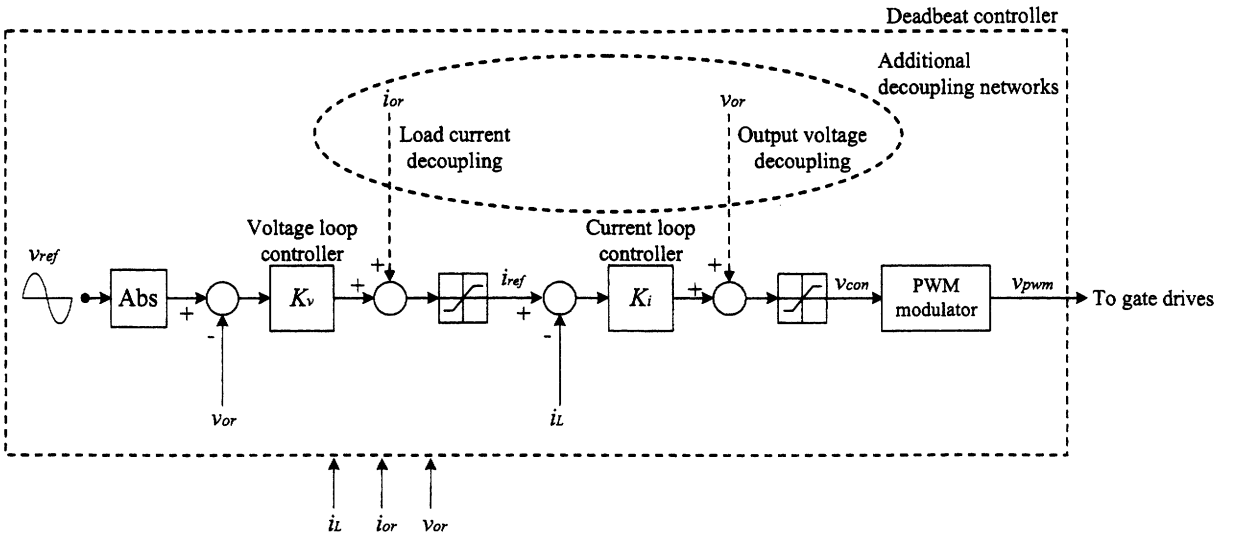


Figure 5. Deadbeat controller for the high-frequency link inverter.

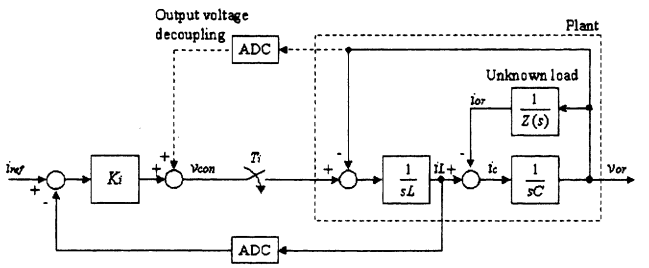


Figure 6. Current loop controller.

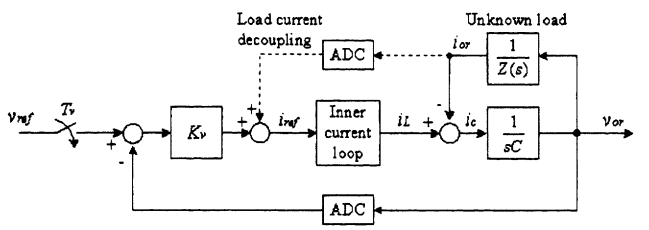


Figure 7. Voltage loop controller.

To ensure Deadbeat response of $v_{or} = z^{-1}v_{ref}$, the voltage loop gain, K_v is designed as:

$$K_v = \frac{C}{T_v} \tag{6}$$

III. Hardware Construction

A 1kVA prototype inverter has been constructed. Fig. 8 shows the photograph of the constructed prototype. The high frequency bridge is constructed using the APT15GP60BDF1 power IGBT. It is a low conduction loss device with good switching capability. The power transformer is wound on the ETD59 ferrite core. The active rectifier's switch is built using the IRG4PH40K IGBT and STTA1212D ultrafast high voltage diode. These power switches can withstand 1200V, thus suitable to be used at the center-tapped active rectifier. The polarity-reversing bridge is constructed using the IRG4PC40FD IGBT. Since almost all the surge voltages have been dampened before entering the polarity-reversing bridge, the chosen power switches are only rated at 600V. Using low voltage IGBT, the forward conduction losses can be minimized. The snubber capacitor is chosen to be 2.2μF, and the snubber switch is an IRF730 MOSFET. Each power transistor is driven by a Hewlett Packard gate driver chip, HCPL3120.

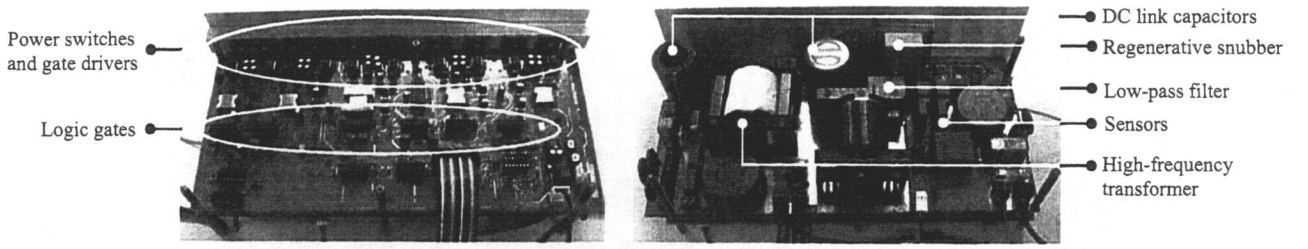
DS1104 DSP board from dSPACE (64-bit floating-point processor with TMS320F240 Slave DSP) is used to implement the Deadbeat controller. It is also used to generate the control signals for the active rectifier, v_s and the polarity-reversing bridge, v_u. The control signals are shown in Fig. 9. Hall effect current sensors, HY10-P and voltage sensor, LV25-P are used for feedback signals sensing. The signal conditioning such as noise filtering and signal amplification are performed in software using the DS1104 DSP.

IV. Experimental Results and Discussions

Laboratory experiments have been carried out to verify the viability of the proposed inverter. The specifications of the inverter are as follows:

- Input voltage ranged from 130V to 150V.
- Sinusoidal output voltage 220 to 250V_{rms}, 50Hz.
- Nominal output power of 1kW.

The output voltage and current waveforms for resistive and inductive loads are shown in Fig. 10(a) and (b) respectively. The latter oscillogram indicates that the inverter is capable of carrying bidirectional power flow. Thus, the inverter is suitable for stand-alone power supply applications.



(a) Top view – gate drive and signal conditioning circuits

(b) Bottom view – power circuit

Figure 8. Photograph of the prototype inverter.

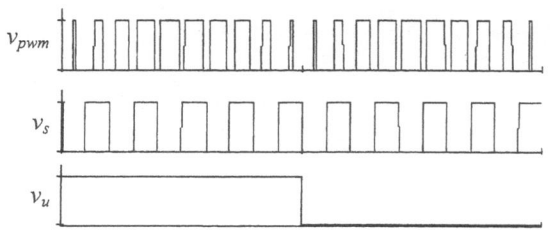
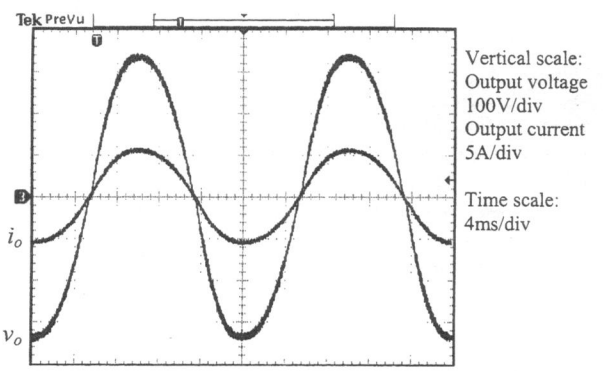
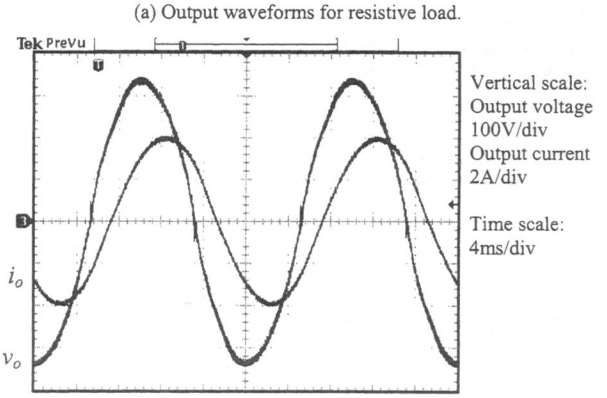


Figure 9. Control signals of the power switches.



(a) Output waveforms for resistive load.



(b) Output waveforms for inductive load.

Figure 10. Output waveforms for resistive and inductive loads.

Fig. 11 shows the key waveforms that depicts the operation of the regenerative snubber. It can be seen that the snubber capacitor is charged and discharged in synchronized with the PWM pulse. The result obtained from the experimental rig is in very close agreement with the theoretical prediction.

Fig. 12 shows the active rectifier's switch (*S*3) collector-emitter voltage (V_{CE}) before and after insertion of the regenerative snubber. It can be seen that before the regenerative snubber is inserted, the voltage overshoot is about 40% of the amplitude. After the insertion of the regenerative snubber, the spike has been reduced to a negligible value.

Fig. 13 compares the inverter efficiency between the regenerative snubber and the conventional RCD snubber. For the latter, the values of C_s and R_s are chosen to be 2.2nF and 22Ω, respectively. The chosen values for the RCD snubber components are rather conservative; typical values are much higher than these. From the figure, it can be seen that the regenerative snubber is able to increase the efficiency of the inverter by about 5%. A higher value for RCD components will make the difference even larger.

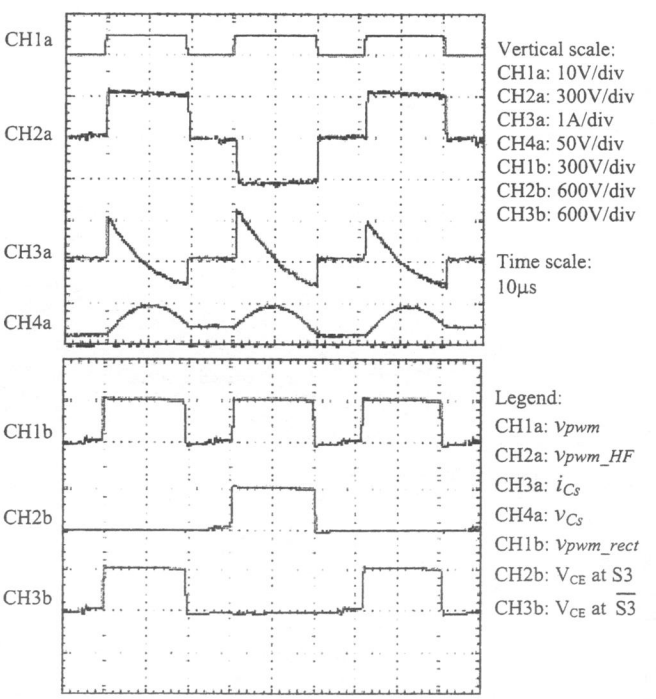
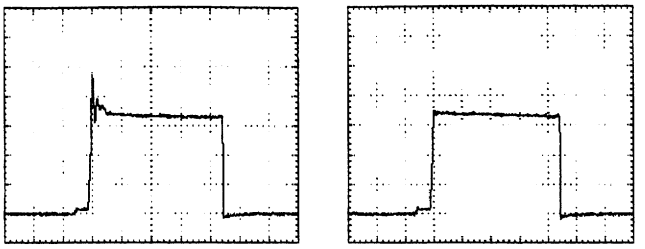


Figure 11. Key waveforms of the snubber operation.



Vertical scale: 200V/div
Time scale: 5μs/div
(a) V_{CE} of $S3$ without snubber

Vertical scale: 200V/div
Time scale: 5μs/div
(b) V_{CE} of $S3$ with snubber

Figure 12. V_{CE} at $S3$ before and after the insertion of regenerative snubber.

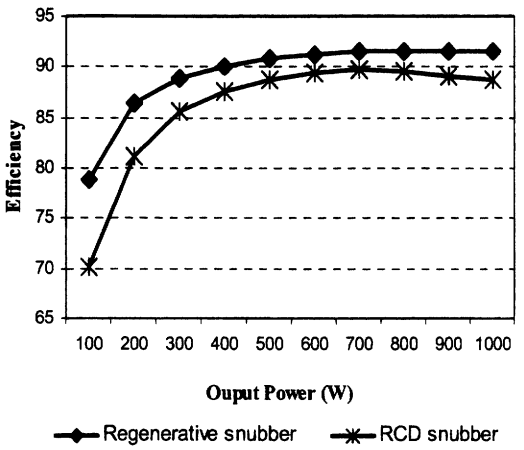


Figure 13. Efficiency vs output power.

Fig. 14 shows the output voltage and current waveforms under step load change for resistive load. A triac load is used as the load. It can be seen that the voltage drop can be recovered quickly even under large current transient.

To test a worse-case loading, the system is connected to a full-bridge rectifier load, with a capacitor filter, C_d and resistive load, R_d of 470μF and 500Ω respectively. The steady-state result is shown in Fig. 15. It can be seen that the sinusoidal output voltage is maintained although the load current is highly distorted.

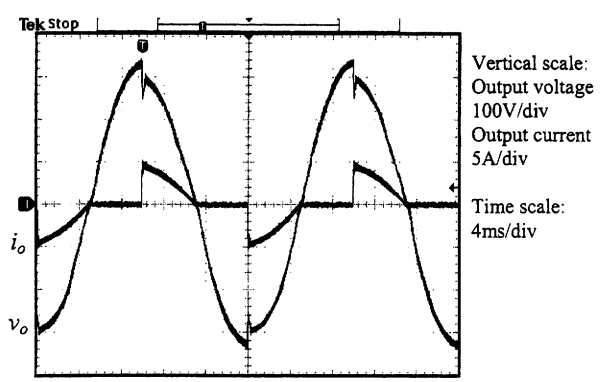


Figure 14. Output waveforms for triac load.

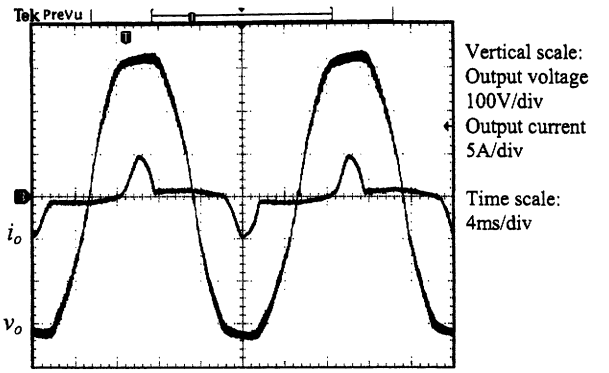


Figure 15. Output waveforms for full-bridge rectifier load.

V. CONCLUSION

This paper has described the high-frequency link inverter with a regenerative snubber and digital closed-loop controller. To prove the concept, a 1kVA prototype inverter is constructed. From the experimental results, it was found that the snubber network functions as predicted. The voltage spike across the active rectifier's switch is reduced significantly. This increases the overall efficiency of the inverter. Besides, the Deadbeat controller exhibits excellent dynamic response with low harmonic distortion, even under highly nonlinear loads. It is thus concluded that the proposed inverter is suitable for wide area of applications, both in stand-alone and grid-connected configurations.

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