The Instability Effect of Constant Power Loads

Awang bin Jusoh

Abstract-- **The sub-system interaction and instability phenomena is a common problem in the Distributed Power System (DPS). The interaction arises because each individual converter has internal control function such as to regulate the converter output voltage, which results in the converter tends to draw a constant power and therefore has a negative incremental input impedance. The constant power and negative input resistance characteristic potentially have a de-stabilising effect on the electrical supply system. The paper presents the analysis, theoretical design and simulation of a simple DC DPS. The analysis of the LC filter and its damping parameters were given. The effect of the negative input resistance of the CPL on the filter was analysed using small-signal input resistance of the load. The passive damping method was used to reduce the system interaction between the converters. The results were verified by MATLAB Simulink simulation.**

Keywords—**Constant power load, negative incremental resistance, passive damping**

I. INTRODUCTION

Over the past few years, there has been extensive research into sub-system interaction and instability phenomena in Distributed Power Systems (DPS). A DPS is a system, usually DC, where the power processing functions are distributed among many power processing units or DC/DC converters at the point of need. The distributed system is increasingly being used in applications such as aircraft, spacecraft, hybrid-electric and electric vehicles, ships, defence electronic power systems, industrial production lines, communication and computer systems and many more due to its beneficial in terms of weight, size, isolation, voltage regulation, flexibility, capability to integrate a large variety of loads and also enables one to control more easily the quality of power reaching each separate board [1-2]. However DPS has some drawbacks such as interaction between the converters and bus instability, as well as imbalance in power distribution among parallel converters, which leads to an unequal distribution of output current hence may create excessive stress on some of the modules and increase their rate of failure.

A. The Causes of Distribution System Instability

When two stable sub-systems are combined or integrated together, there is no guarantee that the combined system will be stable, there may be an interaction between the interconnected sub-systems, which can result in instability in the system. Even though the sub-systems may be well designed for stand-alone operation, the possible interactions may still occur once the sub-systems are integrated [3-4]. This is because the individual sub-systems such as a switching regulator were mainly stand-alone units operating from a low source impedance and driving a passive load. But nowadays since the cost has reduced, switching regulators are more widely used in many applications. Very often with one switching regulator serving as the source for several other converters, for example switching regulators, inverters and motor drives, the potential for load-source interaction is therefore very high. The interaction arises because each individual converter has internal control functions, such as the regulation of the converter output voltage or motor speed. As a result, the converter tends to draw a constant power and therefore has a negative incremental input resistance within the bandwidth of the converter control loop. When the source voltage falls, then the operation of the internal controller results in the converter drawing more current. This in turn could cause the source voltage to fall even further.

The oscillation can be predicted when the input and output impedance of the converters are known. If one consider a simple RLC series circuit, the magnitude and phase plot of the circuit impedance is given in Fig. 1. The parameters used are R = 1Ω , C = 300 μF, and L = 150 mH. The plot shows that at low frequencies, the circuit behaves like a capacitor and has a phase of -90°. At high frequencies, the circuit behaves like an inductor with a phase of +90°. At the resonant frequency $\omega_o = \frac{1}{\sqrt{LC}}$, the phase of this circuit passes through zero degrees, and the impedance is equal to R. If the resistor is very small, then at this frequency a very large current would flow due to a very small voltage.

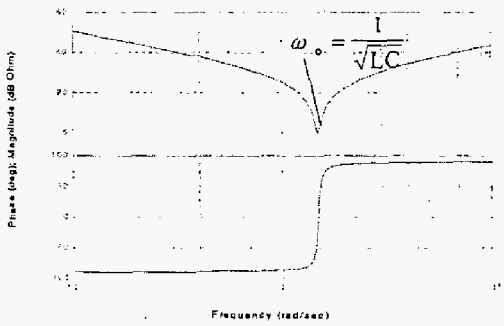

Fig. 1. Magnitude and phase plot for the impedance a simple RLC circuit

Furthermore, if the resistance is very small the poles of the system will almost lie on the imaginary axis in the complex plane, implying that the natural response of the circuit would exhibit slowly decaying oscillations at a frequency of approximately ω_o. The oscillation would continue in the circuit until all the energy is dissipated in the resistor, and with zero resistance the oscillation would continue indefinitely.

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When an L-C filter which has a fairly small resistance, for example due to the winding resistance of the inductor, is connected to a constant power load, the negative resistance characteristic of the load will tend to reduce the filter resistance, producing a more oscillatory system. With a sufficiently large constant power load the system would become unstable, the oscillations would grow exponentially.

B. Negative Input Resistance Phenomenon

A block diagram of a constant power load such as an induction motor drive (IMD) or DC-DC converter is shown in Fg. 2.

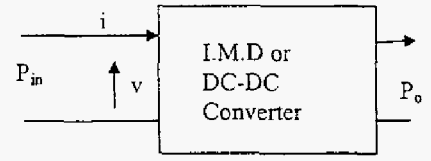

Fig. 2. Constant power load block diagram

The static input voltage v- current i characteristic for the load is shown in Fig. 3, since P_{in} is a constant the plot is a hyperbola.

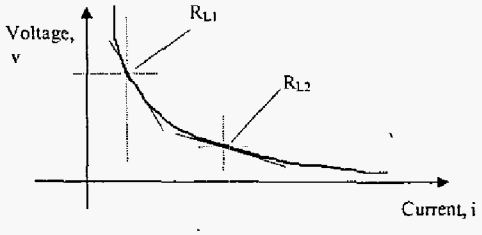

Fig. 3. Constant power load and static input voltage: current characteristic

The input resistance R_L is given by the ratio of small-signal changes in input voltage over the small-signal input current, $R_L = \frac{\Delta v}{\Delta i}$ and this value will depend on the converter operating point. This diagram shows two different values of input impedance, R_{L1} and R_{L2}, at two different operating points. As shown in the graph, the slope of this characteristic is negative, therefore the resistance of the converter is known as a negative input resistance where any increment in input voltage will cause a decrease in the input current and vice versa.

The negative input resistance can be calculated as follows. It is known that the input power and output power of a CPL are equal, that is $P_{in} = P_o = P = vi$ and $v = \frac{P}{i}$. Differentiating the voltage with respect to the current yields

$$\frac{dv}{di} = -i^{-2}P = -\left|\frac{P}{i^2}\right| = -\left|\frac{v^2}{P}\right| = -R_L \qquad (1.0)$$

Equation 1.0 shows the general equation to calculate the small-signal input resistance of a constant power load. The resistance is negative as expected and is also non-linear, depending upon the current and voltage. The negative impedance of the input converter would definitely causes instability in the system.

II. ANALYSIS

A. Stability Analysis of Impedance Based Criterion

The analysis of the impedance based stability criterion proposed by Middlebrook has been carried out in [5], and is summarised here. Fig. 4 shows a simple system consisting of a single source and a single load connected to an interface bus. In this circuit, V_{ts} ,Z_s, V_{tL} and Z_L represent the Thevenin equivalent voltage of the source, impedance of the source, voltage of the load, and impedance of the load respectively. The interface bus voltage is given by v, and the currents to the source and load are given by, I_s, and I_L, respectively.

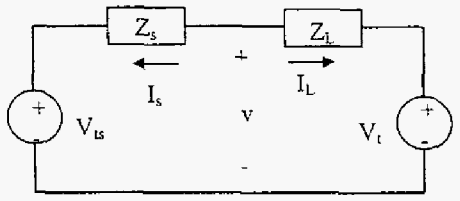

Fig. 4. Impedance based stability criterion circuit

The voltage at the interface, v is given by

$$v = \frac{N_L D_s V_{ts} + N_s D_L V_{tL}}{N_L D_s \left[1 + \frac{N_s D_L}{D_s N_L}\right]} = \frac{N_L D_s V_{ts} + N_s D_L V_{tL}}{N_L D_s \left[1 + \frac{Z_s}{Z_L}\right]} \qquad (2.0)$$

Where N_s, and D_s, denote the numerator and denominator of the source impedance, and similarly N_L and D_L for the load. A reasonable assumption was made for the load to operate in a stable fashion with fed from an ideal voltage source and for the source, it should be able to operate in a stable fashion if the load is a constant current source

Equation 2.0 shows that if N_L and D_s do not have any roots in the right half plane, the system is stable provided that the Nyquist contour of $\frac{Z_s}{Z_L}$ does not encircle the (-1,0) point. Based on the impedance stability criterion given by Middlebrook, if the magnitude of Z_s is always less than the magnitude of Z_L, there could not be an encirclement of the (-1,0) point of the Nyquist plot. This is a commonly used design guideline.

B. Analysis of L-C Filter with CPL and Passive Damping

The L-C filter with CPL and passive damping is shown in Fig. 5. Assuming $C_2 >> C_1$ then at higher frequencies the impedance of C_2 will be very small and the total resistance connected to the output of the filter will be given by the parallel combination of R and $-R_L$, having a value

$R_{eff} = \frac{-|R|.|R_L|}{|R|-|R_L|}$. Looking at this relationship, if $|R_L| < |R|$, the L-C filter will have a net negative damping resistance and the filter will oscillate. Therefore to ensure system stability, the magnitude of the damping resistor, R, must be lower than the magnitude of the load impedance as noticed by Middlebrook in his impedance stability criterion.

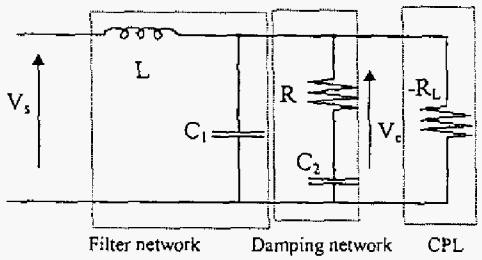

Fig. 5. L-C filter with CPL and passive damping network

The analysis of the circuit is undertaken by considering the input-output voltage transfer function $V_c(s)/V_s(s)$ for the system of Fig. 5, given as equation 3.0

$$\frac{\frac{(1+sC_2R)}{LC_1C_2R}}{s^3+s^2\left(\frac{C_1R_L+C_2R_L-C_2R}{C_1C_2RR_L}\right)+s\frac{(C_2RR_L-L)}{LC_1C_2R_LR}+\frac{1}{LC_1C_2R}} \qquad (3.0)$$

By equating denominator equation 3.0 equal to zero, the plot of the pole movements as the damping resistor R is varied is shown in Fig. 6.

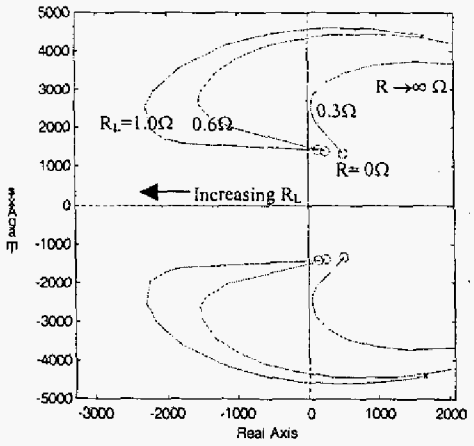

Fig. 6. Pole locus as damping resistor R is varied for various CPLs

Plot in Fig. 6 shows the locus of the system poles as the damping resistor R is varied from zero to infinity. The same filter component values were C_1=300 μF and L=150 μH, and the series DC blocking capacitor C_2 was fixed at $10C_1$ = 3 mF. C_2 is normally chosen at least four times bigger than C_1. The small-signal resistance of the constant power load was set at R_L=0.3 Ω, 0.6 Ω , and 1.0 Ω for the three curves in figure 6, corresponding to constant power levels of 243 kW, 122 kW and 73 kW respectively with a DC source voltage of 270 V.

The poles are in the right half plane for a damping resistor of zero and infinity. As the damping resistance varies between zero and infinity the poles move to the left, and may cross into the left-half plane, as in the case for R_L = 0.6 Ω and 1.0 Ω. With R_L = 0.3 Ω the system remains unstable for all values of damping resistance, showing the limitation of the approximate stability condition derived earlier, namely $R < |R_L|$.

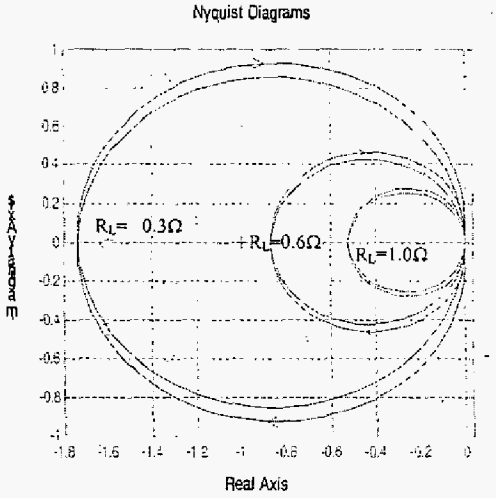

Figure 7. Nyquist plot of impedance ratio, $\frac{Z_s}{Z_L}$

Fig. 7 shows the system stability by using the impedance ratio criterion, that is the plot of Nyquist locus of Z_s/Z_L. In this case Z_s is the output impedance of the filter and damping network, figure 5, which is

$$\frac{sL(1+sRC_2)}{s^3LRC_1C_2+s^2L(C_1+C_2)+sRC_2+1},$$

and Z_L is $-R_L$.

Identical parameters were used as in plot of figure 6, with R = 0.51 Ω. With R_L = 0.3 Ω the locus circles the (-1,0) point indicating system instability, but with the higher values of R_L the system is stable.

III. DESIGN OF PASSIVE DAMPING

Approximate passive damping resistor is designed to ensure the stability of a system connected to a CPL. By approximately factorised the characteristic equation of equation 3.0, equation 4.0 was derived and equation 5.0 shows the multiplied out of equation 4.0

$$\left(s+\frac{1}{C_2R}\right)\left(s^2+s\frac{1}{C_1}\left[\frac{R_L-R}{R_LR}\right]+\frac{1}{LC_1}\right) \qquad (4.0)$$

$$s^3+s^2\left(\frac{C_1R_L+C_2(R_L-R)}{C_1C_2R.R_L}\right)+s\frac{(C_2RR_L+\frac{L}{R}[R_L-R])}{LC_1C_2R_LR}+\frac{1}{LC_1C_2R} \qquad (5.0)$$

Comparing equation 5.0 and equation 3.0, we see that an extra term of $s\frac{LR_L}{R}$ has appeared. Since the approximate condition for stability is that $R_L > R$, then for the approximation in equation 5.0 to be valid requires that $C_2RR_L >> \frac{LR_L}{R}$ resulting in

$$C_2 >> \frac{L}{R^2} \qquad (6.0)$$

Therefore the design procedure is to choose R such that the effective resistance in the quadratic portion of equation 5.0 provides satisfactory damping of the complex poles, then C_2 must be chosen to ensure that equation 6.0 is satisfied. For example to place the complex poles on the 45° line in the s-plane, then the magnitudes of the real part and the imaginary part of the quadratic characteristic equation of equation 5.0 must be equal. This results in the damping resistor R being given equation 7.0

$$R = \frac{R_L\sqrt{LC_1}}{\sqrt{LC_1} + \sqrt{2}C_1R_L} \qquad (7.0)$$

IV. SIMULATION RESULTS

Fig. 8 shows the system simulation circuit, consists of L-C filter, CPL and passive damping, with a positive 50 V step in input voltage V_s. The components used are shown clearly. The damping network was chosen to place the complex poles on the 60° line in the complex plane, using equation 7.0, the values being a damping resistor of 0.7 Ω and a series blocking capacitor of 1200 μF. Plots in figure 9 and 10 show that both current and voltage experience a single overshoot and then quickly settle to the steady-state value, illustrating the effectiveness of the damping network.

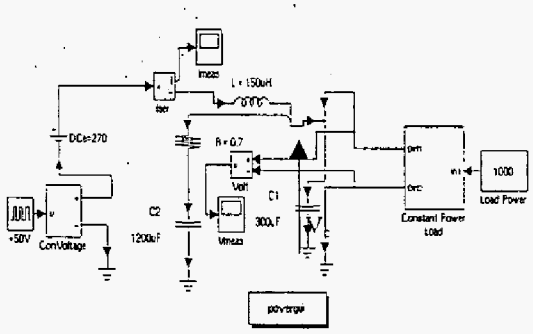

Fig. 8. System simulation circuit diagram

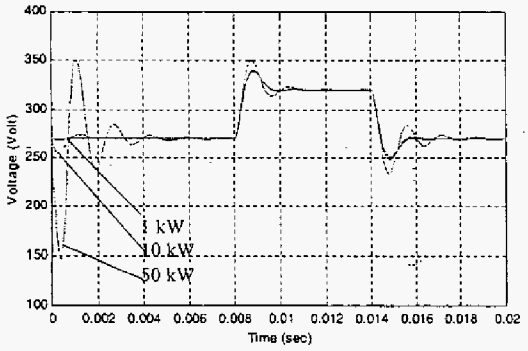

Fig. 9. Simulated plot of bus voltage, V_c for three CPL power values

Both plots show that the system is well damped at the low power level. At higher power levels such as 50 kW, the system starts to show oscillatory behaviour, the responses being more lightly damped with V_s= 270 V as expected, since the small-signal resistance of the CPL has a lower magnitude under these conditions.

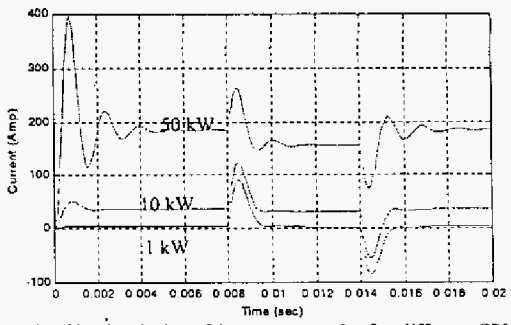

Fig. 10. Simulated plot of input current, I_L, for different CPL power levels

To compare the simulation results with the small-signal analysis, the simulation was repeated for a small step in V_s of 5 V. The CPL power level was taken to be 50 kW, giving a small-signal resistance of 1.5 Ω. The simulation result, figure 11, shows the magnified plot at 8 ms. Fig. 12 shows the corresponding step response generated by MATLAB using equation 3.0. The overshoot and natural frequency of the responses is again seen to be very close.

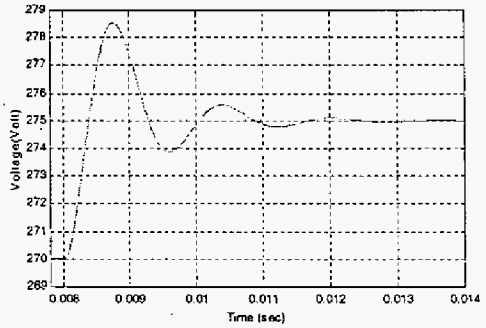

Fig. 11. Magnified plot of simulated CPL voltage, V_c

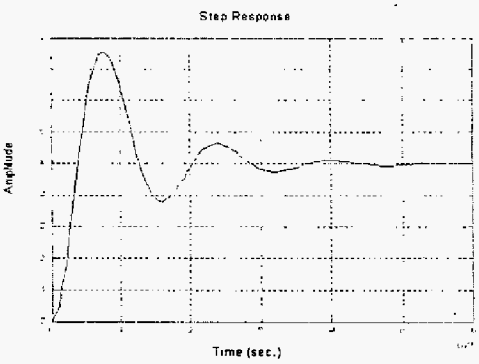

Fig. 12. Theoretical 5 V step response of CPL voltage, V_c

Step changes in the CPL power have also been simulated. The simulation circuit diagram used is the same as in figure 8, but now the CPL power block is changed to a step-up power transient. CPL power is stepped up from 1 kW to 10 kW, 20 kW and 50 kW at time 8 ms. Fig. 13 and Fig. 14 show the input current, i_L and capacitor voltages V_c for the same power transients.

Fig. 13 shows that as the power is increased at 8ms, the system experiences an overshoot and oscillation before

settling at the final conditions. At lower CPL power, the system is well behaved such as a power step to 10 kW. However as the power increases, greater overshoot and more oscillation occurs. The system will become unstable if the CPL power is increased too far.

A similar pattern is seen in the simulation results for the capacitor voltage V_c, the power transient causes a sudden drop in voltage as the CPL starts to draw more current. The voltage then goes through a resonant transient, settling back to 270 V. The higher values of load power result in larger amplitude transients and more lightly damped behaviour.

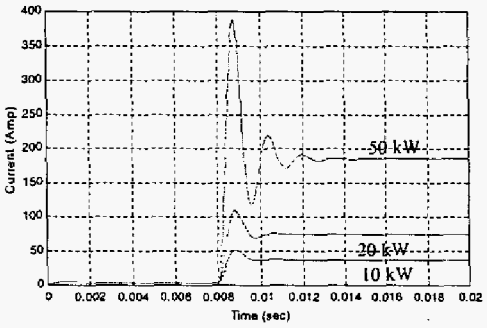

Fig. 13. Simulated input current, i_L, as the power level steps-up

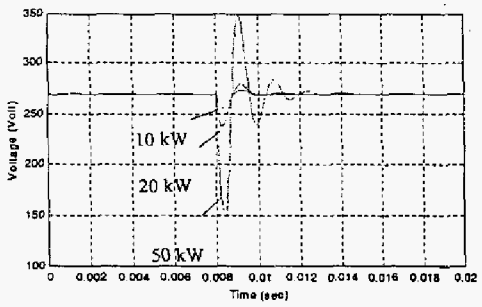

Fig. 14. Simulated capacitor voltage, V_c, as the power level steps-up

To compare the simulation results with the small-signal analysis, the simulation was repeated for small increases in CPL power of 500 W, giving a 2A increases in current with voltage of 270 V. The CPL power level was taken to be 10 kW, giving a small-signal resistance of 7.3 Ω. The magnified simulation result of V_c at 8ms is shown in Fig. 15 and Fig. 16 shows the corresponding step response generated by MATLAB due to a 2A step in i_L. The overshoot and natural frequency of the responses is again seen to be very close.

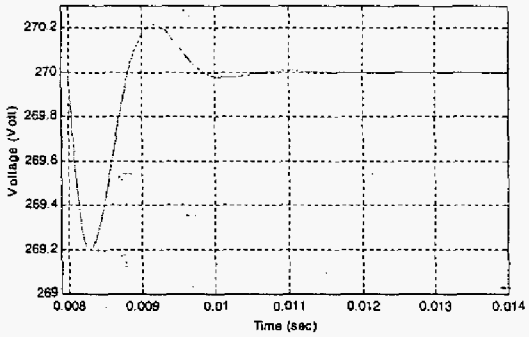

Fig. 14. Magnified plot of simulated capacitor voltage, V_c, as the power level steps-up

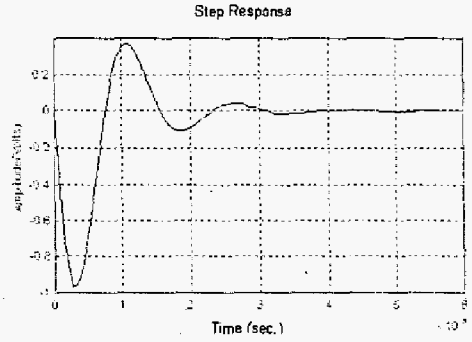

Fig. 15. Theoretical plot of V_c, as CPL power increases by 500 W

V. CONCLUSION

The analysis, theoretical design and simulation of a simple DC DPS consisting L-C filter, passive damping and a CPL were investigated extensively in this paper. The effect of the negative input resistance of the CPL on the filter has been analysed by using the small-signal input resistance of the load. The interaction between a source converter and a load converter, which is mainly due to the negative input impedance of the load converter, has been examined. The passive damping method was used to reduce the system interaction between the converters and the results were successfully verified by MATLAB Simulink simulation.

VI. REFERENCES

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